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A Low-power VCSEL Driving Structure Implemented in a 4 x 14-Gbps VCSEL Array Driver

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We present design and test results of a four-channel 4 x 14-Gbps VCSEL array driver ASIC with a novel output structure fabricated in 65 nm CMOS technology. The driver die features a size of 2000 μm × 1230 μm with four independent channels. Each channel receives 200 mVp-p differential CML signals and outputs a 2 mA bias current and a 5 mA modulation current at 14 Gbps/ch.

The analog core of each channel consists of the limiting amplifier (LA) and the output driver. The LA design includes a 3-bit RC degeneration equalizer and a four-stage pre-driver with the shared inductor structure. The innovative output driver adopts a PMOS current mirror as the load of the differential MOS at the output stage without the bandwidth degradation. The modulated current of the internal branch now can also contribute to the output branch. Thus the output modulation current can be - Imod ˜ Imod instead 0 ˜ Imod in the conventional design. The modulation efficiency is effectively improved at the output driver stage from the structure level.

The driver ASIC has been taped out and tested after integraed with a 4 channel VCSEL Array. Widely-open 14 Gbps optical eyes have been captured, and BER < 10E-12 has been achieved in the full channel optical test.

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