A Design of Clock and Timing System Prototype for Hard X-ray FEL Facility

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***Abstract*—Shanghai Hard X-ray Free Electron Laser Facility (SHINE) is aimed at producing the X-ray pulses in the photon energy range from 3 keV to 25 keV, which is under construction. To target the design purpose, SHINE requires quite precise clock distribution of the clock and timing system over distance of about 3.1 km. Based on the standard White Rabbit (WR) precision time protocol, this paper presents a prototype design of customized high precision clock and timing system. With the special clock processing methods, the system can meet the requirements of different devices in SHINE, including clock division, precision delay and duty cycle adjustment and adding MASK information. Test results indicate that the skew jitter RMS of distributed clock at the frequency from about 1Hz to 1MHz is less than 20 picoseconds and the clock phase delay can be adjusted up to 1 second with the step of about 400 picoseconds.**

***Index Terms*—prototype, Clock and timing system, precision delay adjustment, SHINE**

I. Introduction

Shanghai Hard X-ray Hard X-ray Free Electron Laser Facility (SHINE) is the first high repetition-rate X-ray free electron lasers facility in China. [1]-[3] Based on an eight GeV CW SCRF linac, the facility is built in a 3.1 km long tunel underground at Zhang-Jiang High Tech Park, which can generate X-ray pulses in the photon energy range from 3keV to 25keV. In SHINE, the Clock and timing system plays a crucial role. The distributed clock of multiple diagnostic and control device need not only a high quality and stability but also an ability of high precision automatic phase synchronization. In the existing accelerator devices, the clock and timing systems use electrical signal for clock distribution, which cannot achieve the mixed transmission of data and commands and the automatic phase compensation.

The White Rabbit (WR) precise time protocol (PTP) is an implementation of PTP in synchronous Ethernet optical fiber networks, which can achieve multi-node precision clock synchronization for sub-nanosecond levels within a range of 10 km [4]. However, the WR PTP is based on the standard network protocol with a 125MHz time base, which does not match the special mechanical frequency of SHINE. Based on the standard WR PTP, this design presents a customized time synchronization protocol running at the frequency of about 135.417MHz (135 times of the machine clock in SHINE). Meanwhile, in order to meet the complex requirements of different devices in SHINE, we also proposed a high precision clock shaping method to achieve flexible clock delay and duty cycle adjustment in this system.

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II. Design of the Clock and Timing System

A. Structure of the clock and timing systems

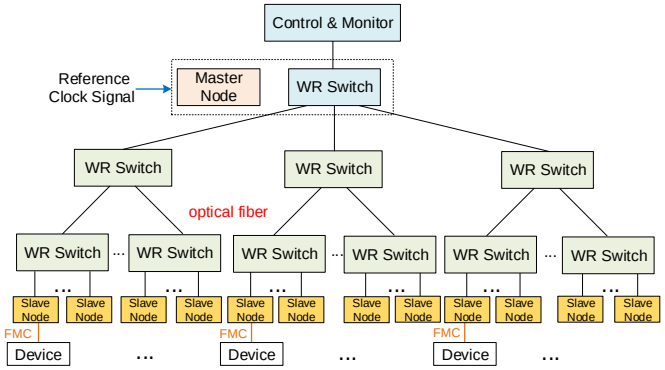

Fig. 1. Structure of the clock and timing systems

As shown in Fig.1, the clock and timing system mainly consist of three parts: the master node, WR switch and the slave node. Similar to the normal WR clock systems [4], the master node or grandmaster WR switch will receive reference clock signal including reference clock and related pulse per second (PPS) signal. According to the top-down network synchronization structure of WR PTP, the slave node will automatically compensate the phase difference with the upper WR switch. Meanwhile, each slave node electronics connect to other SHINE's devices through the FMC interface, sending the synchronous clock, data and commands.

B. Slave node electronics

As the crucial part in the clock and timing system, the slave node will complete the automatic phase compensation and flexible clock processing. The details is shown in Fig.2.

As mentioned above, the slave node mainly has two part peripheral circuits besides the FPGA: the WR clock recovery system (CRS) and the clock processing circuits (CPC).

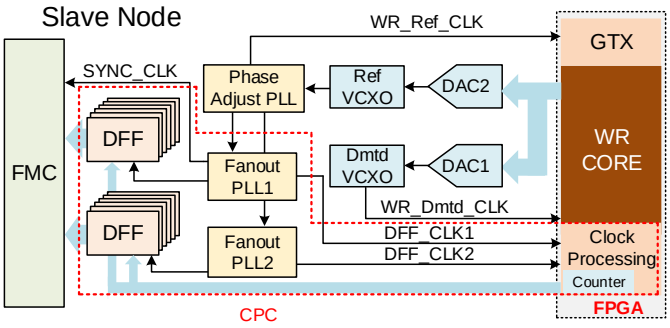

Fig. 2. Block of the slave node

The customized WR CRS is similar to that of standard WR [4] except for the special center frequency of the reference temperature-compensated voltage controlled crystal oscillator (Marked as "Ref VCXO" in Fig. 2). The other circuits, including two fan-out PLL, 12-channels D Flip Flop (DFF), combining with the related logic in FPGA, complete the flexible clock processing functionality. Using the peripheral circuits of the PLLs and DFFs rather than the resources in FPGA aims to ensure the high quality of the distributed machine clocks that are finally sent to devices through FMC interface. In addition, the fan-out PLL can also accomplish multi-channel fine delay adjustments with a step of about 400 ps.

C. *Master node electronics*

The master node electronics can be configured as the WR grandmaster model or the slave model. Its main task is to send the control commands or information through the WR network. The circuit structure of master node is similar to the slave node. We do not repeat the details no more here.

III. Test Results of the Clock and Timing System

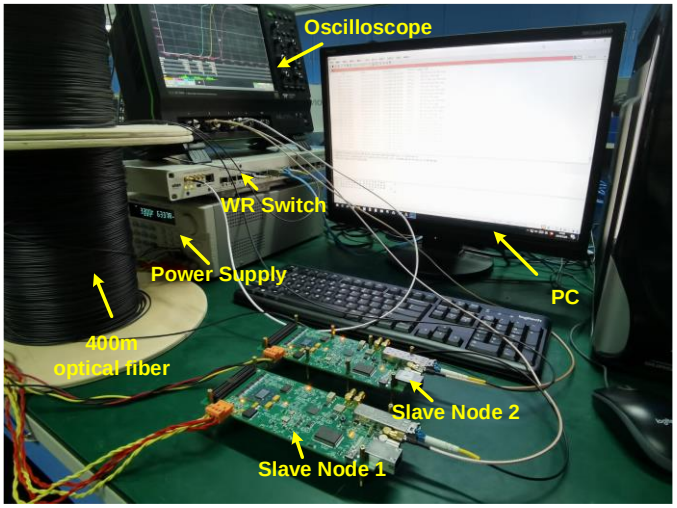

Fig. 3. Prototype system under test

We conducted a series of tests to evaluate the performance of this prototype system. Shown in Fig. 3 is the prototype system under test. Applying the internal clock of WR switch as the clock source, the two slave nodes finish the automatic phase compensation and the same clock processing operation, and then feed the distributed machine clock to oscilloscope for measurement.

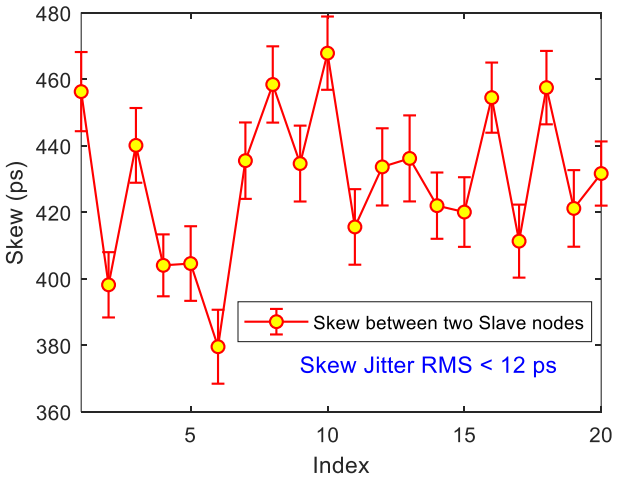

Fig. 4. Skews between two slaves after powering up and down multiple times

In order to evaluate the performance of automatic phase compensation, we powered up and down the whole prototype circuits 20 times. Shown in Fig. 4. is the skews of the synchronous machine clock in two slave nodes. The results indicate that the skew jitter RMS of distributed clock is less than 12 picoseconds and the peak-to peak skew varies within the range of 120 picoseconds after powering up and down multiple times, which can meet the requirements of the clock and timing systems.

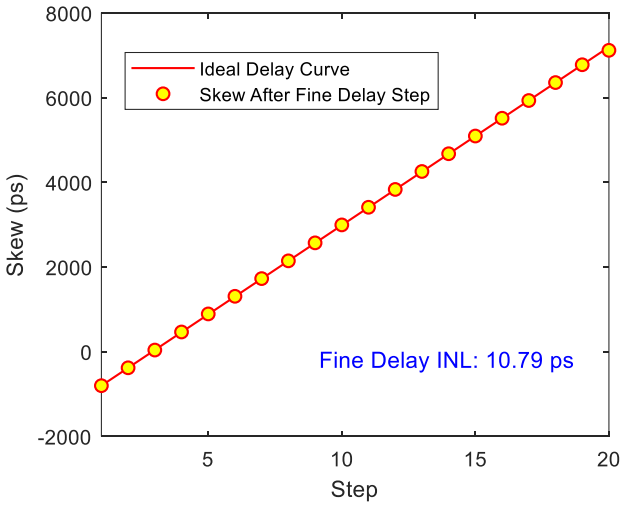

Fig. 5. Phase adjustment test of fine delay

Meanwhile, we also tests the clock phase delay of the prototypes. As mentioned above, the phase delay adjustment consists of the coarse adjustment in FPGA and the fine delay by the PLLs circuits. Fig. 5. presents the test results of the fine delay. With the fine delay circuits, we can achieve about fine delay with the step of about 400 picoseconds in a coarse clock cycle and the INL of the fine delay is less than 15 ps.

IV. Conclusion

Due to the requirements of long-distance high-precision synchronous clock distribution in SHINE, based on the standard WR PTP, we designs the clock and timing systems.

Meanwhile, the new clock shaping method is proposed for ensuring the quality of the machine clock after any multiple division and arbitrary delay adjustment. Test results indicate that the system can realize the long-distance clock synchronization and the distributed clocks' skew jitter is better than 20 ps. In addition, with the clock processing methods, the phase delay up to 1 second with the step of about 400 ps can be finished in the systems.

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