MDT Level-0 Trigger
FPGA Mezzanine Card (FMC)
Prototype V0

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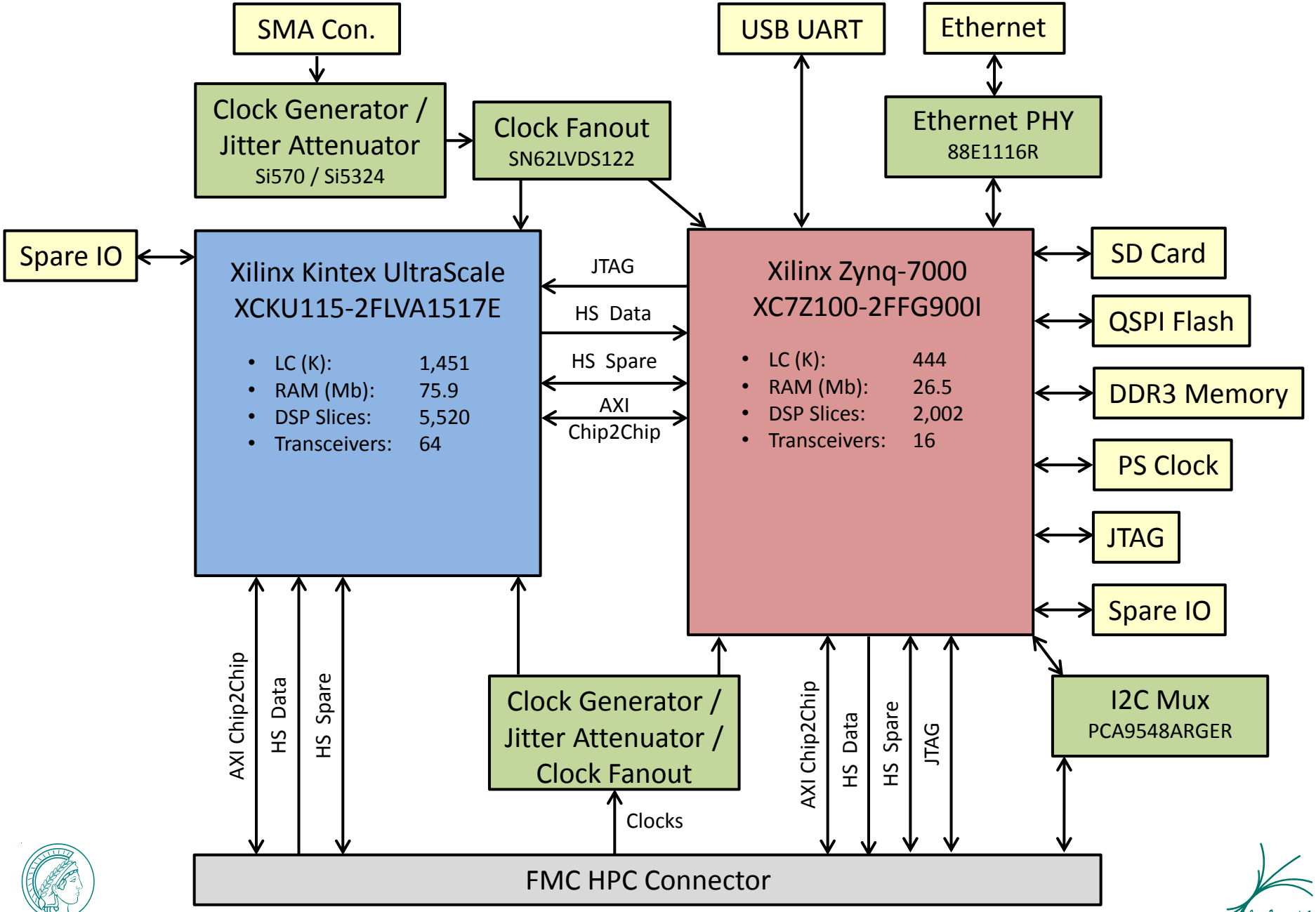
M. Fras, Electronics Division,
MPI for Physics, Munich

L0MDT FMC V0 – Features and Purpose

- FMC HPC mezzanine card sitting on the L0MDT ATCA blade prototype V0.
- Optional stand-alone operation in order to be independent of the blade:
  - Cost, availability, power consumption, heat production, space required on desk, …
  - Provide JTAG connector, Ethernet port, SD card slot, on-board clocking.
- Provide all infrastructure in order to:
  - Develop and test firmware and software framework as prototype for the final L0MDT hardware.
  - Implement and test the 1D segment finding algorithm for one muon in a sector (inner + middle + outer layer).
  - Implement and test the 2D segment finding algorithm for one muon.
  - Run Linux and / or bare metal applications on the ARM processor.
  - Perform track reconstruction and p_T evaluation either on an ARM core or in the FPGA fabric.
- Provide sufficient spare IOs, connectors, LEDs, jumper, buttons for easy testing and optional extensions.

L0MDT FMC V0 – Block Diagram



L0MDT FMC V0 – Components

- Zynq boot: See ZC706 schematic, pages 9, 15
- DDR3 Memory: See ZC706 schematic, pages 17-20
- QSPI Flash: See ZC706 schematic, page 21
- SD Card: See ZC706 schematic, page 22
- FMC HPC: See ZC706 schematic, page 24
- Ethernet: See ZC706 schematic, page 29 & 30
- I2C Mux: See ZC706 schematic, page 38
- USB UART: See ZC706 schematic, page 40

L0MDT FMC V0 – Signals

- AXI Chip2Chip:
  - SelectIO (~ 20 traces)
  - Serial link: Aurora, requires RefClk and free running clock
- High Speed, low latency data links:
  - ATCA blade to FMC: xx links, yy Gbps
  - Kintex UltraScale to Zynq-7000: xx links, yy Gbps
  - Zynq-7000 to ATAC blade: 12 links, 9.6 Gbps (12 x lpGBT to FELIX)
- High Speed, low latency spare links:
  - ATCA blade <-> FMC: xx links, yy Gbps
  - Kintex UltraScale <-> Zynq-7000: xx links, yy Gbps
  - Zynq-7000 <-> ATAC blade: xx links, yy Gbps
- JTAG:
  - Access from Xilinx header.
  - Alternative access from the ATCA blade.
- I2C:
  - Access to clock generators, switches, etc, on the FMC.
  - Alternative I2C access from the ATCA blade.

L0MDT FMC V0 – JTAG

- Purpose of the JTAG on the FMC:
  - Download firmware to the Zynq-7000 and the Kintex UltraScale (KU) FPGA
  - Store firmware image in the QSPI flash
  - Debug the ARM cores of the Zynq-7000
- JTAG chain options:
  - 2mm 2X7 JTAG header -> Zynq -> KU
  - FMC connector -> Zynq -> KU
  - Zynq as JTAG master for the KU, so that the firmware of the KU can be downloaded by the Zynq PL/PS: Zynq -> KU
- Jumper or DIP switches to select between the JTAG chain options.
- See ZC706 schematic:
  - Page 3: JTAG connection to Zynq (U1)
  - Page 16: 2mm 2X7 JTAG header (J3)
    Buffer for JTAG signals (U10)
- All JTAG signals shall be routed through 0 Ohm resistors for testing, debugging and optional extensions/fixes.

L0MDT FMC V0 – Clocking

- Local clocks on FMC:
  - 33 MHz for Zynq PS
  - MGT RefClk for AXI Chip2Chip
  - Free-running clock for AXI Chip2Chip
  - MGT RefClk for spare serial links
- Clocks from the ATCA blade:
  - LHC clock (fanout to Zynq and KU)
  - (lp)GBT RefClk (fanout to Zynq and KU)
  - MGT RefClk for high speed, low latency Chip2Chip data
  - AXI Chip2Chip clock (RefClk for serial interface, PHY clock for SelectIO interface)
  - Auxiliary clock

L0MDT FMC V0 – I2C Bus Tree

- I2C Masters:
  - Zynq-7000 PS
  - ATCA blade through FMC connector
- I2C Slaves:
  - I2C multiplexer
  - Clock synthesizers, jitter cleaners
  - Crosspoint switches
- All I2C signals shall be routed through 0 Ohm resistors for testing, debugging and optional extensions/fixes.

L0MDT FMC V0 – Boot and Configuration

- Zynq-7000 boot options:
  - JTAG
  - QSPI flash
  - SD card
- Zynq-7000 boot documentation:
  - ug585-Zynq-7000-TRM.pdf
    - General description: Section 6.1
    - Boot mode MIO pins: Table 6-4
  - See ZC706 schematic
    - Zynq MIO connections (bank 500, 501): Page 9
    - Boot selection switch incl. reset: Page 15
    - Dual QSPI flash: Page 21
    - SD card: Page 22
- Kintex UltraScale boot options:
  - JTAG