



Timing for DAQ



ISOTDAQ 2019 – Royal Holloway, University of London

Sophie.baron@cern.ch



Outline



- A bit of Vocabulary
- Timing in the LHC
- Timing for Front End Detectors
- Timing for Trigger & DAQ
- What is a good timing distribution system for LHC detectors?
- Current timing distributions systems
- New Challenges for Timing distribution in HL-LHC

Time



- the indefinite continued progress of existence and events in the past, present and future regarded as a whole (*Oxford Dictionary*)
- the measured or measurable period during which an action, process or condition exists or continues (*Webster's Collegiate Dictionary*)

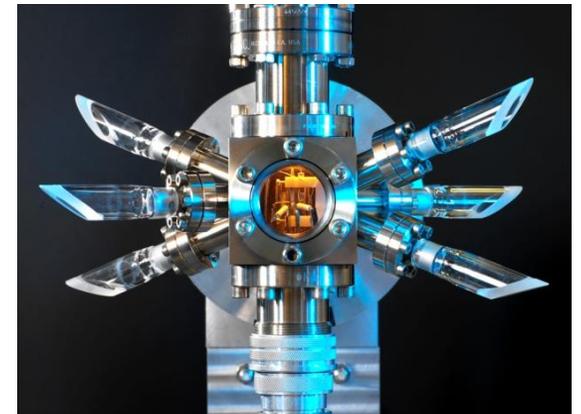
...and also...

- what prevents everything from happening at once (*physicist John Wheeler and others*)
- a linear continuum of instants (*philosopher Adolf Grünbaum*)
- a continuum that lacks spatial dimensions (*Encyclopaedia Britannica*)
- **what clocks measure** (*attr. to physicists Albert Einstein, Donald Ivey, and others*)

Clock

...a physical mechanism that counts the passage of time

- Calendar based on Sun, Moon and Stars, Sundials, water clocks
- 1656 Christiaan Huygens: Pendulum
- 1920 Quartz oscillators
- 1950 atomic clocks
- 1967 definition of SI standard 1 sec based on Caesium atom
- Currently: Optical atomic clocks



A strontium-ion optical clock, Nature

Time Standards

Two widely used time standards:

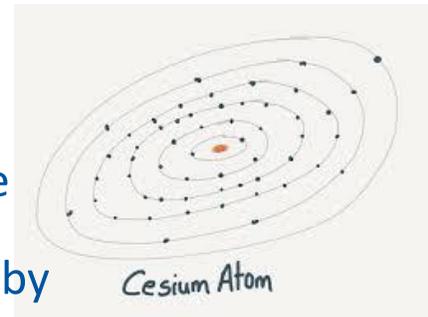
1. GMT/UT - Based on earth rotation

- not uniform due to periodic changes and long term drifts
- Varies by ~ 1 sec/year (order $< 10^{-8}$)
 - **UT1** - Universal Time (UT1) is a measure of the actual rotation of the earth, independent of observing location. Formerly called Greenwich Mean Time (**GMT**).



2. TAI/UTC - Based on atomic oscillations (cesium 133)

- Currently the closest approximation to a uniform time
- Varies ~ 1 us/year (order $< 10^{-14}$)
 - **TAI** - International Atomic Time - the primary time standard in the world today. It is the combined input of many clocks around the world
 - **UTC** - Coordinated Universal Time - is the time broadcast by WWW and other services by technologies such as the GPS satellites and Network Time Protocol (NTP).

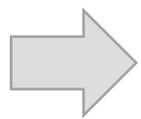


<http://www.cv.nrao.edu/~rfisher/Ephemerides/times.html>

Aligning the time standards

- By definition, UTC and TAI have the same rate, but UTC stays close to Mean Solar Time by adding integer numbers of seconds, called **leap seconds**, from time to time to keep $UT1-UTC < 0.9$ s (today, $UTC - TAI = 37$ seconds)
- The difference, $DUT1 = UT1 - UTC$ is monitored by the International Earth Rotation Service and published weekly in IERS Bulletin A along with predictions for a number of months into the future.

<http://www.leapsecond.com/java/gpsclock.htm>

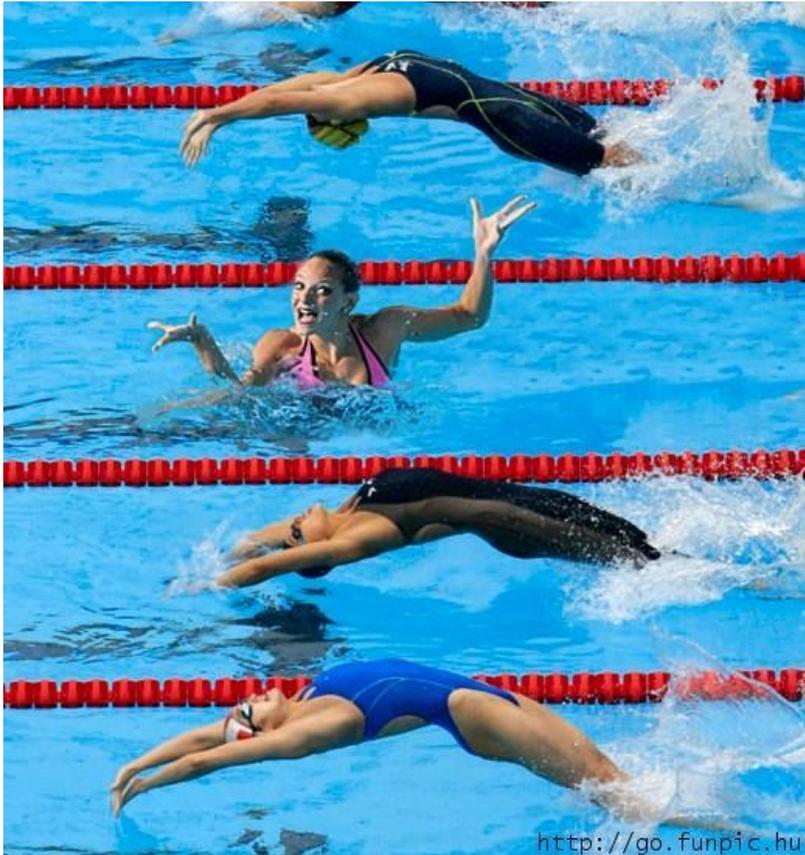


This is a tentative of '**synchronization**' of UTC versus UT1.
Two different clock sources, as precise as they might be, drift one from each other.

Synchronization

- the coordination of events to operate a system in unison

aesthetic consequences



...or dramatic ones



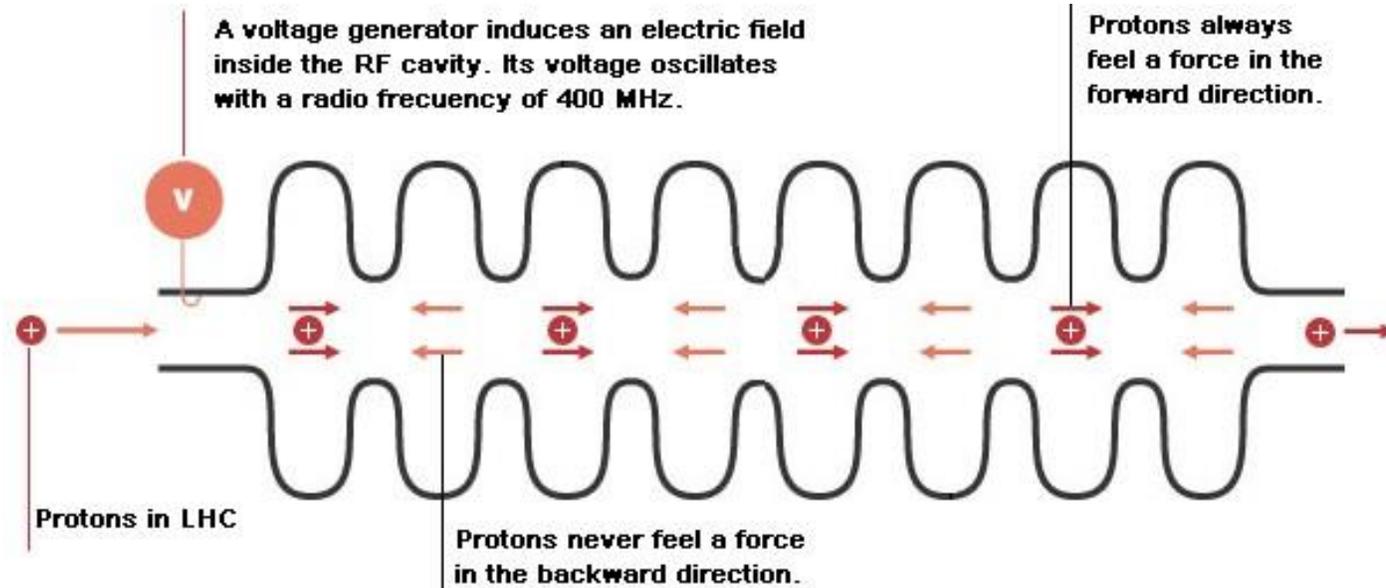
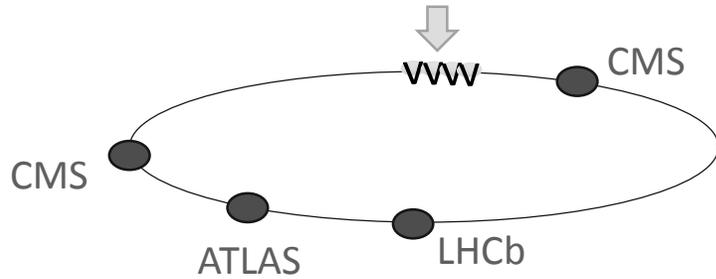
The Sopwith Camel

Timing in the LHC



LHC's "atomic clock": the RF

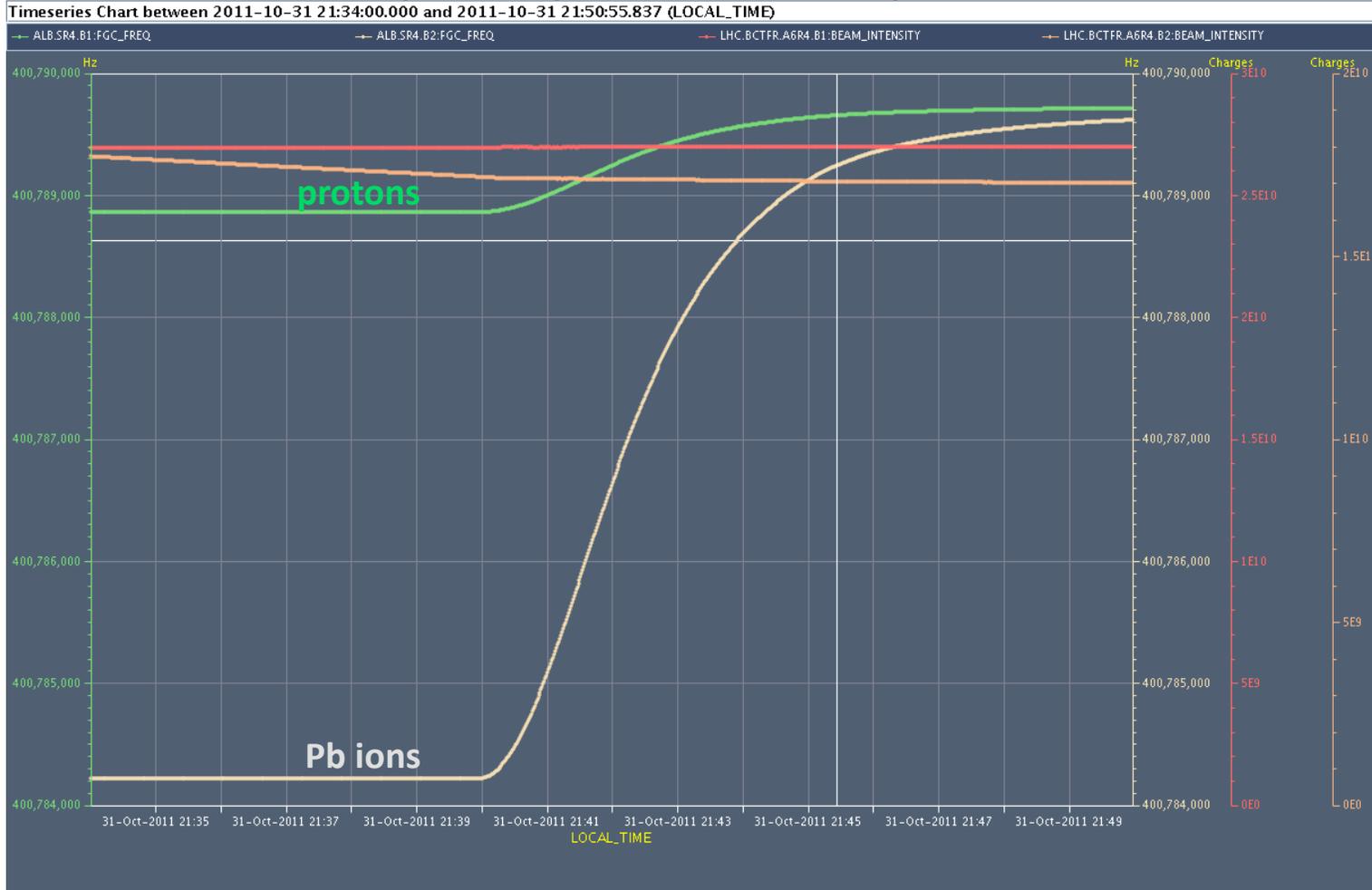
RF cavities in LHC
(4 modules@point4, Echenevex)



RF= Radio Frequency

The LHC RF

- The Radio Frequency is **not always the same**



The Radio Frequency is not fixed:

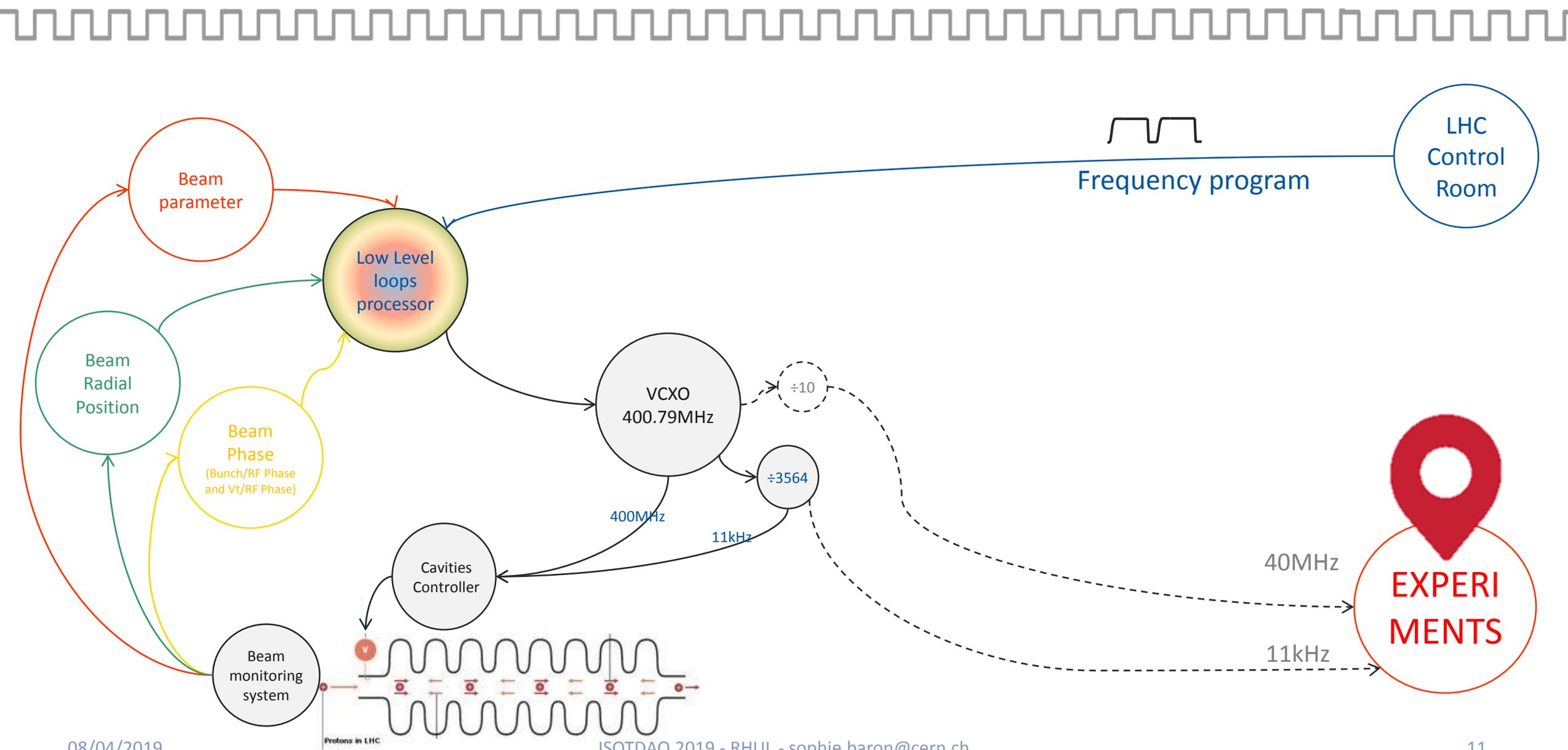
- it is a **function of particle type and energy**
- It is **ramping up** at the beginning of each fill

400.788860 MHz -> 400.789715 MHz (protons)

400.784216 MHz -> 400.789639 MHz (ions)

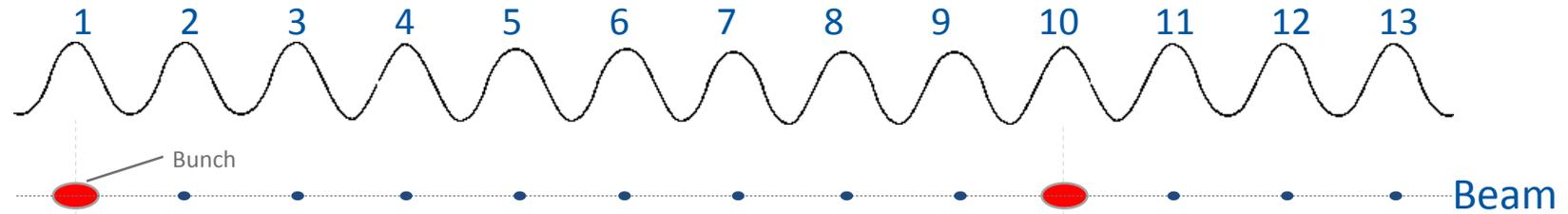
- it is **modulated** by beam characteristics and RF parameters
- It is however **extremely stable** during flat top (ie during collision time).

The LHC RF Modulation Scheme (simplified)

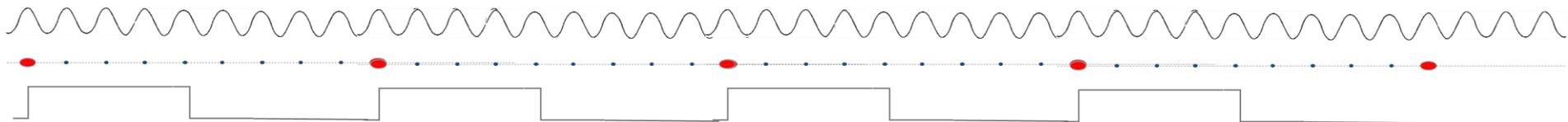


The LHC RF & the Particle Bunches

Buckets
LHC RF
~400.8MHz

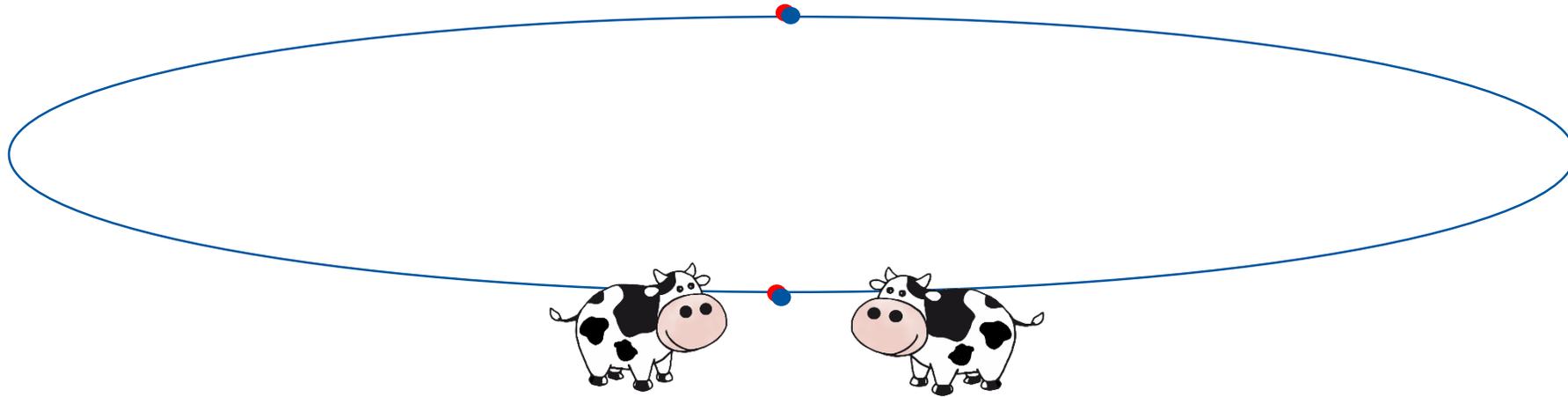


LHC Bunch Clock
~40.08MHz



The Bunch Clock is the frequency at which an observer sitting close to the ring could 'see' particles passing

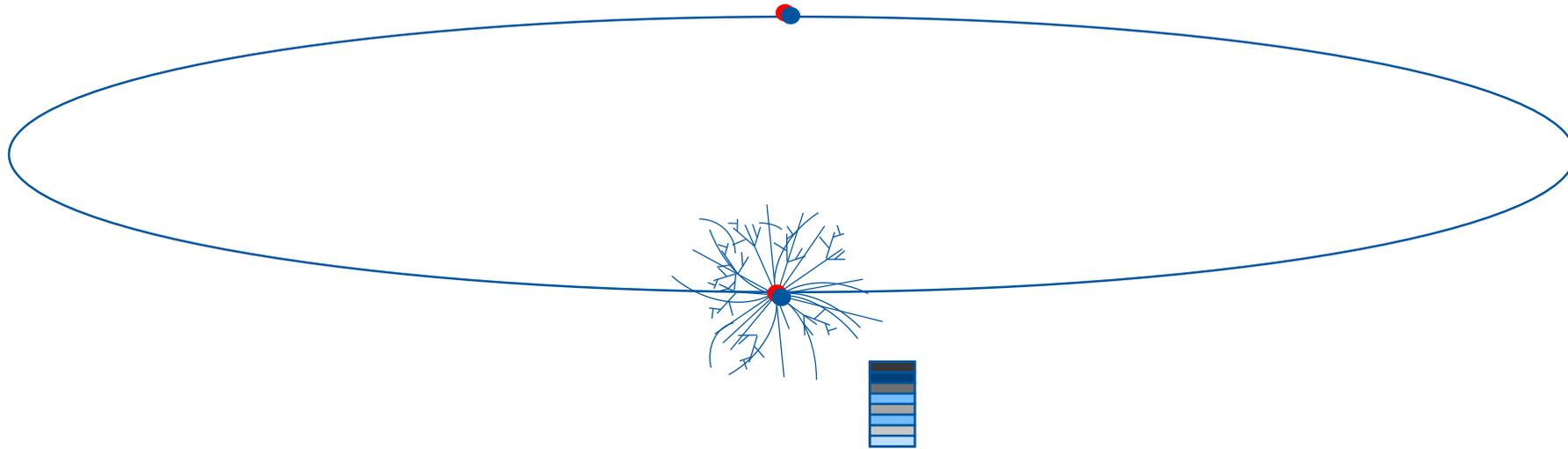
The LHC Bunch Clock



BC frequency ~ 40.079 MHz

Orbit (Revolution Frequency) ~ 11.2 kHz

The LHC Bunch Clock & the collisions

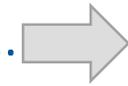


The BC: the heart beat of the LHC detectors

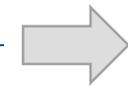


In LHC detectors, **everything** is happening **synchronously to the Bunch Clock**:

- Collisions
- Signal sampling for Analogue to Digital conversion.....
- Event stamping
- Sorting event data (coincidences)
- Trigger generation
- Particles identification
 - Measuring the time of flight between two points to obtain the velocity
 - Combining with momentum information to derive the mass
- Track reconstruction
- Vertex reconstruction (between 20 and 60 piled up events per collision at LHC)
- Event reconstruction



Individual need of each front end sensor



System need (Trigger, Event reconstruction)



The Bunch Clock (40.079MHz) has to be delivered

- EVERYWHERE,
- ANYTIME,
- and with an excellent STABILITY & QUALITY

The Orbit signal (a.k.a. revolution frequency) (11.24kHz) is also needed

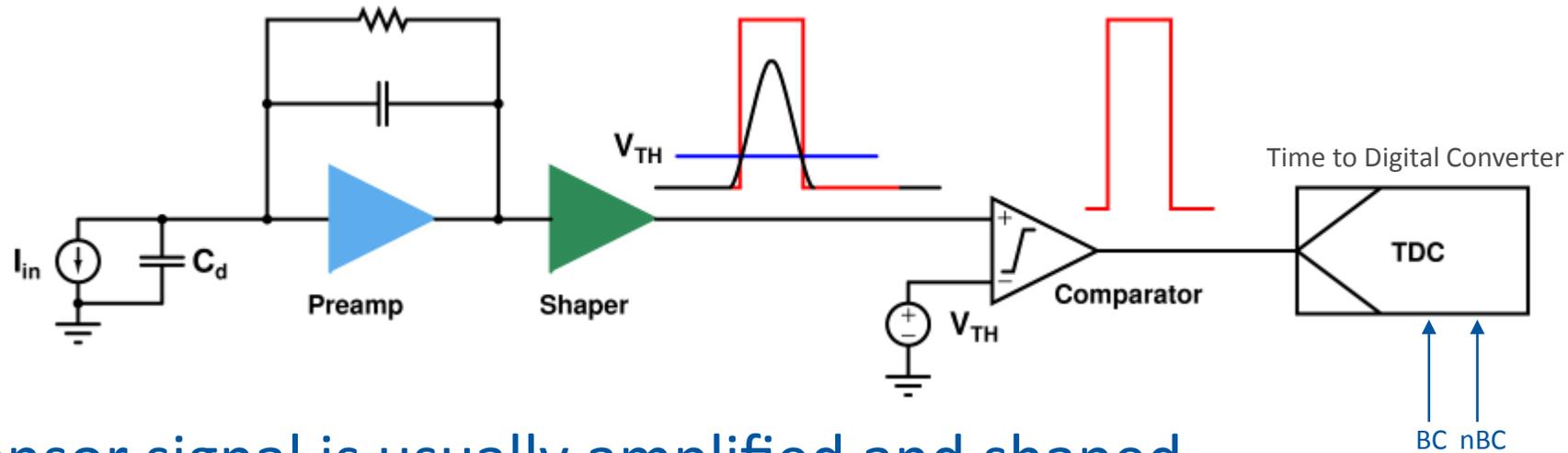
Timing for ...

Detector front end electronics

Trigger & DAQ

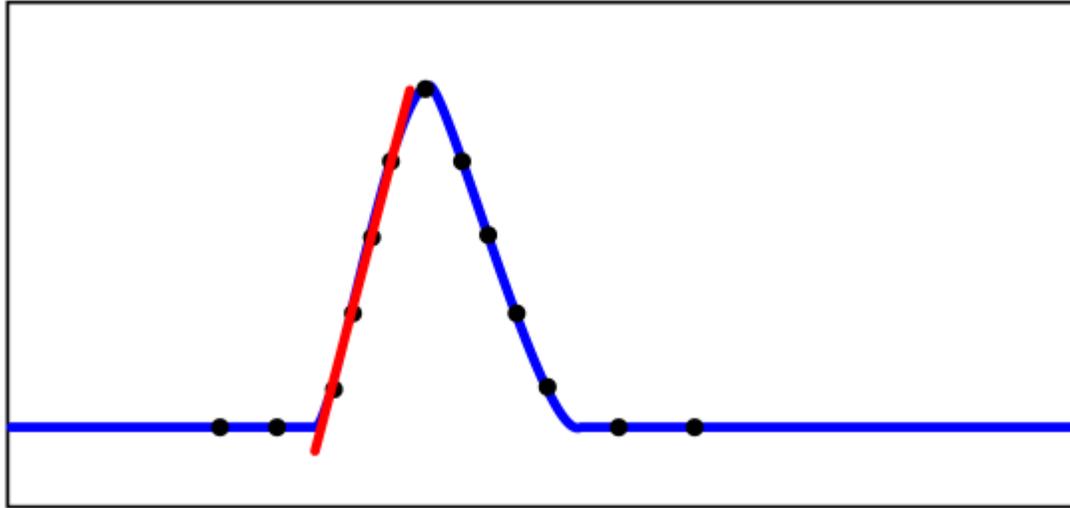


Detector front-ends: single sample



- The sensor signal is usually amplified and shaped
- A comparator generates a digital pulse
- The threshold crossing time is captured and digitized by a TDC
- TDC measures the passing time of the pulse/particle
 - uses the **Bunch Clock** as a start event
 - a high speed clock counts the elapsed time— **a multiple of the Bunch Clock**

Detector front-ends: multiple samples



- The sensor signal is usually amplified and shaped
- The full waveform is sampled and digitized at high speed (**a multiple of the Bunch Clock**) by an ADC
- Information on shape, amplitude, passing time is extracted with DSP algorithms from the digitized waveform samples

Timing Accuracy for Detectors Front-Ends

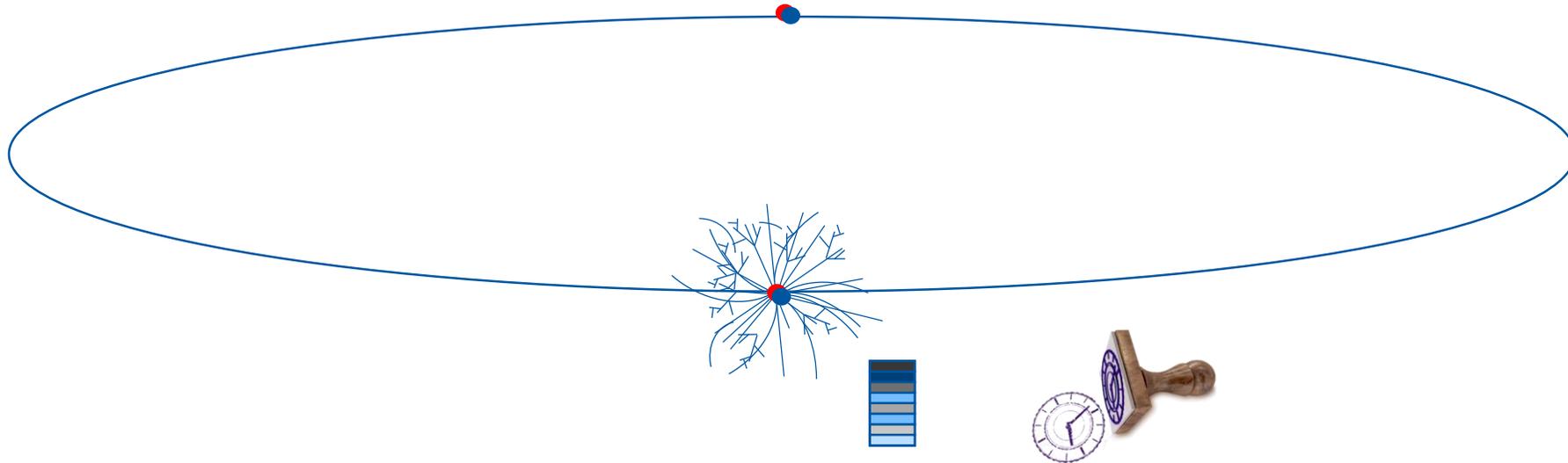


- Several factors challenge the accuracy of these systems:
 - Random noise internal to the front-end electronics
 - Signal integrity (substrate noise, etc..)
 - Pulse amplitude variations
 - Pulse shape variations
- **Random & deterministic noise from the clock distribution system**
 - Irregular sampling clock distorts the signal or gives a wrong passing time information
 - Multiplying a dirty clock makes things even worse

Timestamping for Trigger & DAQ

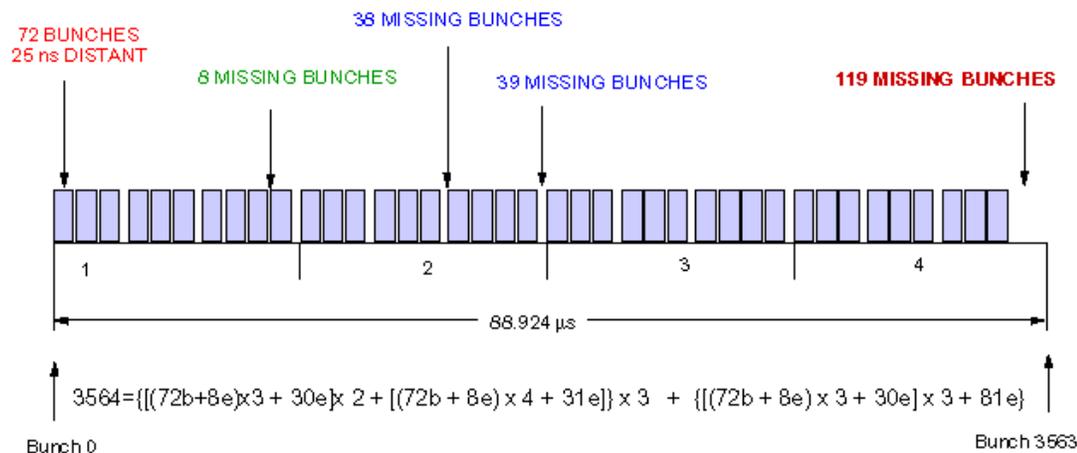


...crucial for event reconstruction!



Timestamping for Trigger & DAQ

- Every single bunch crossing is timestamped in each Front End module using a local counter incrementing at the collision rate (BC – 40.079MHz)
- This counter is usually reset at every turn by Orbit/Revolution frequency (11.24kHz), which is every 3564 BC periods
- Note that all the timestamps don't necessarily carry a collision (bunch structure) ... but that each bunch crossing carries up to 60 collisions (pile up)



Timing distribution ...



- Timing distribution systems in LHC experiments are in charge of
 - **Distributing the Bunch Clock** signal to each node of the detectors
 - With **accurate and stable frequency** – for accurate signal shaping
 - With a **fixed phase** with respect to the beam/collisions – for proper timestamping
 - **Broadcasting time critical signals** to each node of the detectors
 - Orbit
 - Trigger
 - And some other time critical signals
- ...with a **low, fixed and deterministic latency**

What is a good timing distribution?

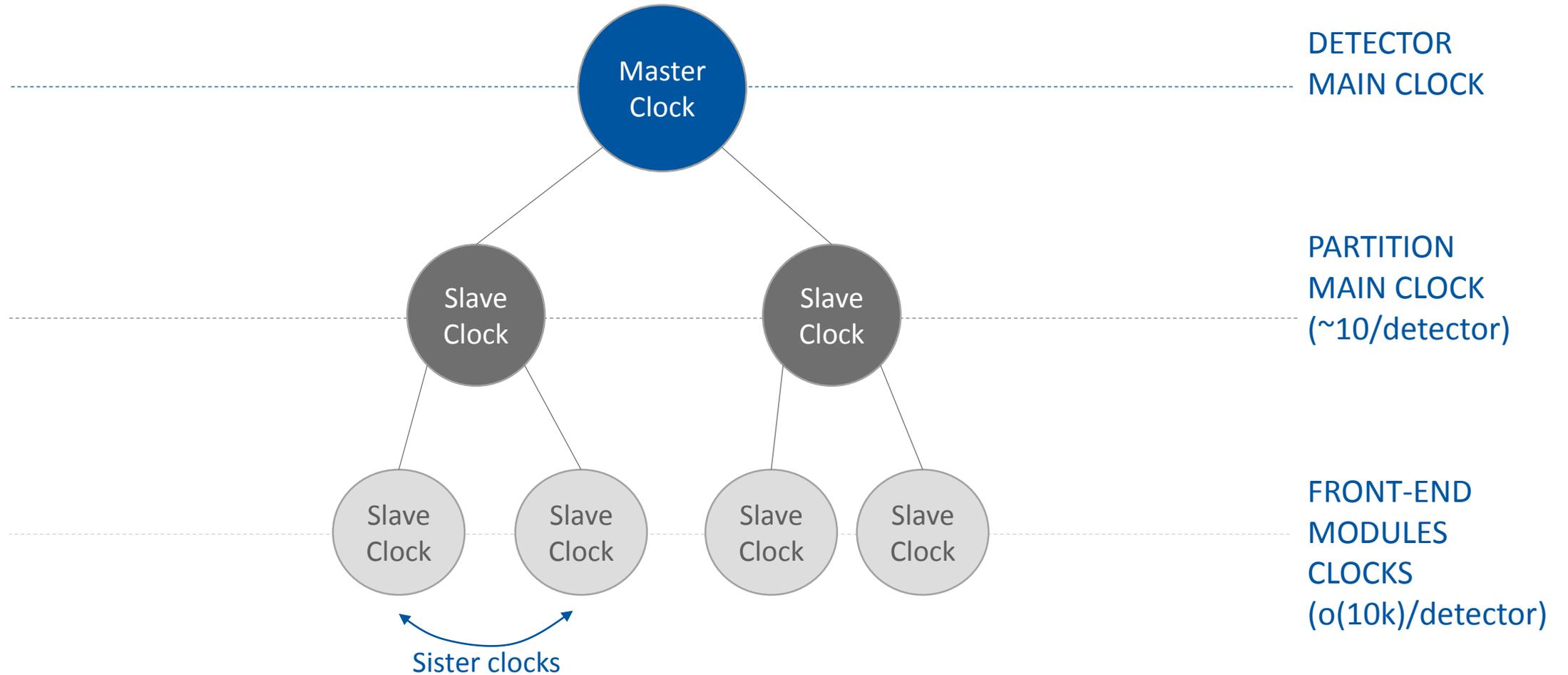
Distribution systems ..

Assessing distribution quality ...

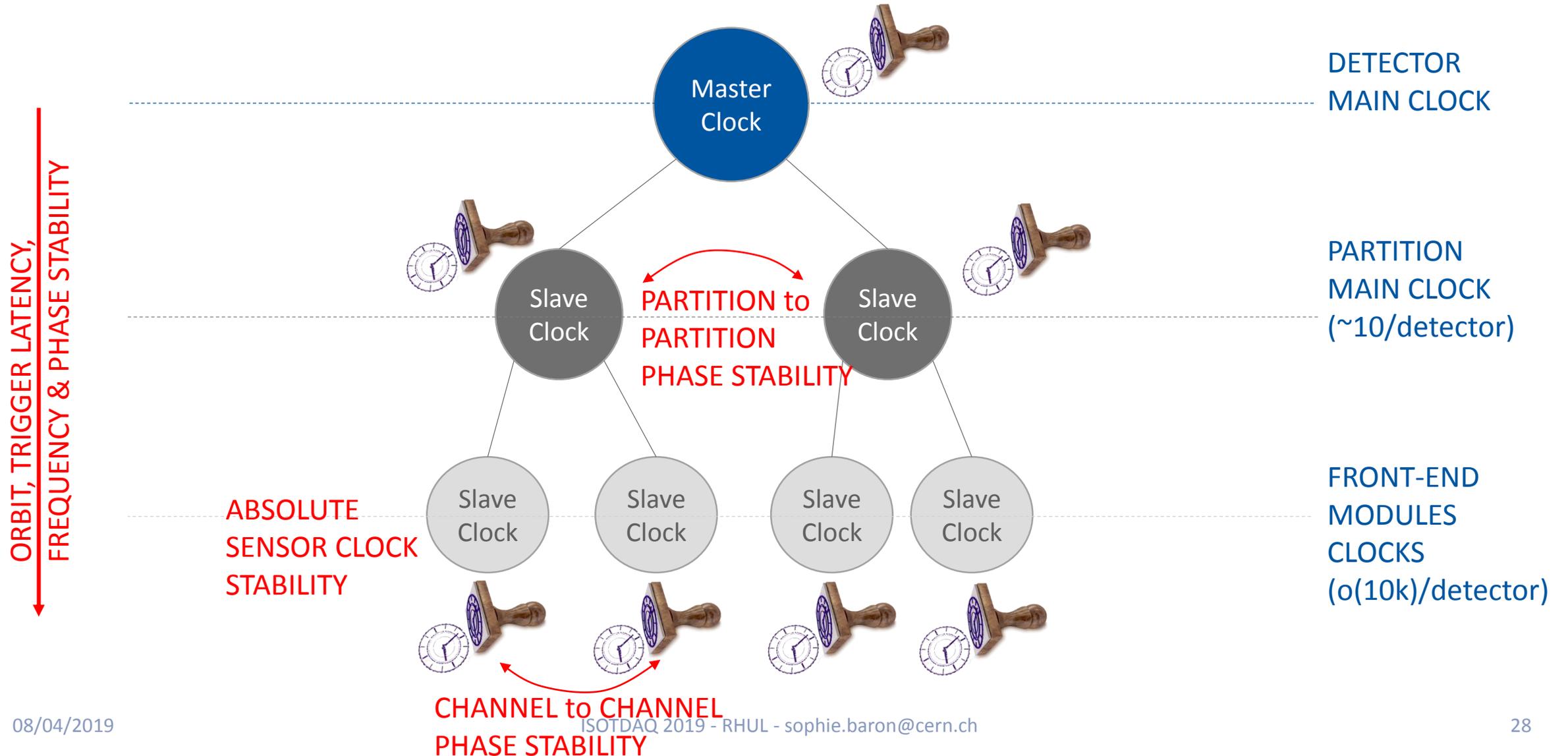
Good clock for ...



Timing Distribution System in a detector



Timing Distribution System in a detector



Jitter & Phase Noise



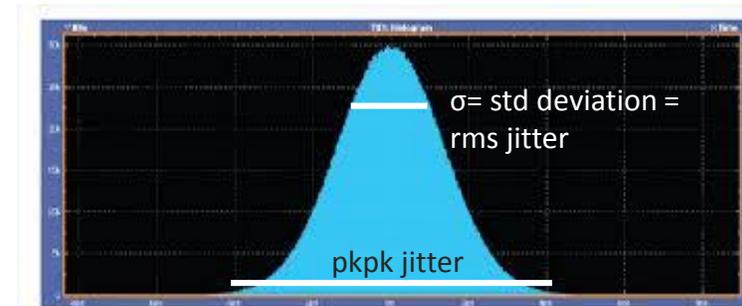
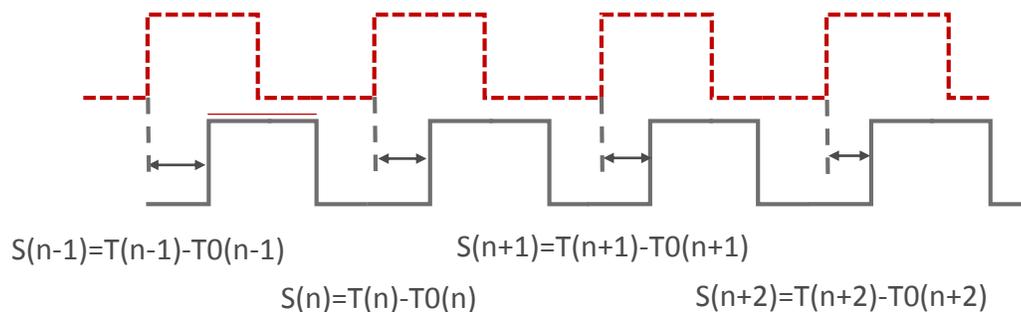
How to assess the quality of a clock?

- Jitter (in the time domain)
- Phase Noise (in the frequency domain)

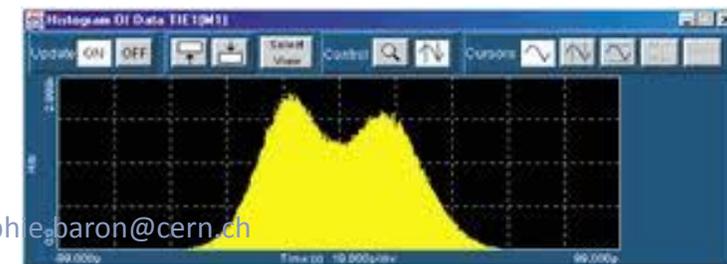
Jitter



- **Time domain** measurement
- Various Jitter types (Cycle-to-cycle, period, ..)
- TIE jitter (Time Interval Error or accumulated/phase Jitter):
 - Actual deviation from the ideal clock period over all clock periods
 - The « Ideal Clock » can be an absolutely perfect reference, the master of a distribution system or a sister clock (skew jitter)
 - Measured with real time oscilloscopes
 - Histogramming its Probability Density Function gives interesting information on jitter sources.
 - Spectrally rich type of jitter

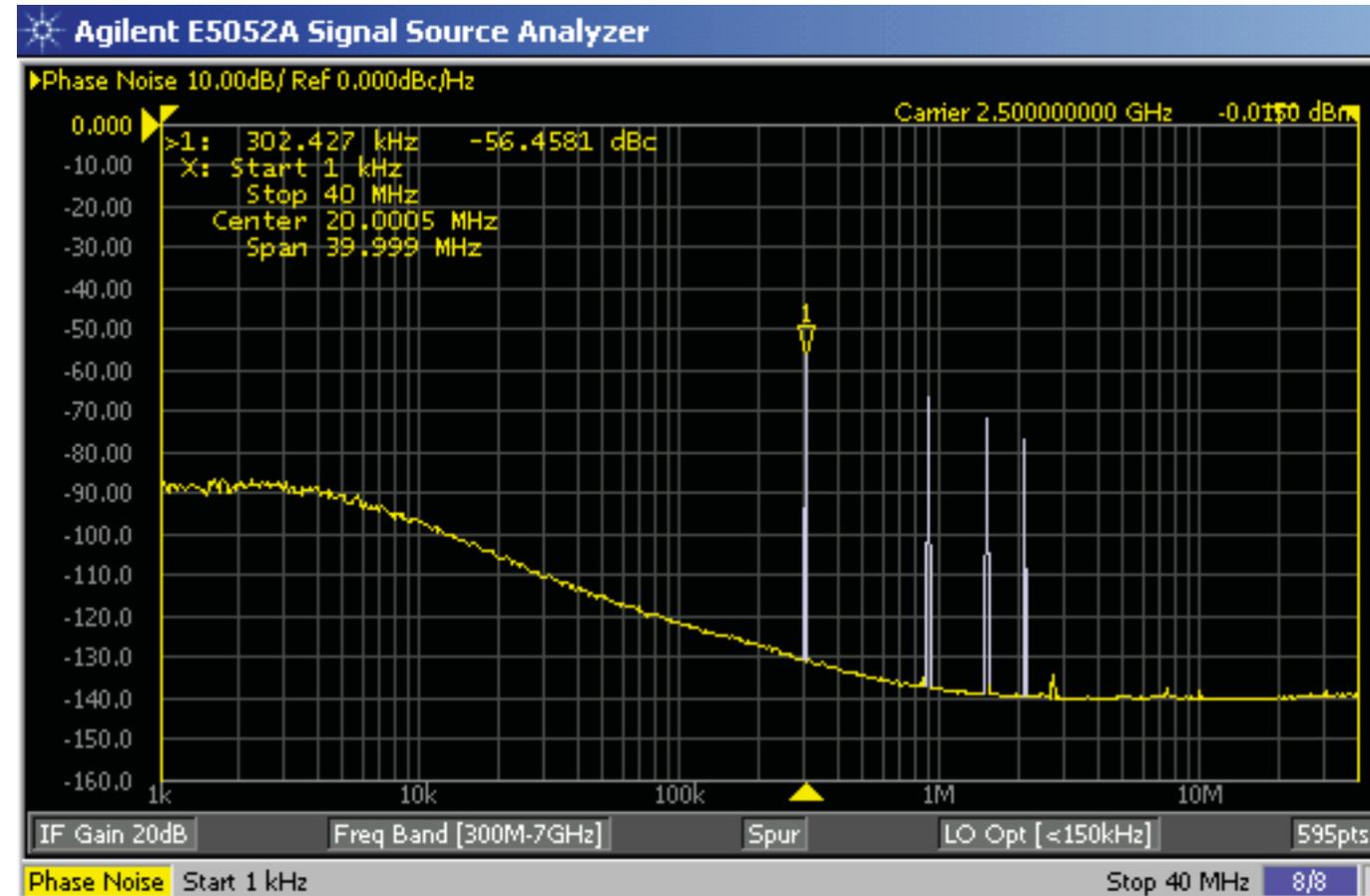


Random jitter:
Gaussian shape



Deterministic
Jitter

Phase Noise



$$a_{ideal}(t) = A \sin(2\pi f_c t)$$

$$a_{real}(t) = A(1 + \alpha(t)) \sin(2\pi f_c(t + \varphi(t)))$$

$$a_{digital}(t) = A \sin(2\pi f_c(t + \varphi(t)))$$

Phase Noise = $\left(\frac{\text{Spectral power density at foffset}}{\text{total power of the carrier signal}} \right)$ F_{offset} = Offset Frequency from the signal carrier frequency

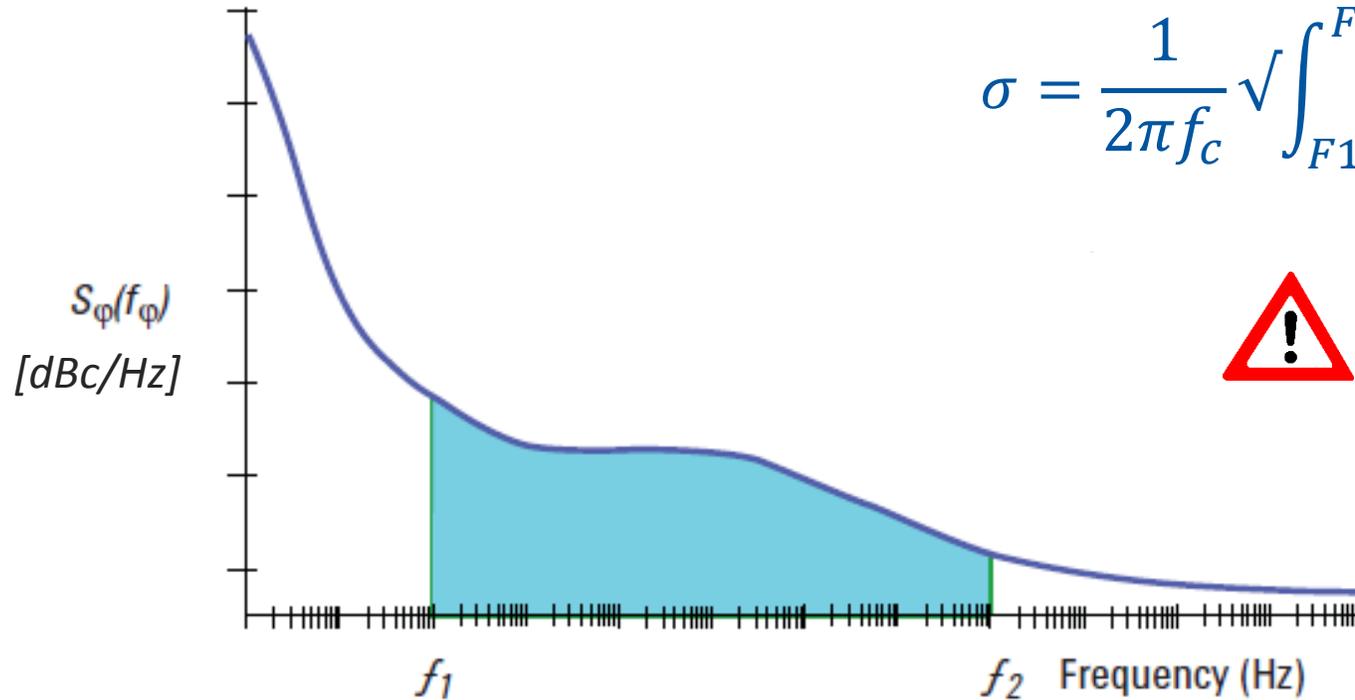
Frequency & Time Domains relationship



= Phase Noise & Jitter relationship

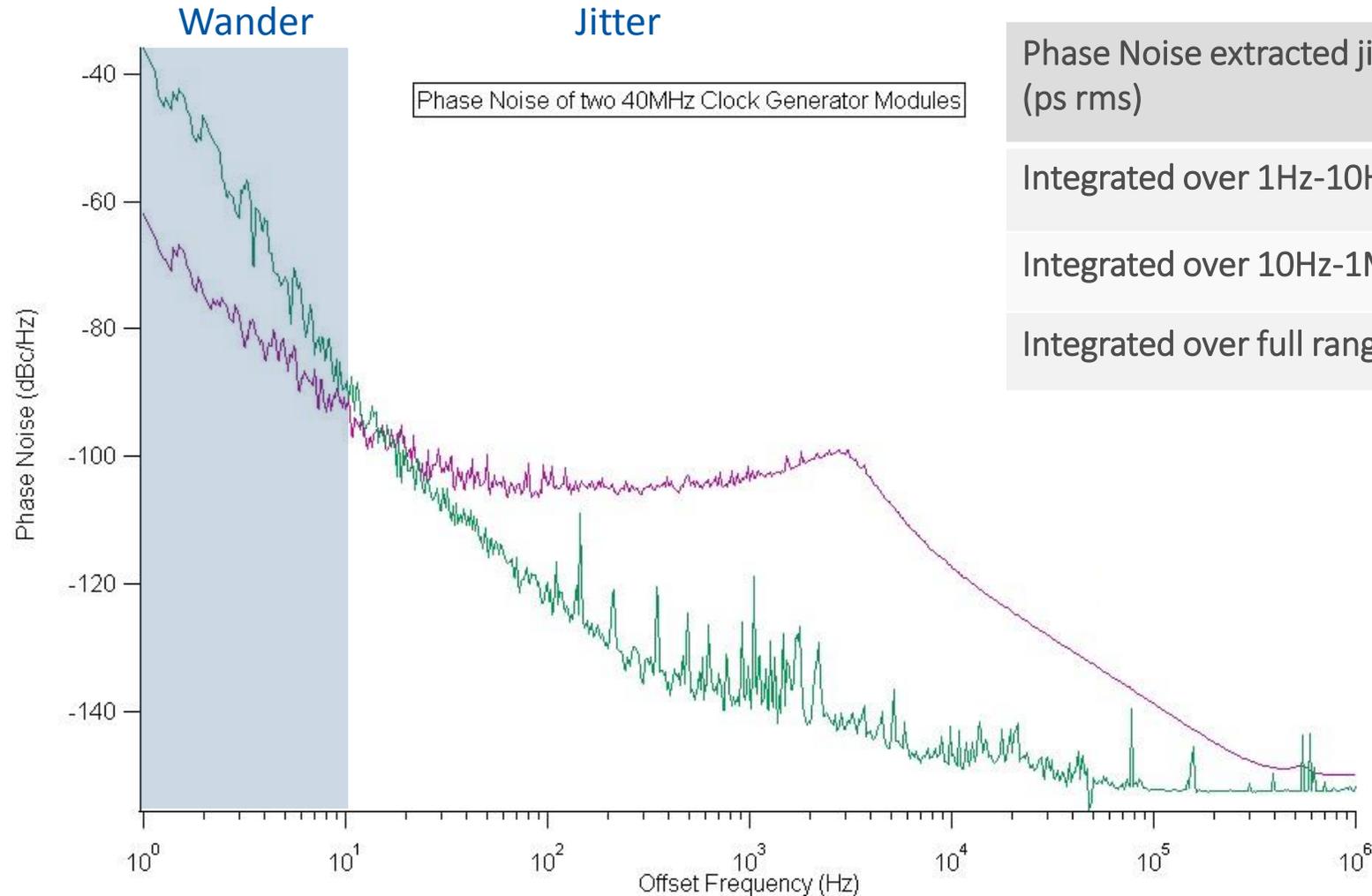
TIE jitter (rms) is close to

$$\sigma = \frac{1}{2\pi f_c} \sqrt{\int_{F1}^{F2} S\varphi(f) df}$$



[F1;F2] = integration range

Phase Noise interpretation



Phase Noise extracted jitter (ps rms)	Clock generator	Crystal Oscillator
Integrated over 1Hz-10Hz (wander)	1.78 ps rms	30.5 ps rms
Integrated over 10Hz-1MHz	2.39 ps rms	0.97 ps rms
Integrated over full range	2.98 ps rms	30.5 ps rms

— Clock generator
— Crystal Oscillator

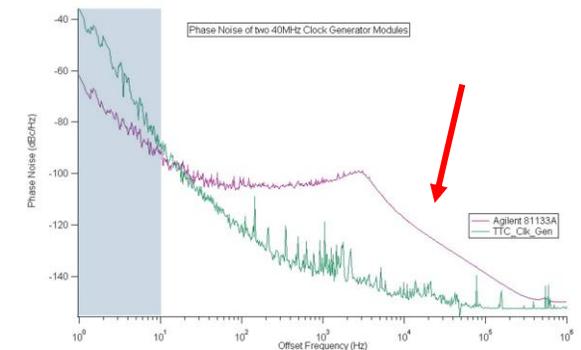
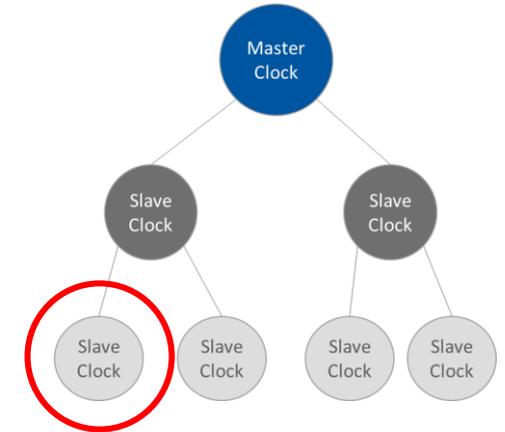
A good clock for individual sensors...



- Sensors are very sensitive to timing errors as they directly convert into sampling errors
- Unregular sampling edges can distort of the shape of digitized pulses.

=> remove the high frequency jitter

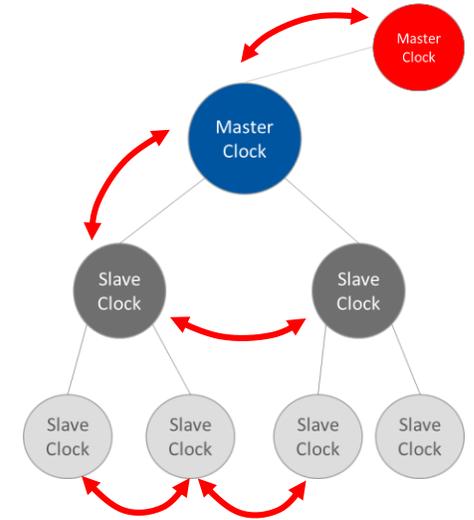
...use PLLs – Phase Lock Loops



A good clock for a (sub) detector/system...

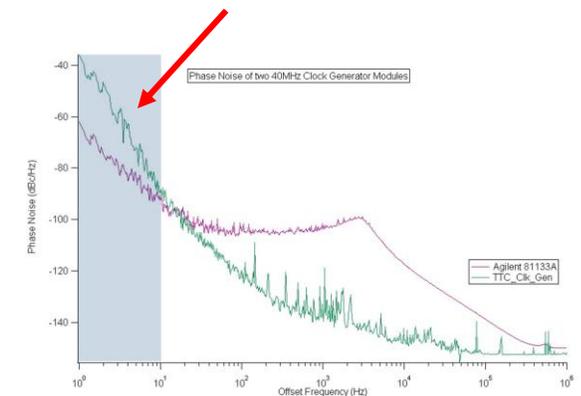


- Track, vertex or event reconstruction
- 1000s of Bunch Clock destinations spread all over the detectors
 - Beware of sister clocks drifting one from each other
- stable phase between Bunch Clock and Beam

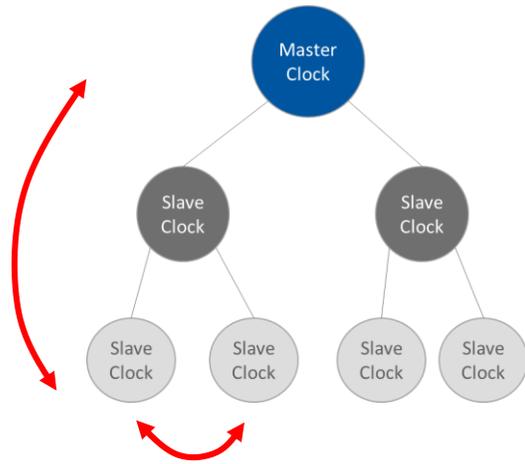


⇒ Reduce WANDER due to environment variations

- limit temperature variations
- measure and compensate propagation time



Orders of Magnitude for LHC experiments

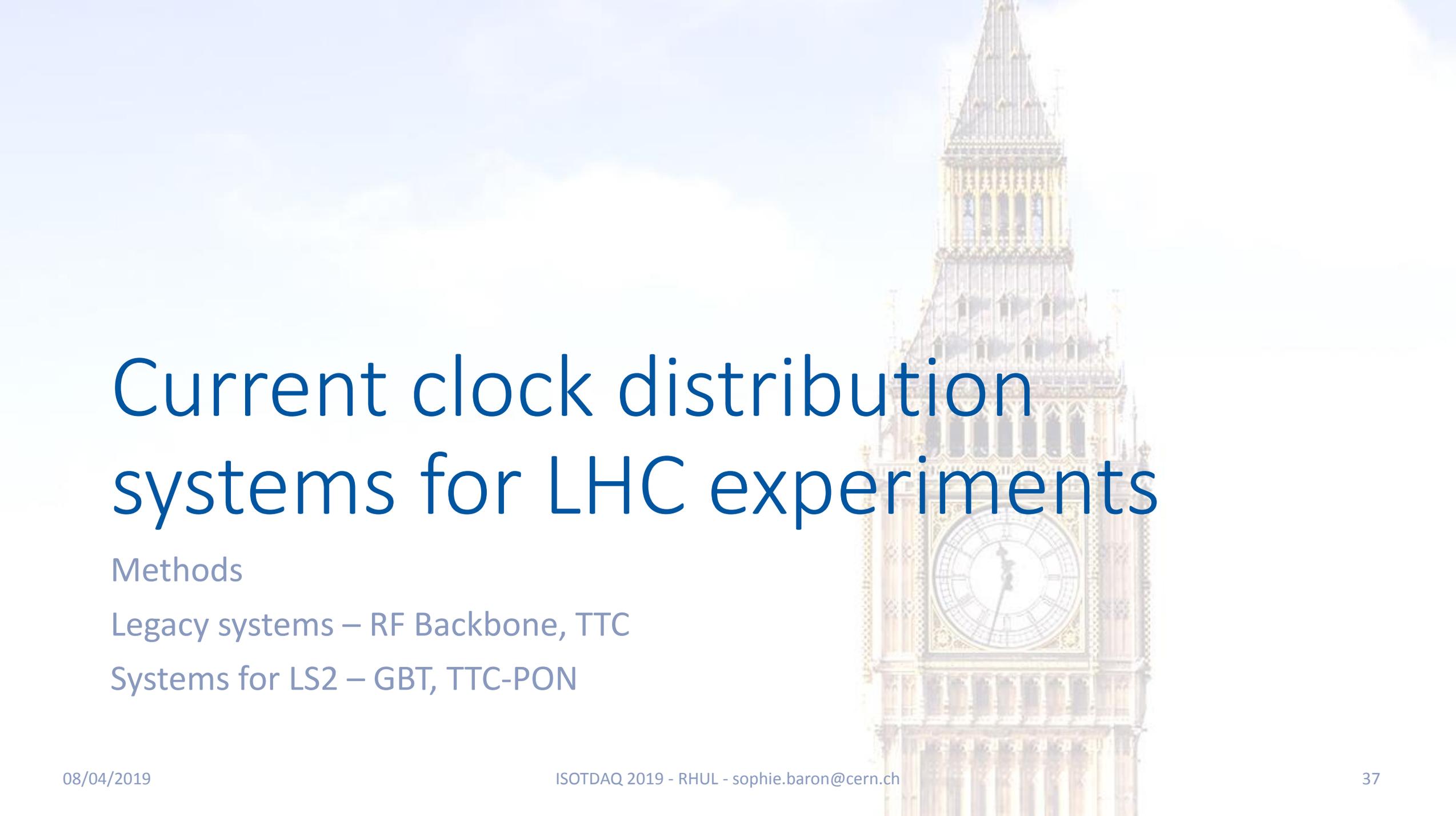


$$\begin{aligned} TIE_{BC} &\approx 50 \text{ ps rms}^{(1)*} \\ TIE_{Ch-Ch} &\approx 1 \text{ ns rms}^{(2)*} \end{aligned}$$

*A posteriori requirements for LHC detectors. Specific run conditions of 2017-2018 were challenging these values.

(1): the Bunch Clock at the RF is close to a perfect clock <1ps rms

(2): maximum channel-to-channel skew jitter between 2 nodes in the detector



Current clock distribution systems for LHC experiments

Methods

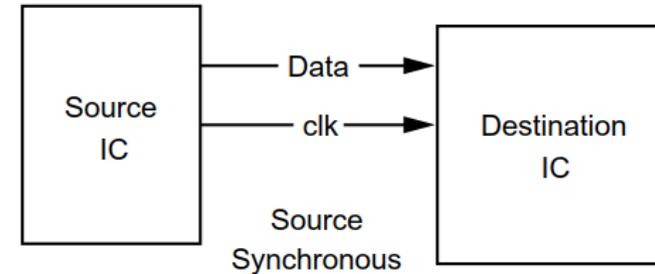
Legacy systems – RF Backbone, TTC

Systems for LS2 – GBT, TTC-PON

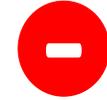
Synchronization methods

- **Source synchronous** systems

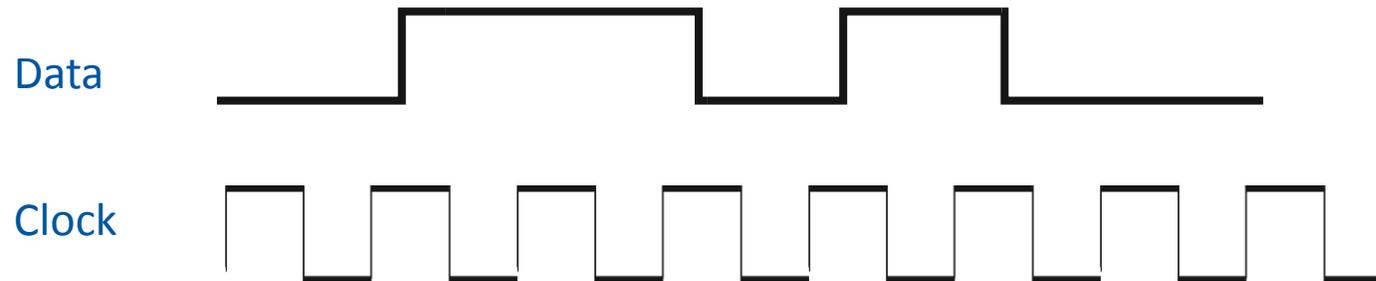
- a copy of the clock is sent along with the data (trigger for example)
- The output of the forwarded clock is adjusted so that the clock transitions in the middle of the data cell. (clock domain crossing)



Clock goes straight and is really clean



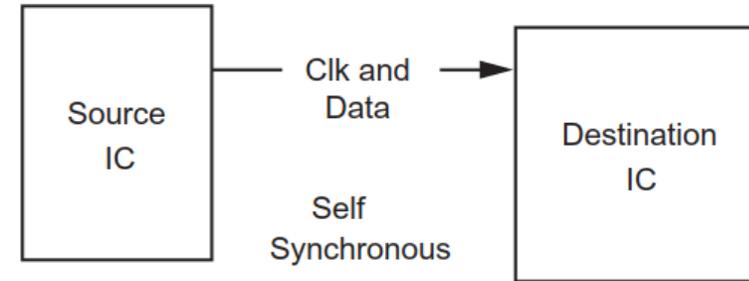
2 links, data/clock retiming at Rx



Synchronization methods

- **Self-synchronous** systems

- the data stream contains both the data and the clock.



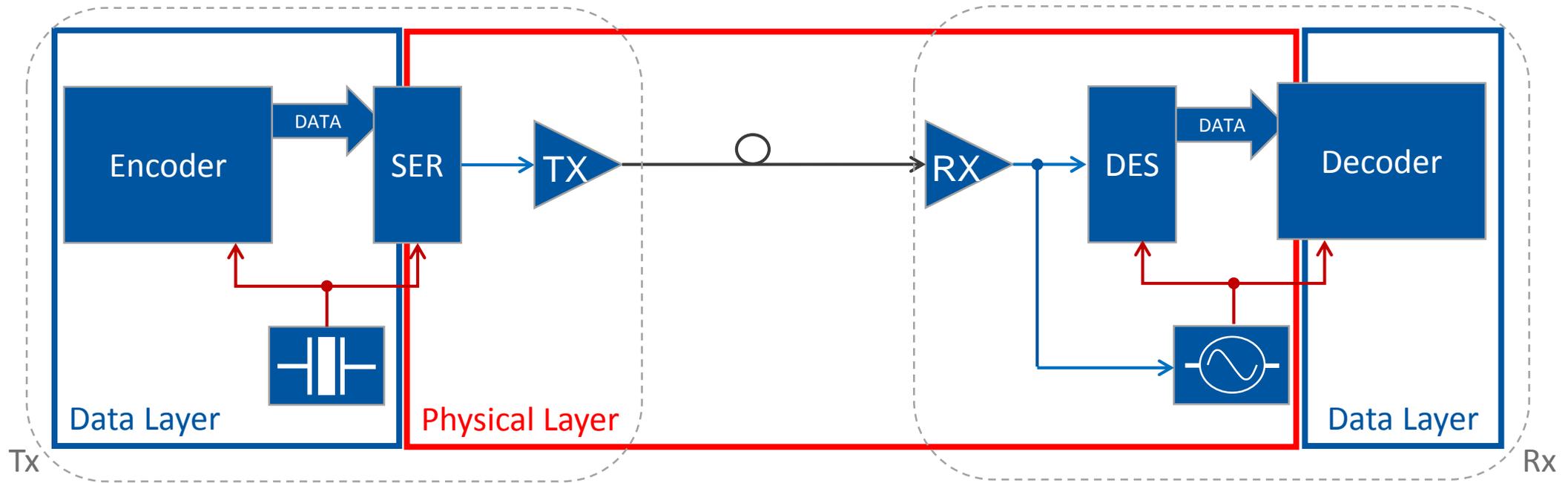
+ No retiming at Rx, 1 link

- Clock recovery not simple at Rx

Data



Self synchronous systems



- Physical Interface (LVDS, CML..)
- Modulation Schemes (NRZ, PAM4 ...)
- Clock and Data Recovery (CDR)
- Signal Integrity Considerations,
- Pre-Emphasis, Equalization

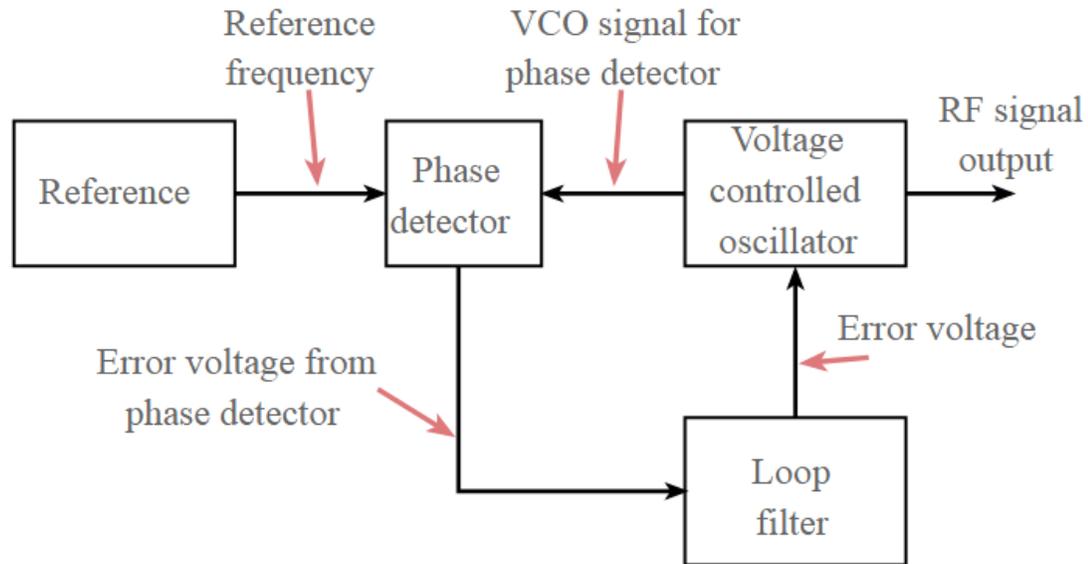
- Encoding/Scrambling
- Frame Alignment
- Comma Detection
- Error Correction schemes
- Clock Domain Crossing

Self synchronous systems

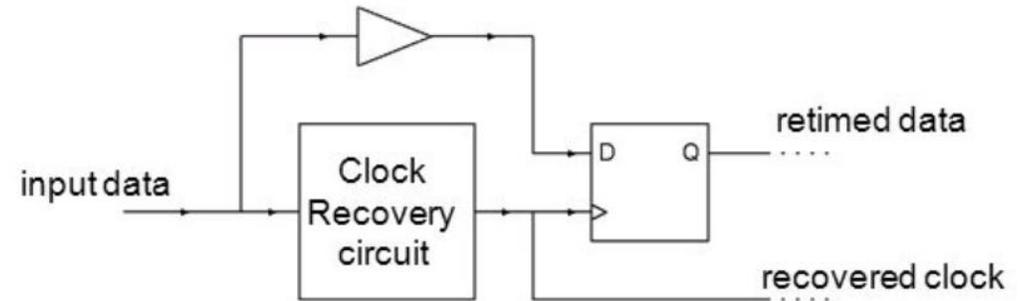


Phase Locked Loops & Clock and Data Recovery...THE keys of self-synchronous systems

(aka PLL) (aka CDR)

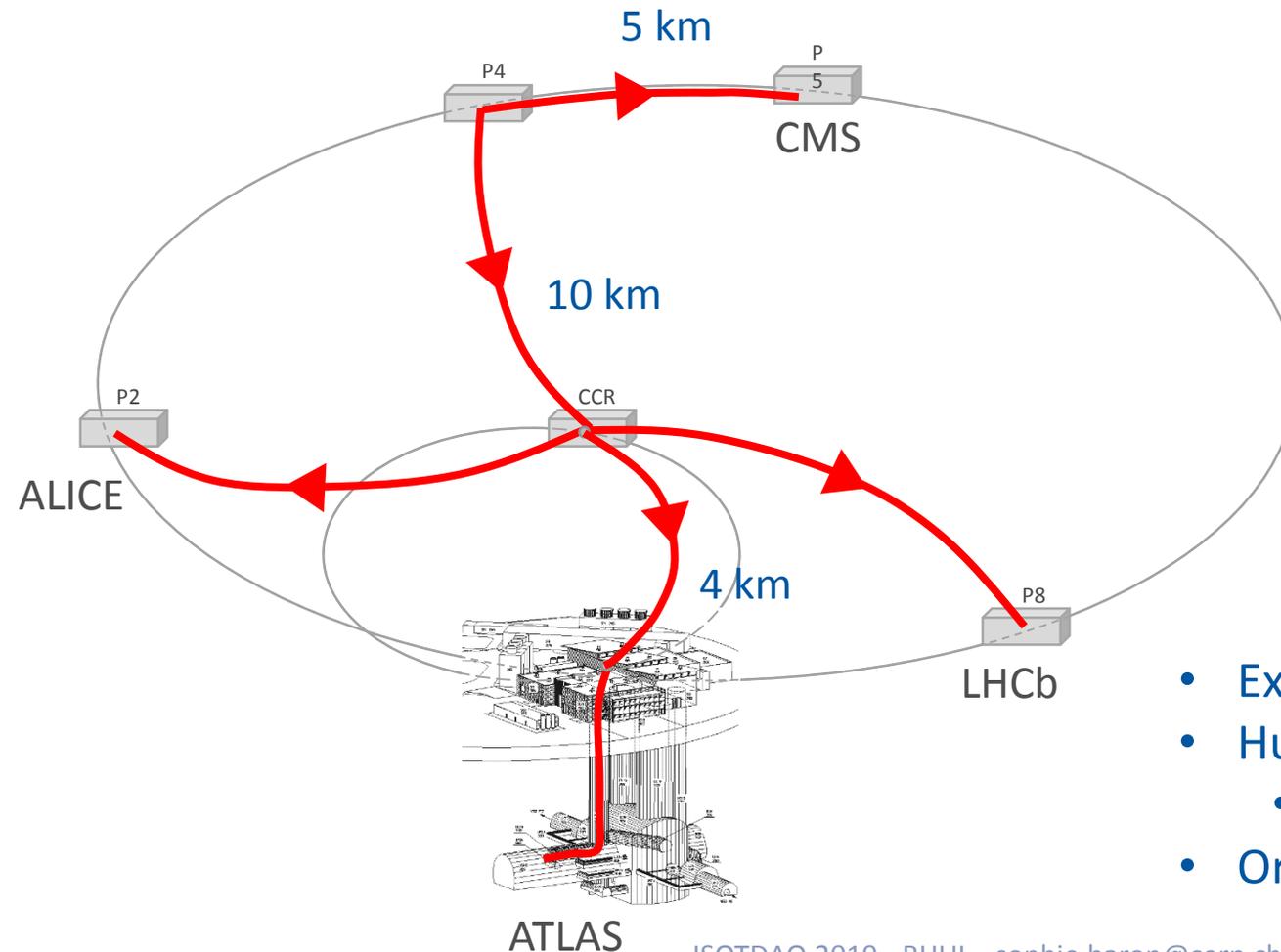


Phase locked loop diagram showing voltages



From the LHC-RF to the experiments

- The “RF Backbone”
- **Source synchronous** for a purer clock quality & compatibility with RF needs

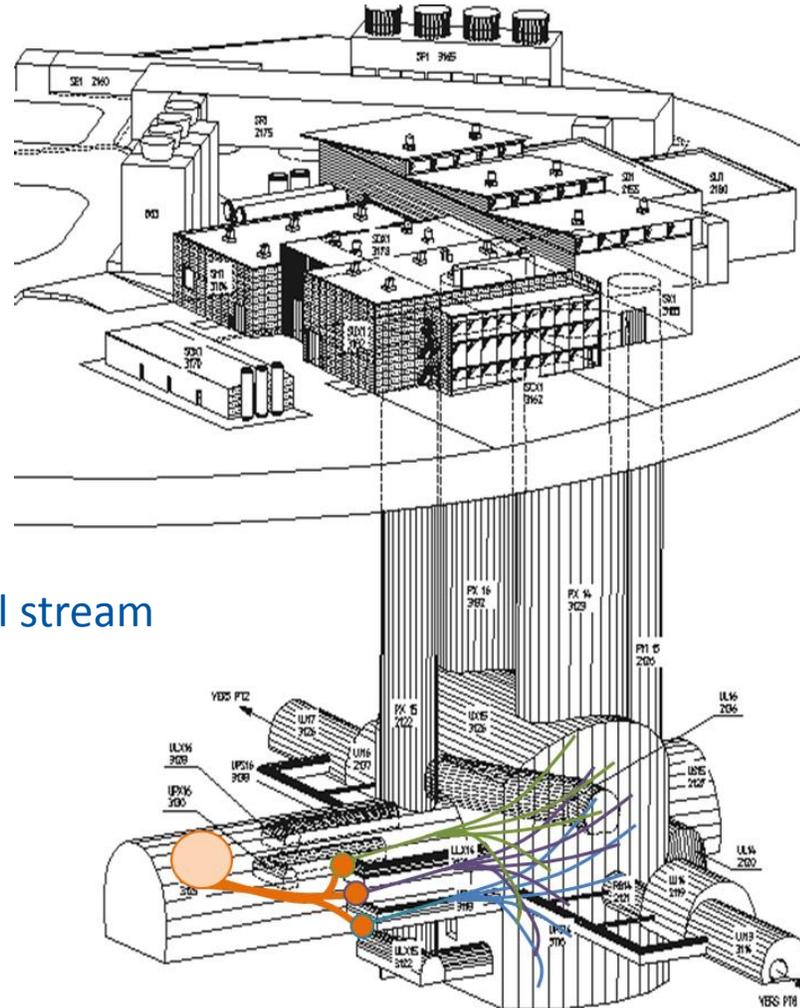


- 2 Bunch Clocks (beam 1 & 2)
- 2 Orbit signals (beam 1 & 2) = ‘data’

...sent over **4 parallel optical fibers**

- Excellent BC quality at Rx (~ 2 ps rms)
- Huge wander (up to 8ns seasonal drift)
 - Phase adjusted wrt beam at experiments
- Orbits need to be resynchronized at Rx

And in the experiments...mostly self-synchronous ...so far

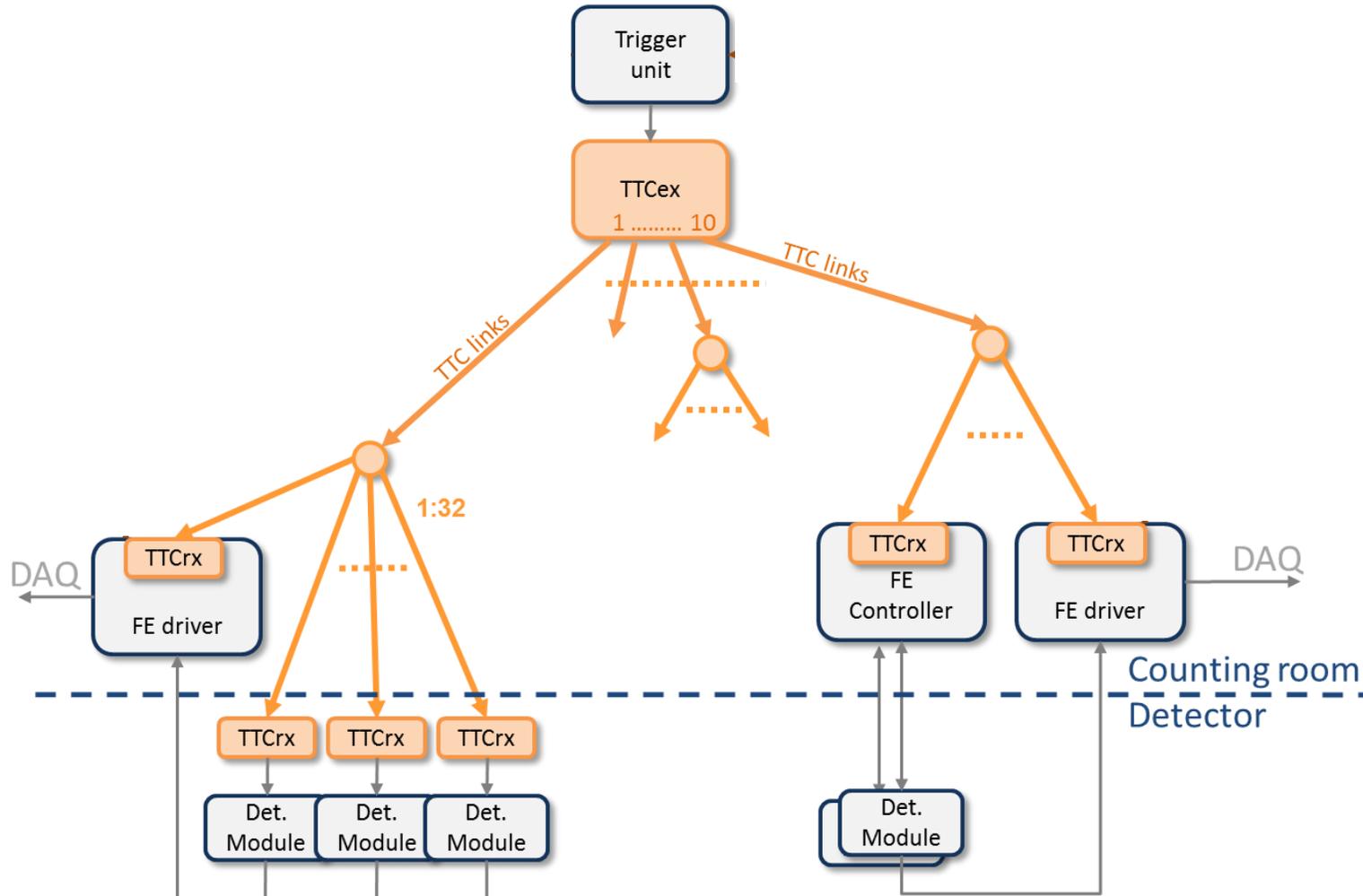


Self Synchronous systems:
Clock and data are embedded in a serial stream

Some examples ...

TTC

Timing Trigger & Control



- 1997-2007
- Self Synchronous
- Optical, Unidirectional
- Carrier Clock: LHC BC (40.079MHz)
- Data:
 - Fixed latency:
 - level-1 trigger
 - Low latency
 - Orbit
 - bunch and event numbers
 - test signals
 - broadcast commands
- Receiver in radiation area
 - Specific ASICs for CDR
 - TTCrx
 - QPLL

TTC

- Physical layer:

- Time Domain Multiplexing of A & B channels
- Bi-phase Mark encoding
- 160Mbps line rate

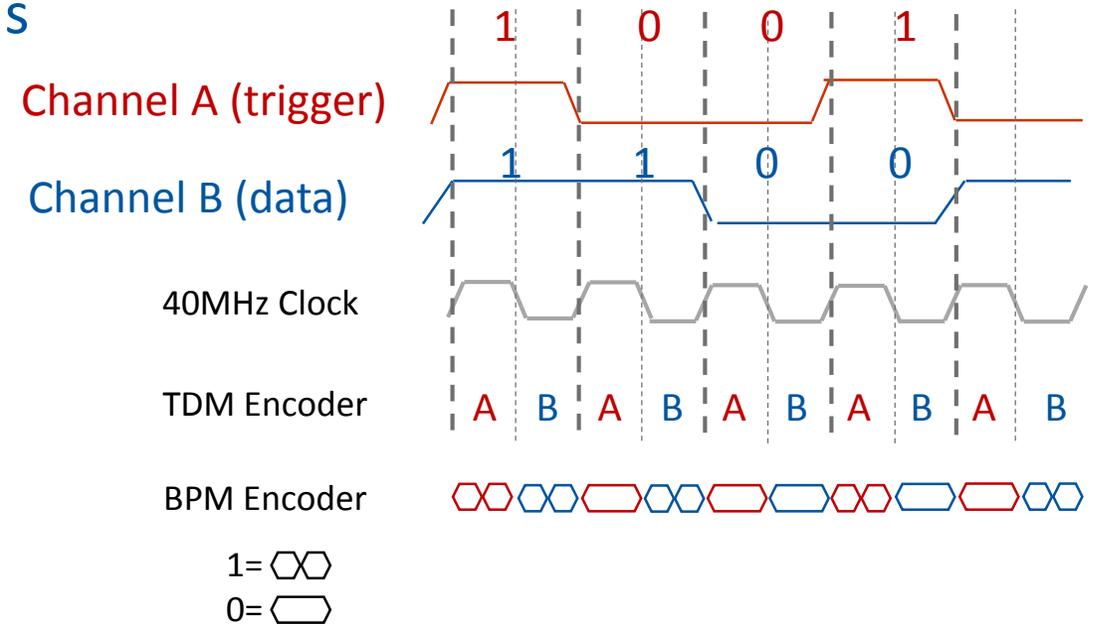
- Data Layer - Protocol:

- A Channel (40Mbps):

- Broadcasting ONLY L1a Trigger (1 bit signal)
- Low & fixed latency (1 bit per BC period)
- Not protected

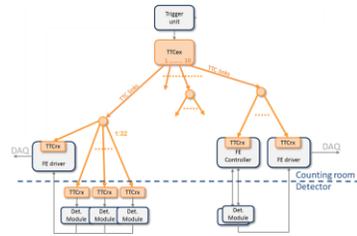
- B Channel

- Framed & formatted commands and data
- Redundancy for error correction & detection
- Hamming code (1 bit error correction, 2 bits error detection)

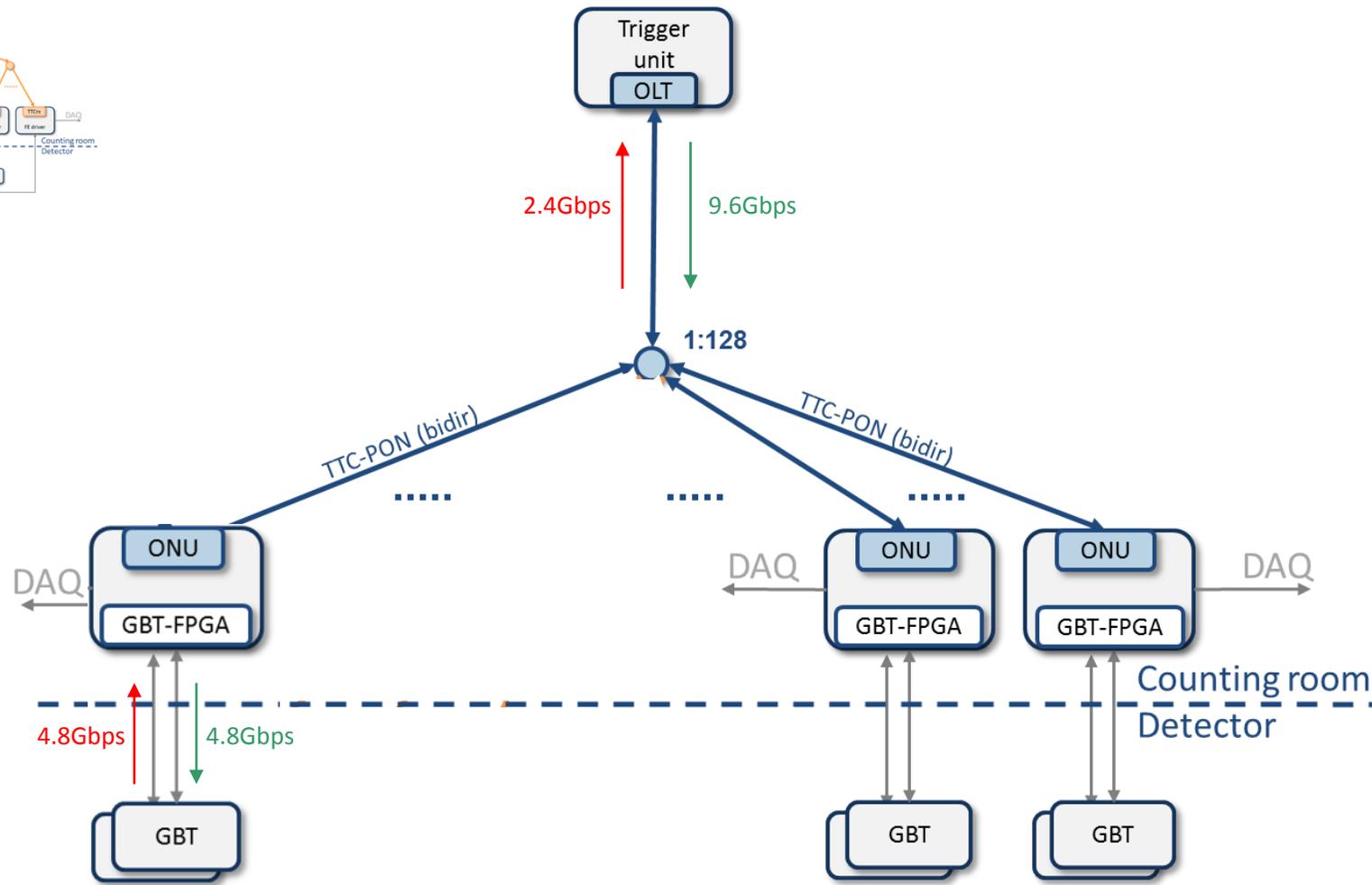


- + Good Clock jitter ~ 10 ps rms
- Narrow locking range (sometimes unlocks during ramp)
- Strong wander due to temperature variations
- Jitter sensitive to data payload

GBT & TTC-PON (commissioning LS2)



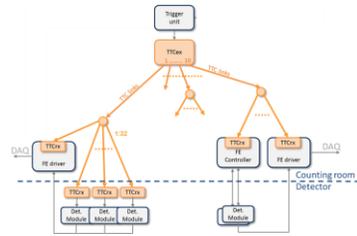
Replacing TTC



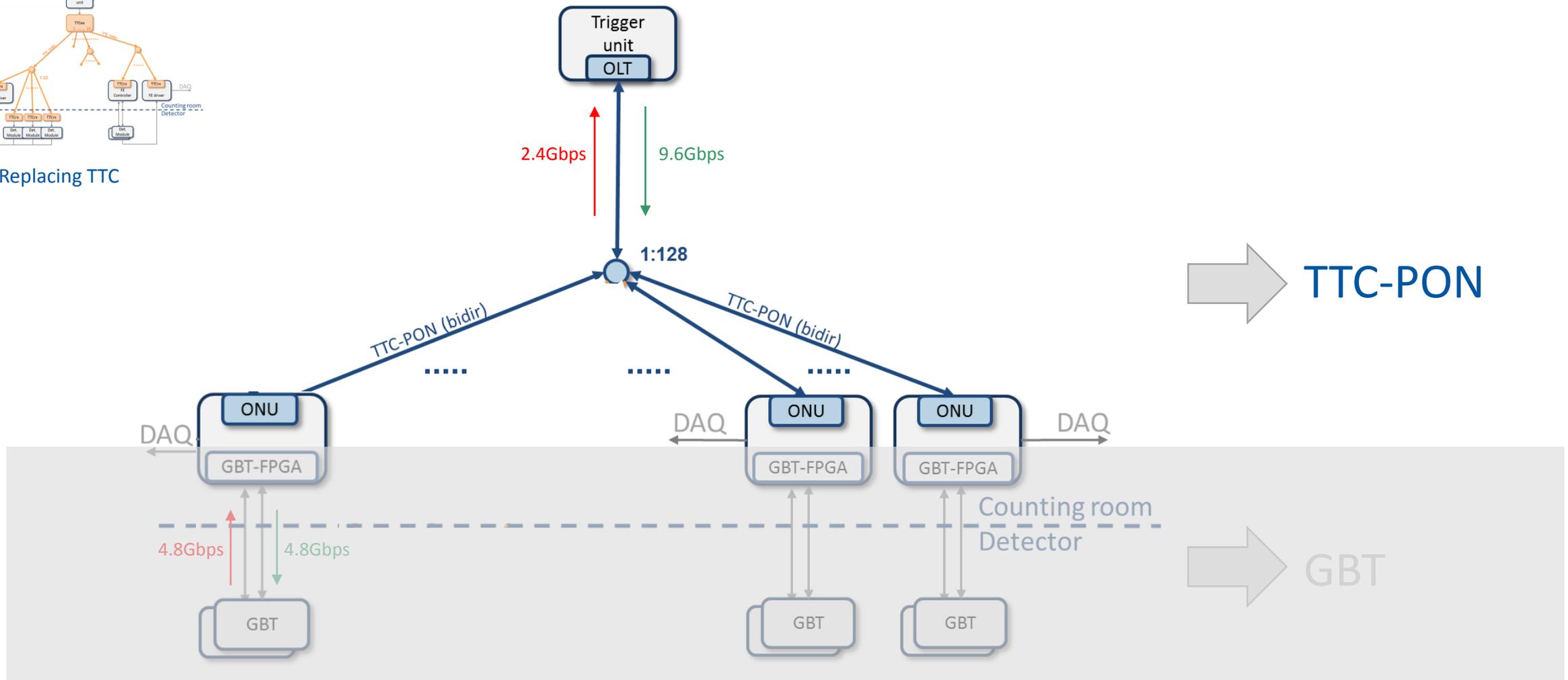
➔ TTC-PON

➔ GBT

GBT & TTC-PON (commissioning LS2)

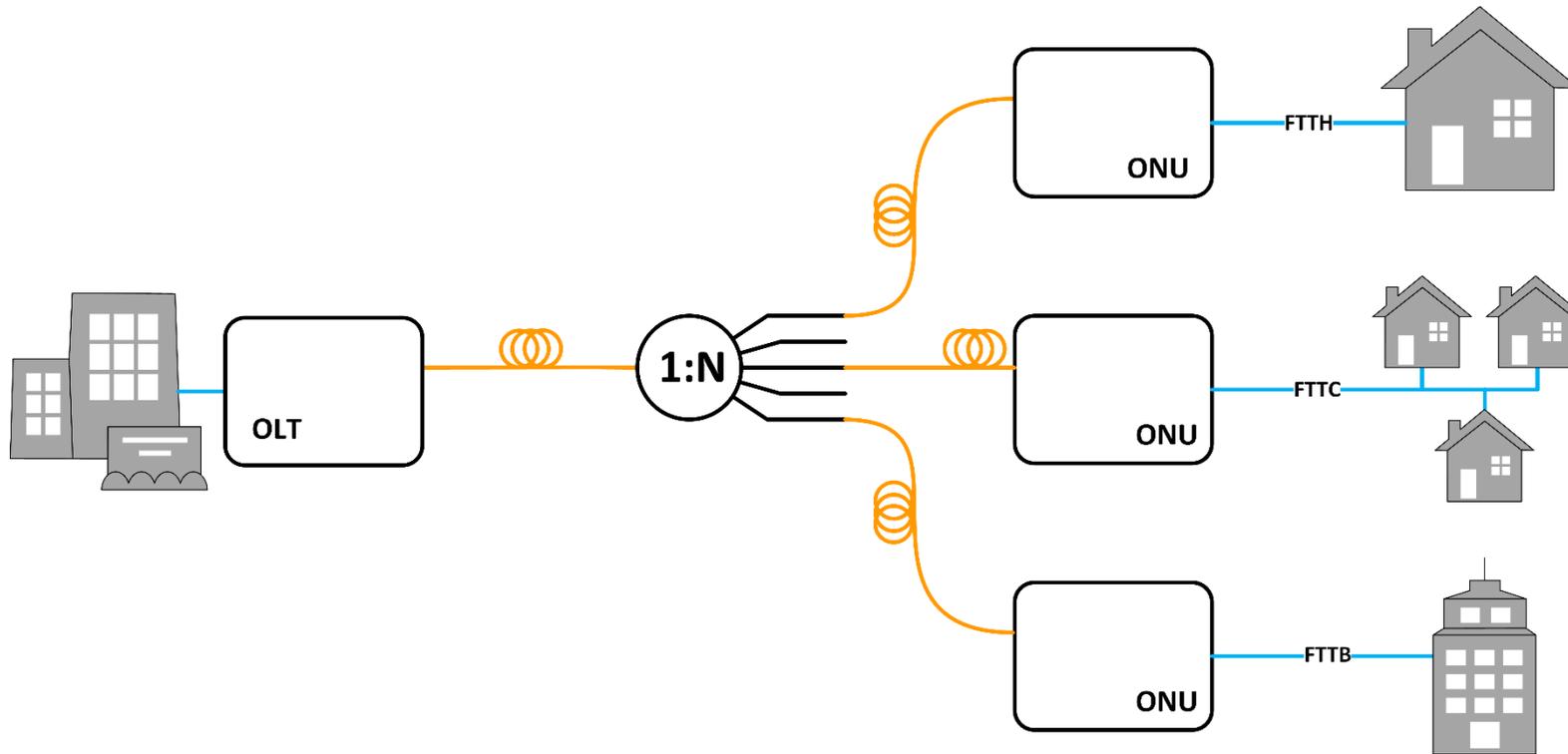


Replacing TTC



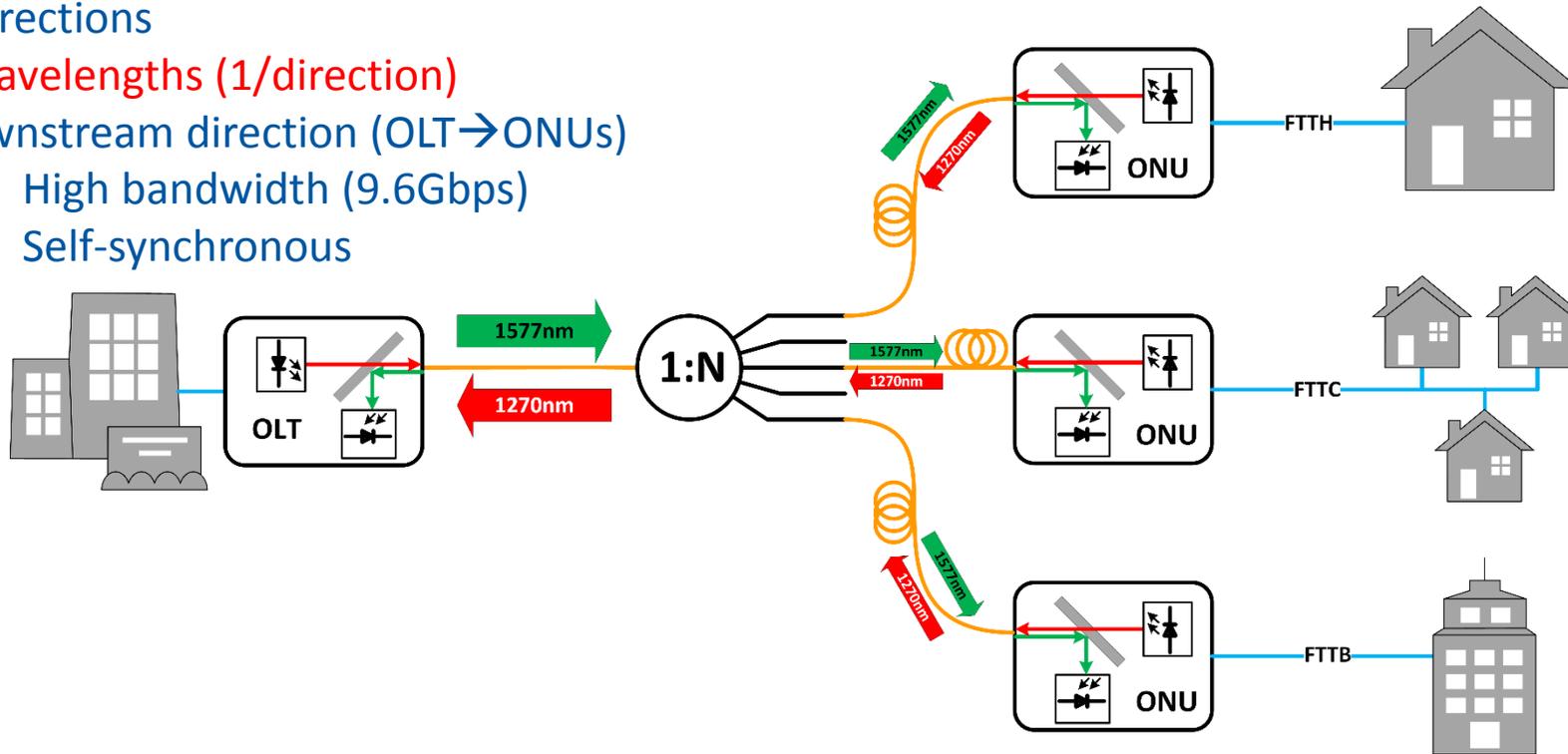
TTC-PON

- **PON**: Passive Optical Network
- **FTTH**: Fiber To The Home
- Single fiber



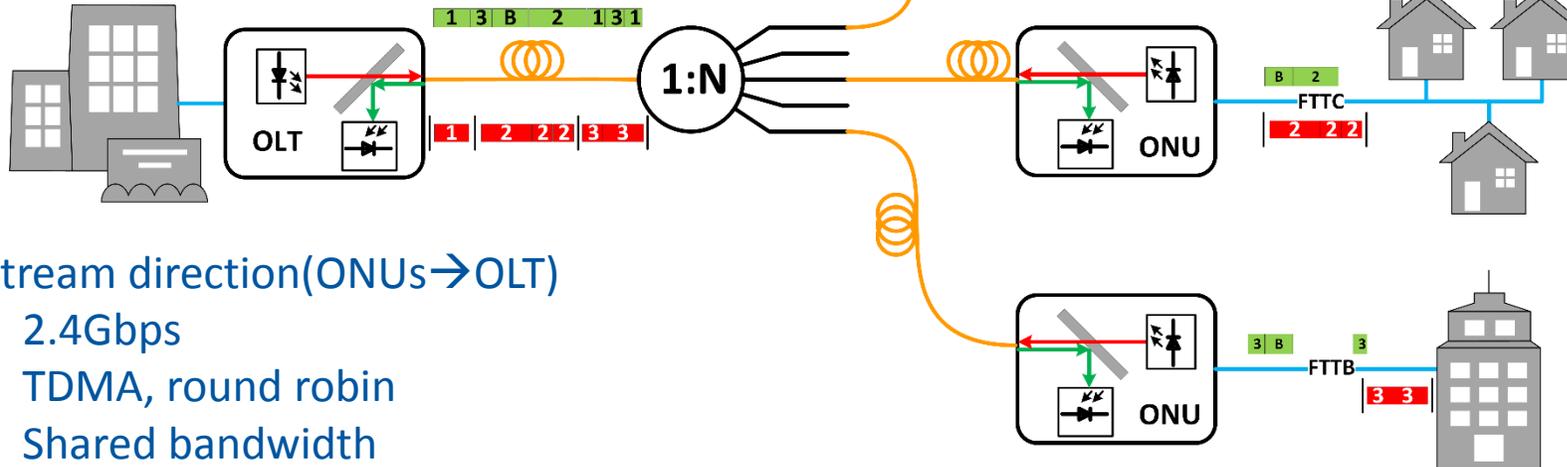
TTC-PON

- **PON**: Passive Optical Network
- **FTTH**: Fiber To The Home
- Single fiber
- 2 directions
- 2 wavelengths (1/direction)
- Downstream direction (OLT→ONUs)
 - High bandwidth (9.6Gbps)
 - Self-synchronous



TTC-PON

- **PON**: Passive Optical Network
- **FTTH**: Fiber To The Home
- Single fiber
- 2 directions
- **2 wavelengths (1/direction)**
- Downstream direction (OLT→ONUs)
 - High bandwidth (9.6Gbps)
 - Self-synchronous



- Upstream direction(ONUs→OLT)
 - 2.4Gbps
 - TDMA, round robin
 - Shared bandwidth
 - Synchronized to Bunch Clock



TTC-PON

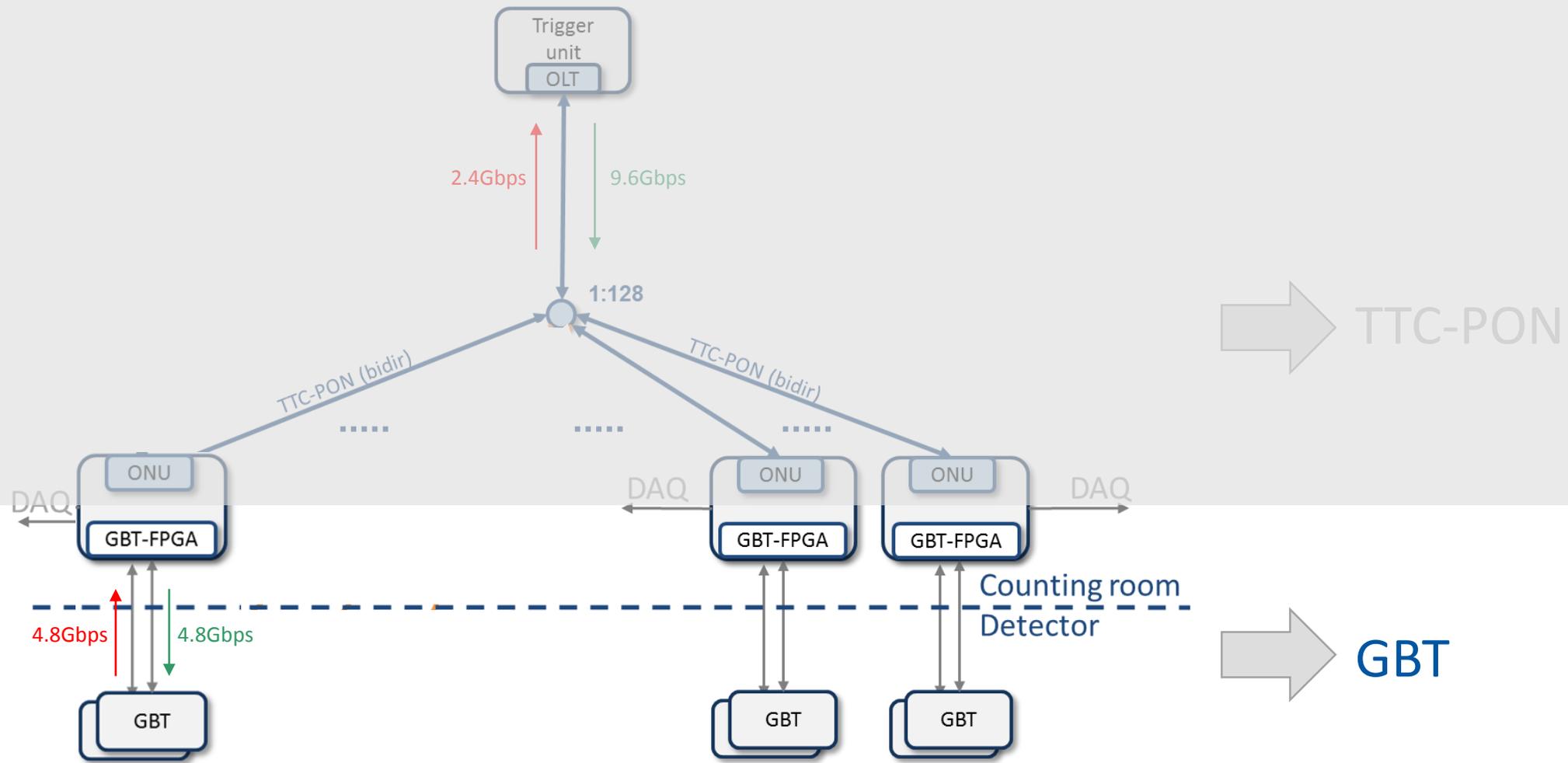
- Deliverables:

- XG-PON optical modules (COTS)
- Python based control software
 - Control field reserved in the PON frame
- Sophisticated VHDL IP blocks
 - Implementing PON protocol and system calibration/monitoring tools
 - Providing fixed and deterministic phase and latency
 - Both for clock and data
 - Interfacing easily to GBT
- Hardware reference design
 - Using the Si5344/45 PLL family to clean recovered clock out of the FPGA
 - Extremely good and fixed phase!

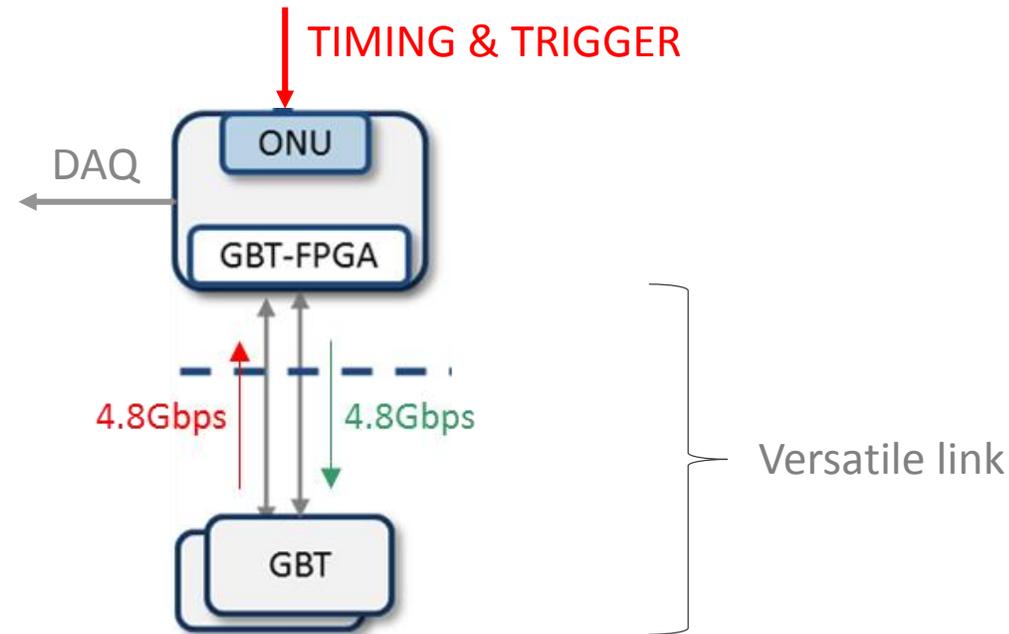


- + Super low clock jitter ~ 2 ps rms
- + Insensitive to payload
- + limited wander / to temperature variation

GBT & TTC-PON (commissioning LS2)



GBT



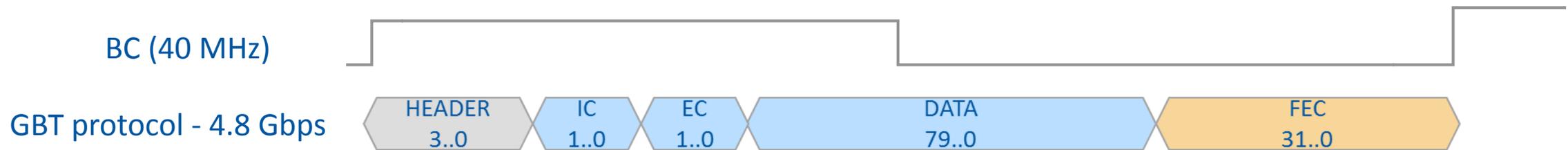
- Self-synchronous
- 4.48 Gb/s optical links, synchronized to Bunch Clock
- Timing and Trigger downstream, Data Acquisition (DAQ) upstream + Slow Control
- Point-to-point, optical, bidirectional (two fibres), constant latency
 - Back-end: HDL IP core implementing specific GBT protocol (GBT-FPGA)
 - Front-end: custom designed Rad-hard chipset (GBTx, GBT-SCA, LpGBT, GBTIA...) – 50 MRad

GBT

- GBT protocol

- Strong Forward Error Correction (FEC)

- 32 bits of redundancy for 84 bits of payload data (total of 120 bits per frame @ 40.079MHz)
 - Correction of up to 16 wrong consecutive bits
 - 3.32 Gb/s user payload downstream
 - FEC can be disabled upstream to increase bandwidth (widebus mode)

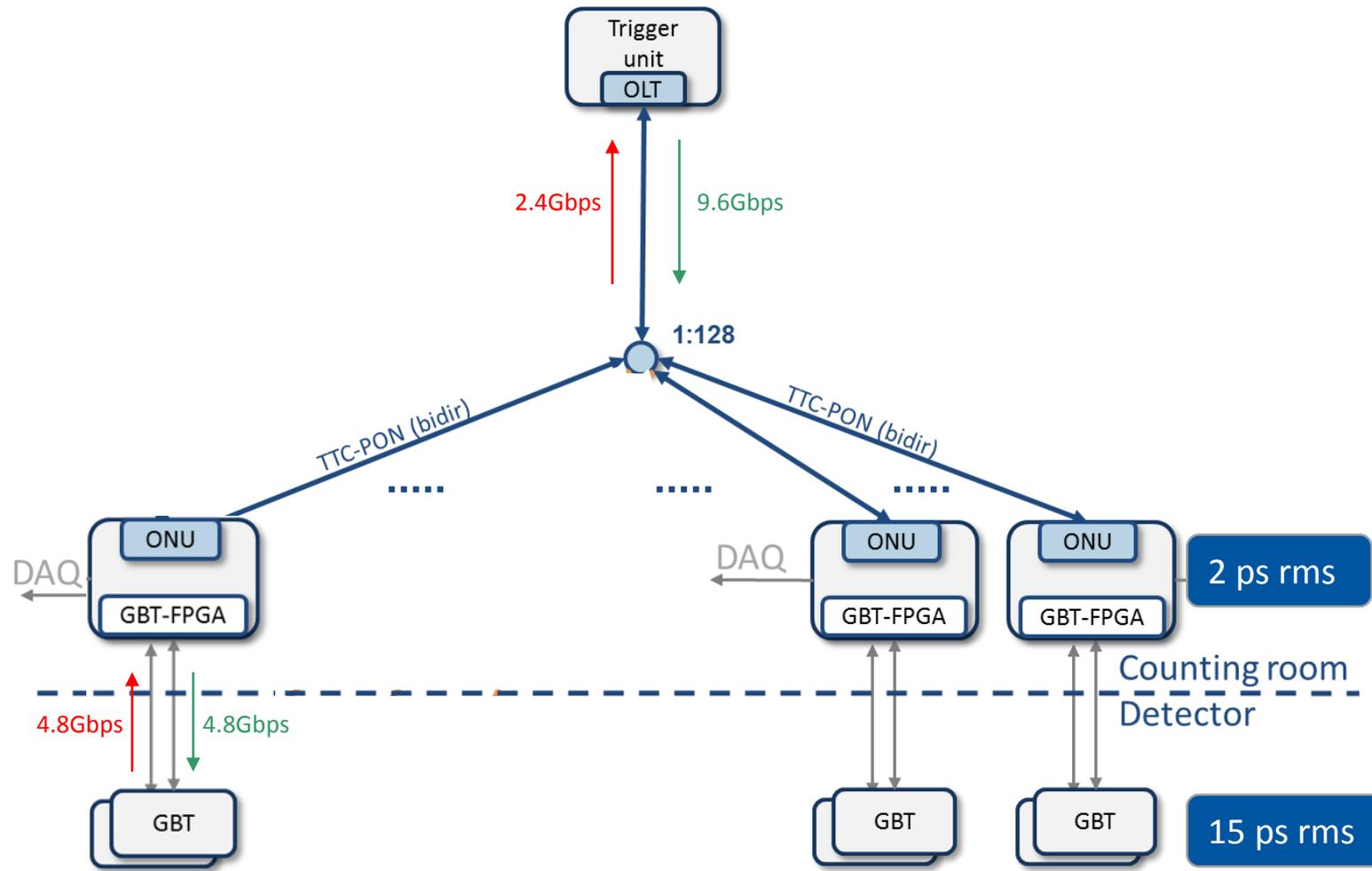


- Fixed and Low latency

- Clock & data recovered at fixed phase/latency
 - Very specific requirement
 - Not common in commercial world

+ Clock jitter ~ 15 ps rms
+ independent from payload
+ limited wander / temperature variation

GBT & PON – TIE Jitter



Ok for LHC, but ...

Challenges for HL-LHC

Focussing on detector

New needs for HL-LHC

CMS 200PU HL-LHC Event:

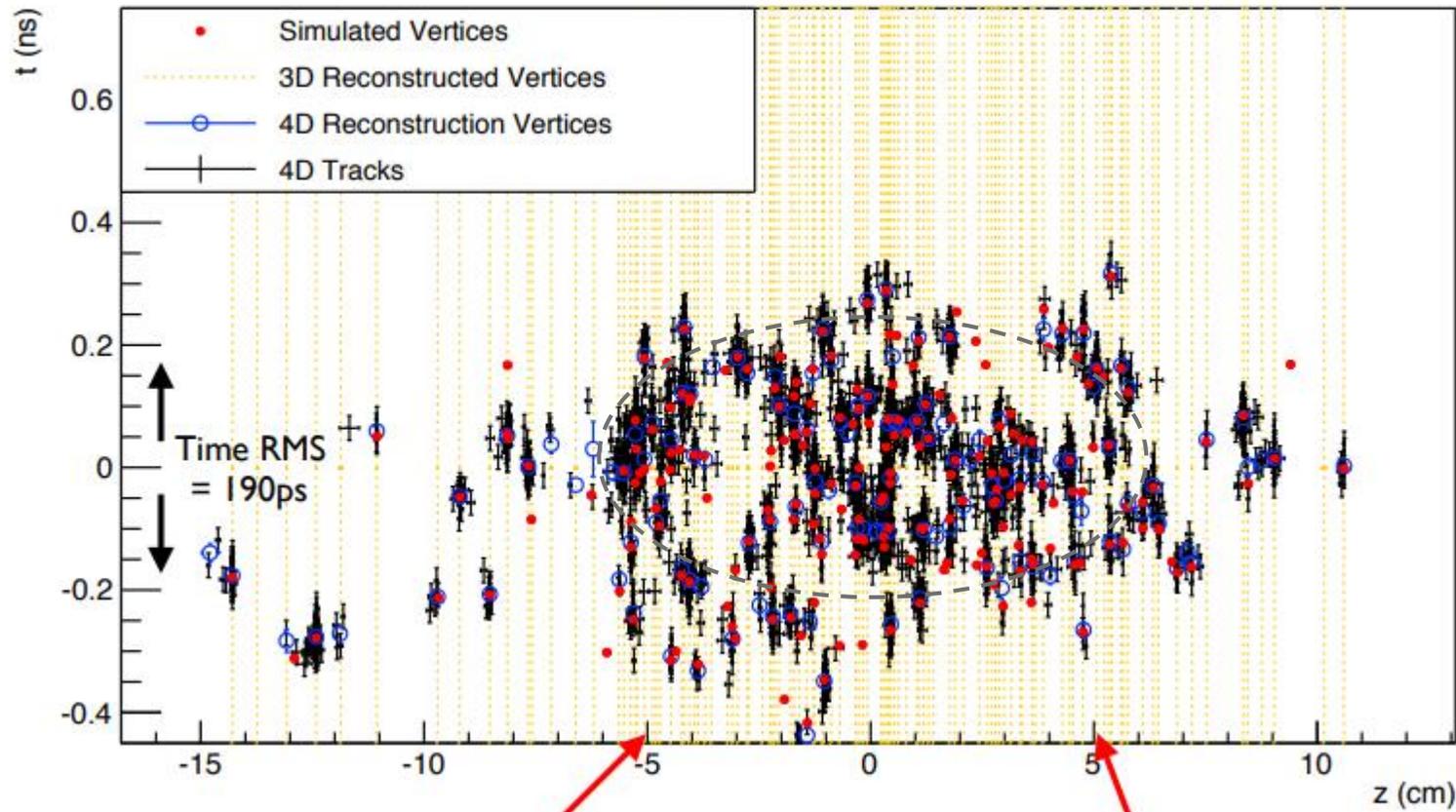


Courtesy Lindsey Gray, FNAL

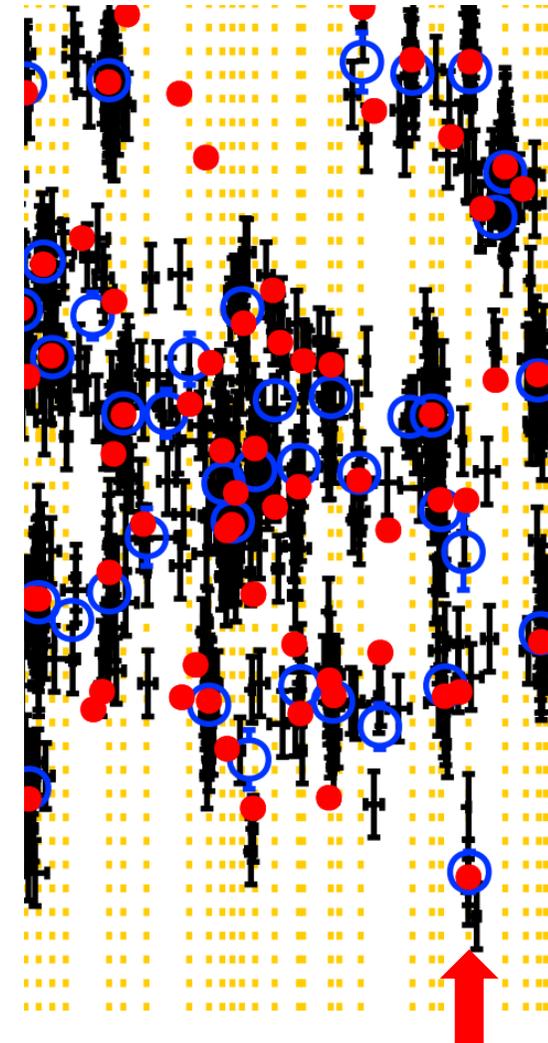
Ultimate HL-LHC luminosity target is now 7.5×10^{34} Hz/cm² = 200 Pile Up events

High Precision Timing to fight Pile Up

- High Precision Timing allows time separation of Interaction vertices



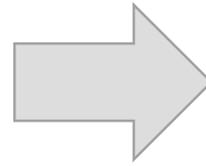
Courtesy Lindsey Gray, FNAL



Get prepared for new requirements...

LHC Initial needs

- $TIE_{BC} \approx 50$ ps rms
- $TIE_{Ch-Ch} \approx 1$ ns rms



HL-LHC requirements

- $TIE_{BC} \approx 10$ ps rms
- $TIE_{Ch-Ch} \approx 30$ ps rms
- And more radiations...
- And more bandwidth...
(and more troubles)

Backbone...towards a new paradigm: white Rabbit

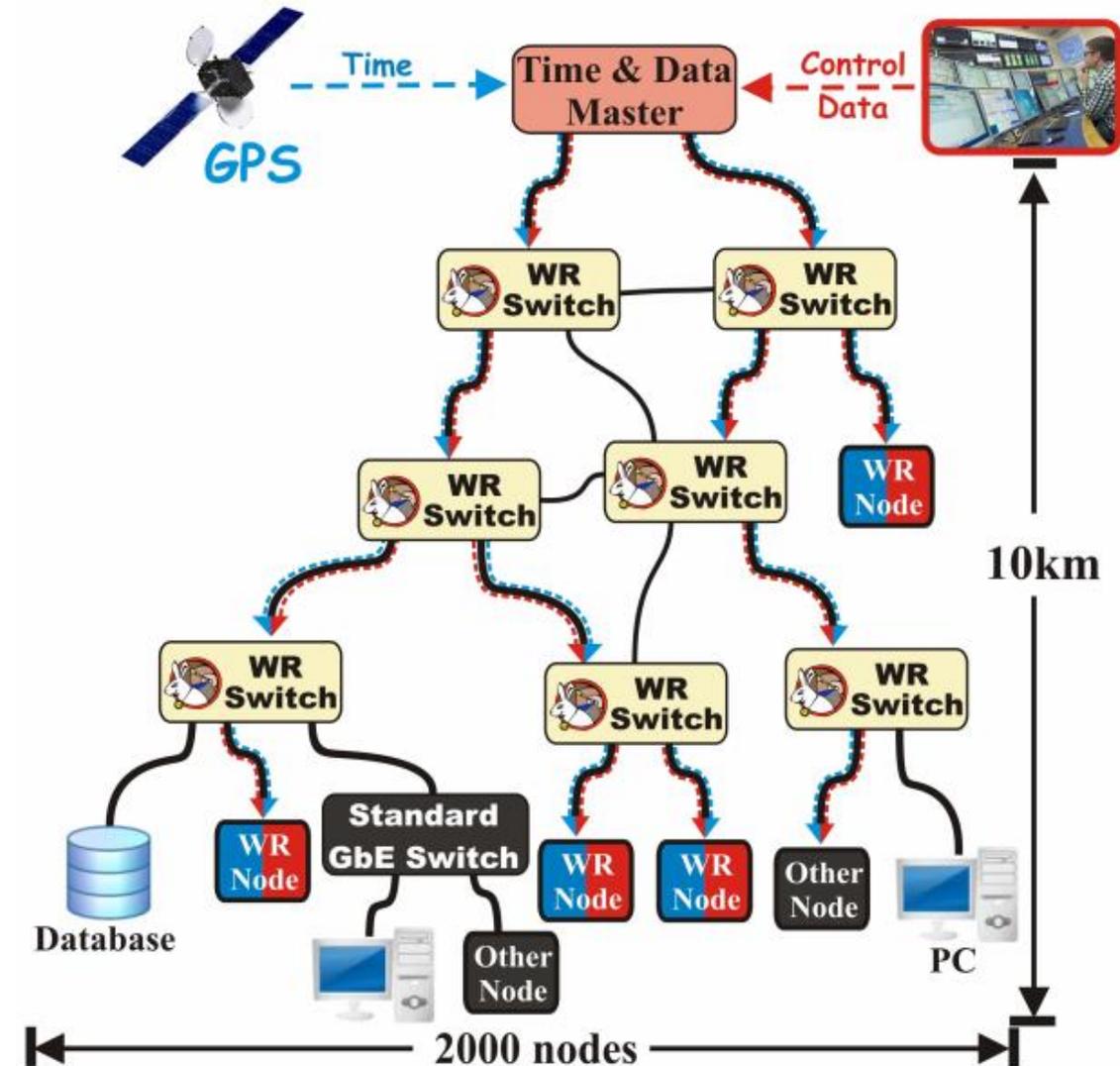


- Don't distribute the Bunch Clock itself anymore...
- But distribute
 - The information to reconstruct it at each end node
 - Frequency and phase variation
 - With a fixed & controlled latency

Backbone...towards a new paradigm

- Innovative concept
 - Self synchronous Standard Ethernet network
 - Future part of PTP standard
 - IEEE1588-2018 (High Accuracy)
- High accuracy synchronisation to the GPS time
 - Precise GPS distribution
 - Precise round trip measurement & compensation
 - Wander ~ 0 , even over 10km
 - Bounded and low-latency Control Data

+ specific hardware modules to recreate the Bunch clock



On detectors: LpGBT



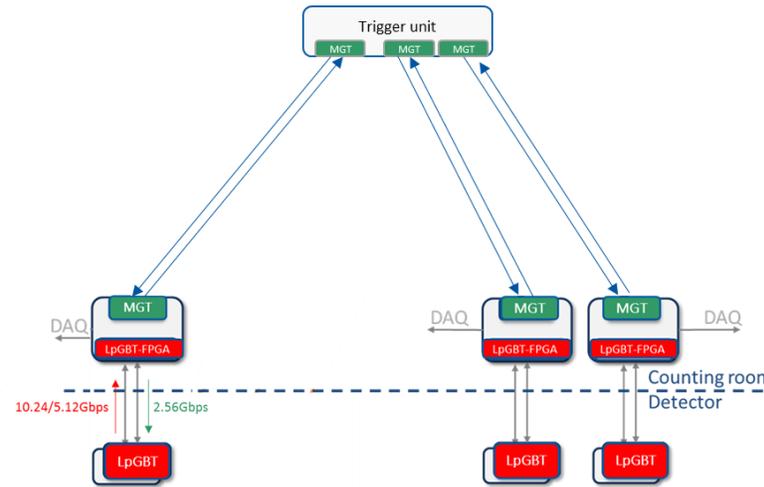
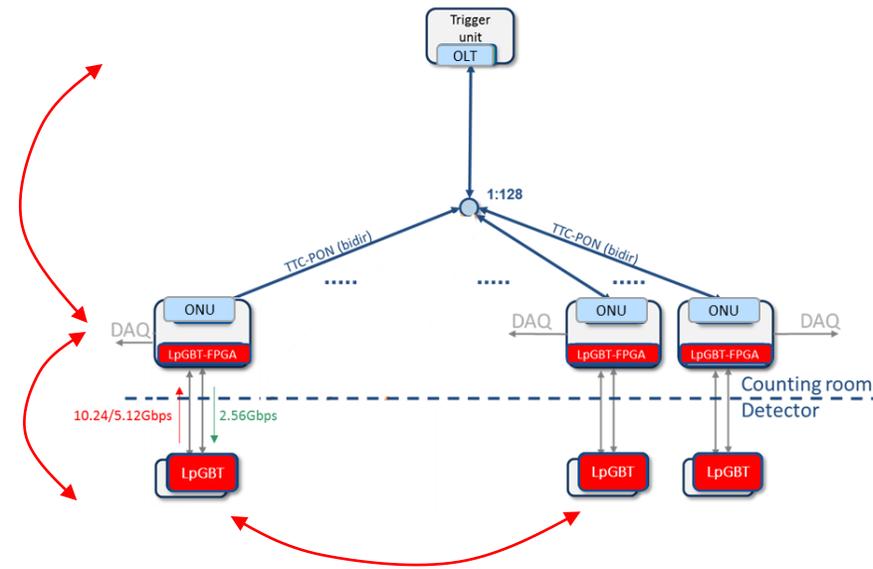
- New custom ASIC:
 - First proto taped out and validated
- Lower Power 500mW/750mW (5.12/10.24Gbps)
- Higher radiation hardness – TID 200 Mrad
- Lower jitter <5ps rms
- Higher upstream bandwidth (10.24Gbps)
- ...and much more in the specs!

<https://espace.cern.ch/GBT-Project/LpGBT/>

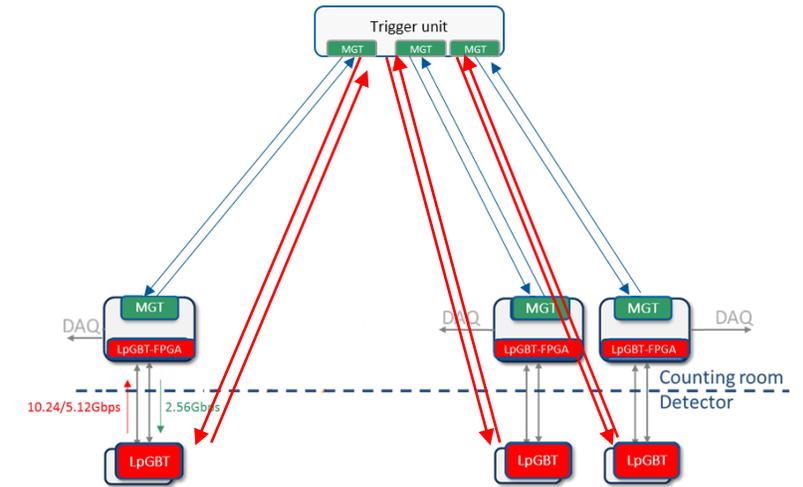
...and High Precision Timing



Self-synchronous?



Source Synchronous?



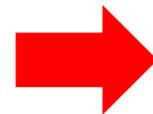
Ensuring low jitter and low wander between master-slave and slave-slave is a challenge for each layer

- Extreme care on link design
- Precise round trip measurement and/or compensation

All experiments are collaborating on this challenging topic...



<https://espace.cern.ch/HighPrecisionTiming>



Join our interest group if you want to know more
About the challenges we are facing!

HPTD-interest-group@cern.ch

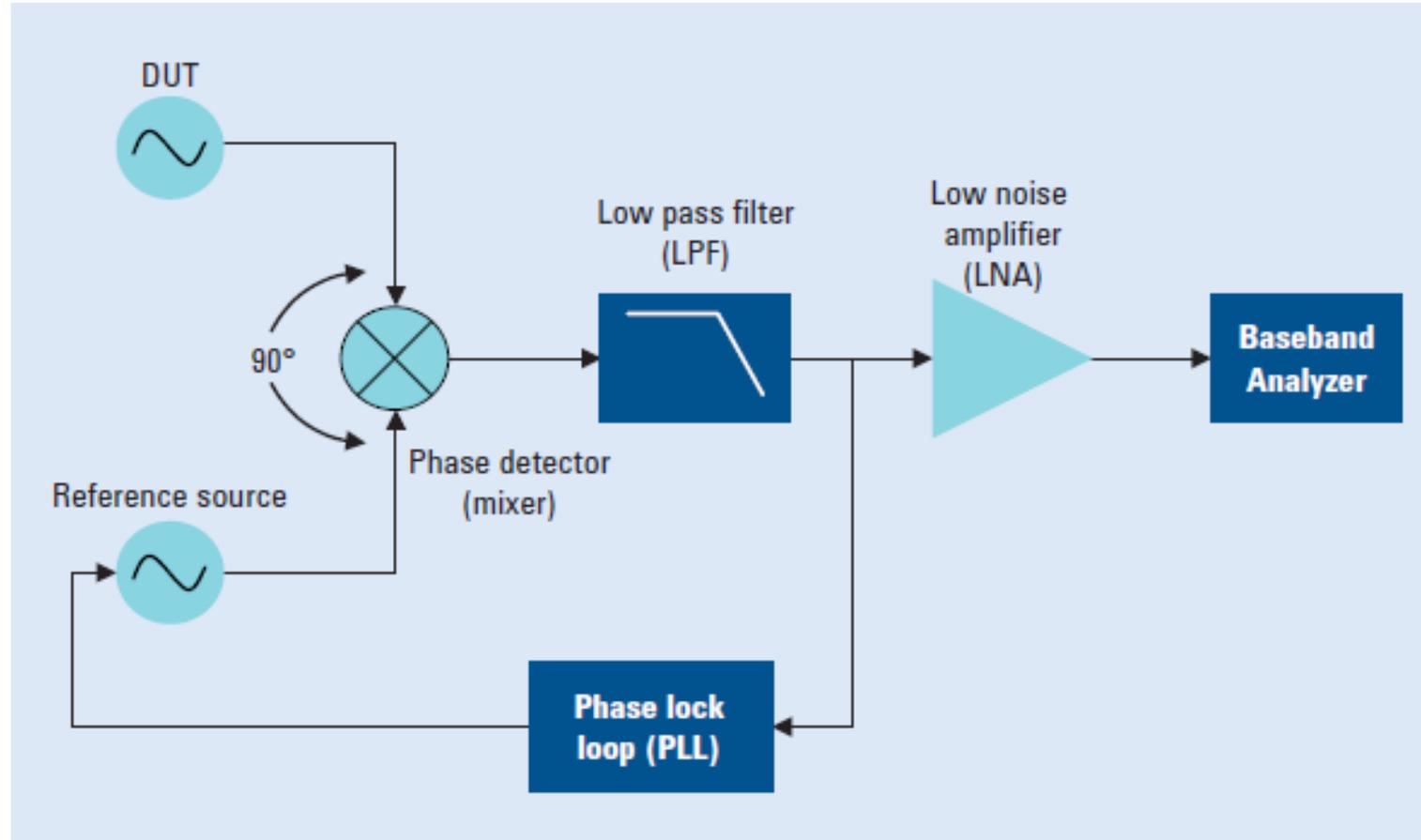
Thanks!



Spare slides

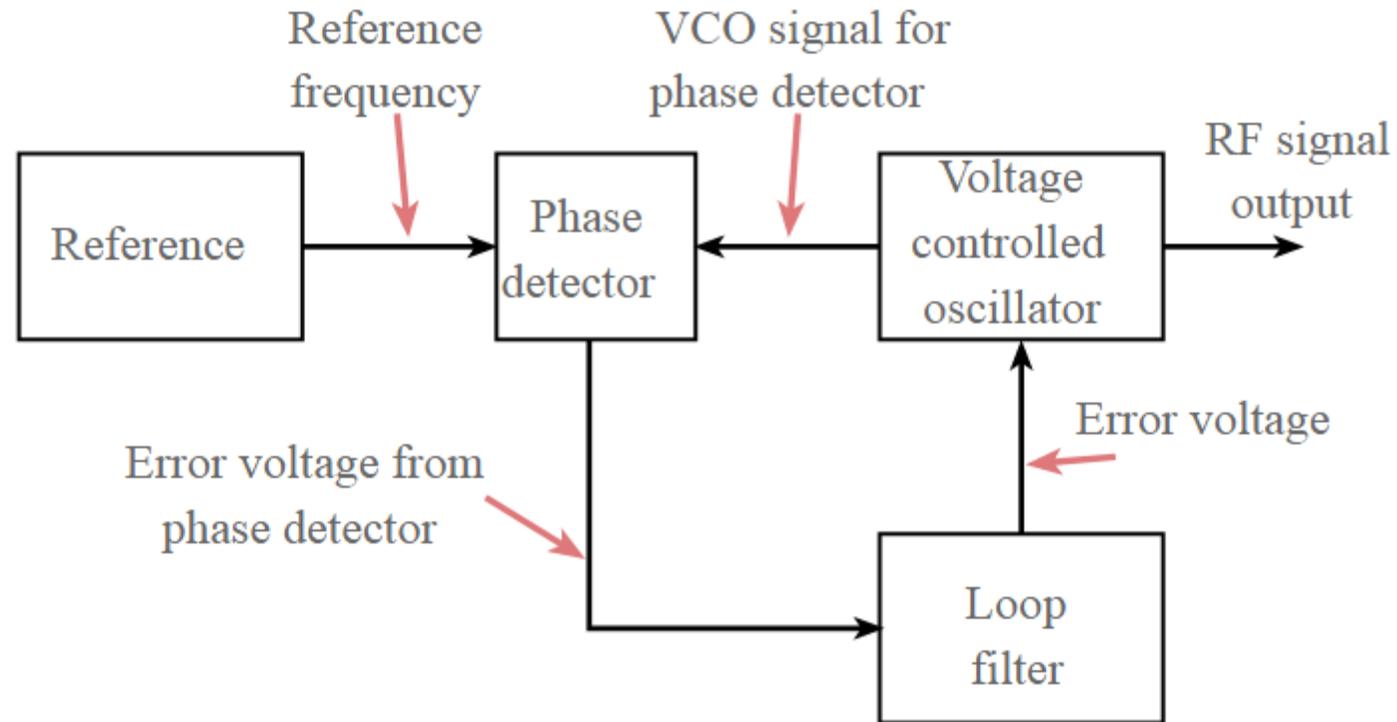


Phase Noise measurement



E5052B SSA Signal Source Analyzer

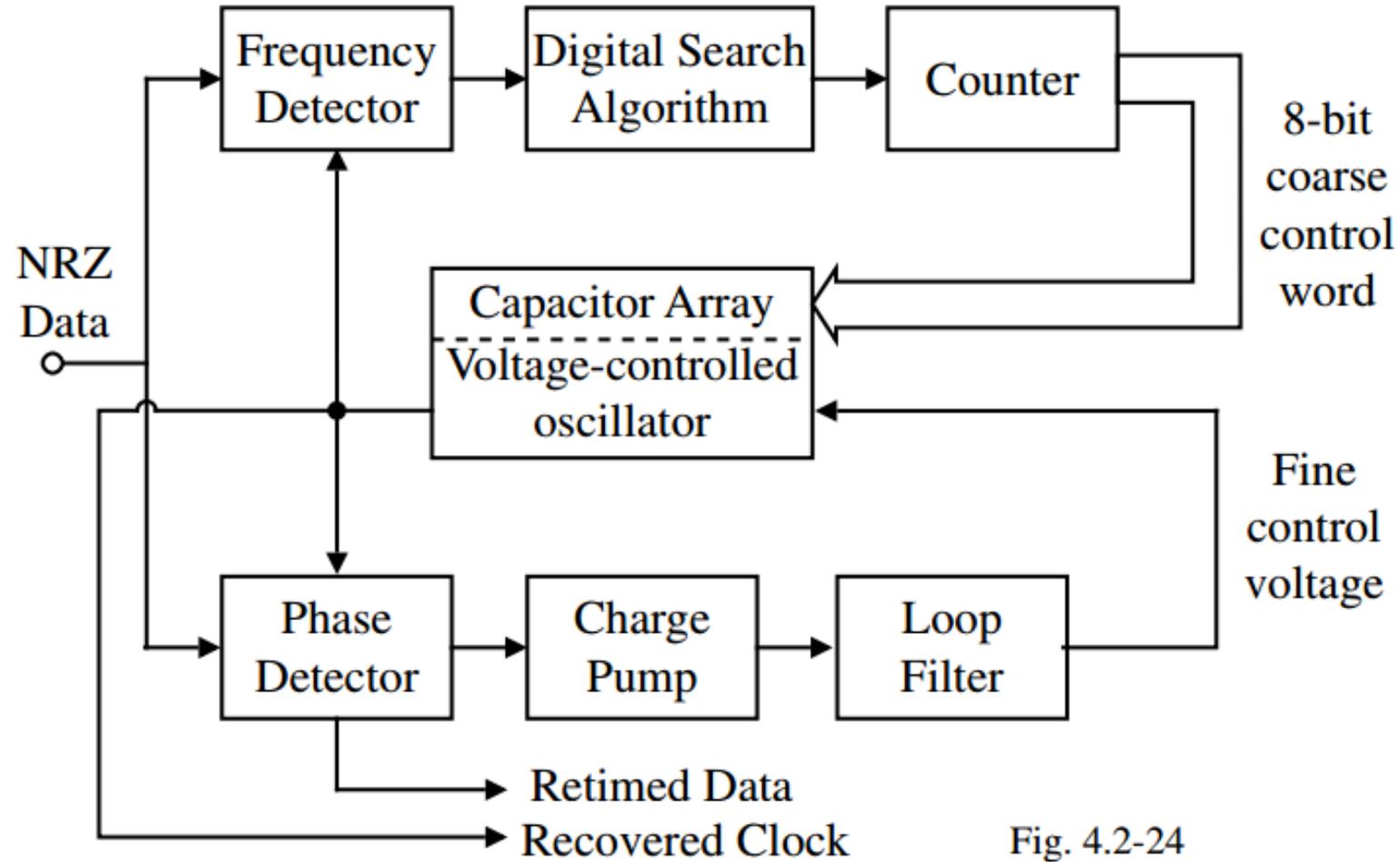
PLL principle



Phase locked loop diagram showing voltages

<https://www.electronics-notes.com/articles/radio/pll-phase-locked-loop/tutorial-primer-basics.php>

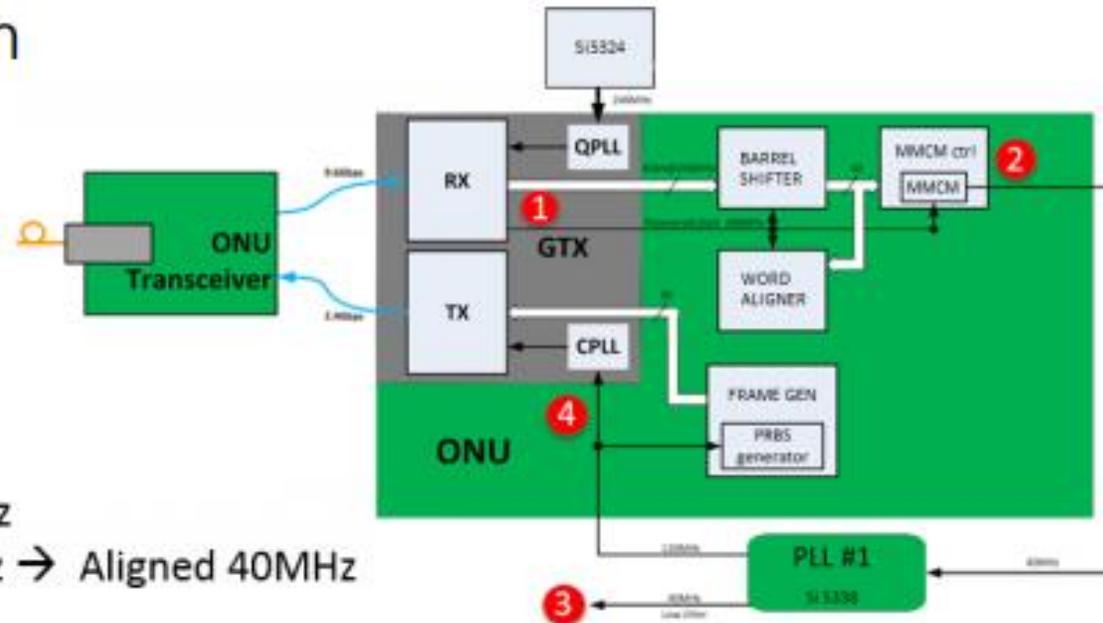
CDR principle



TTC-PON ONU synchronization for upstream

Link synchronization @ ONU ...

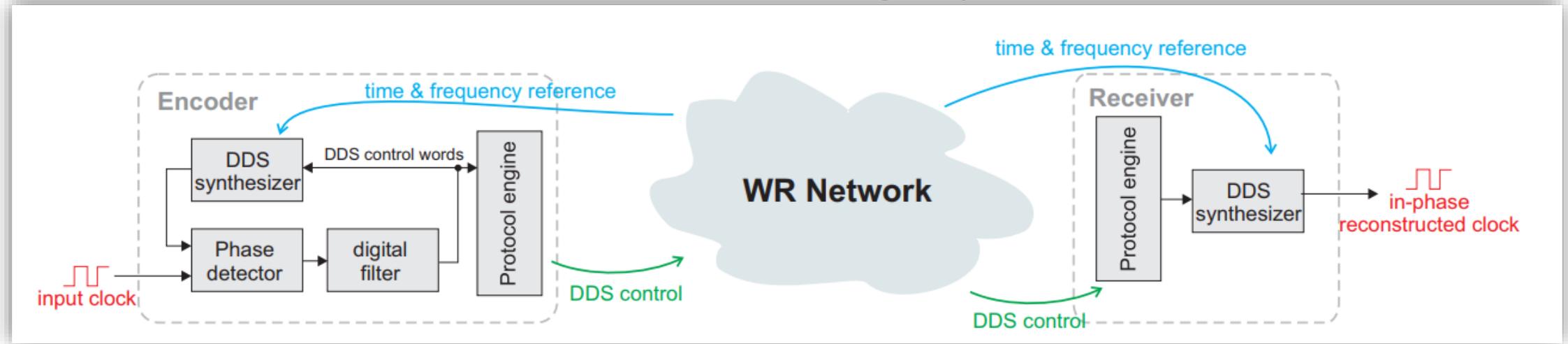
- o Clock recovery and re-use for upstream transmission



1. Recovered 240MHz
2. 240MHz \rightarrow 40MHz \rightarrow Aligned 40MHz
3. Clean 40MHz
4. 40MHz \rightarrow 120MHz aligned to 40MHz

Bunch Clock over White Rabbit

Distributed Direct Digital Synthesis



- Phase and frequency information of the RF/Bunch Clock could be transmitted with a fixed propagation time guaranteed by the White Rabbit Network allowing to reconstruct the RF/Bunch clock at the node
- If the DDS synthesizer is precise enough, the reconstructed RF/Bunch Clock could potentially benefit from the best of both worlds:
 - Excellent quality
 - Fixed phase wrt the RF/BC source

=> Requires specific and careful design, handled by the White Rabbit Team