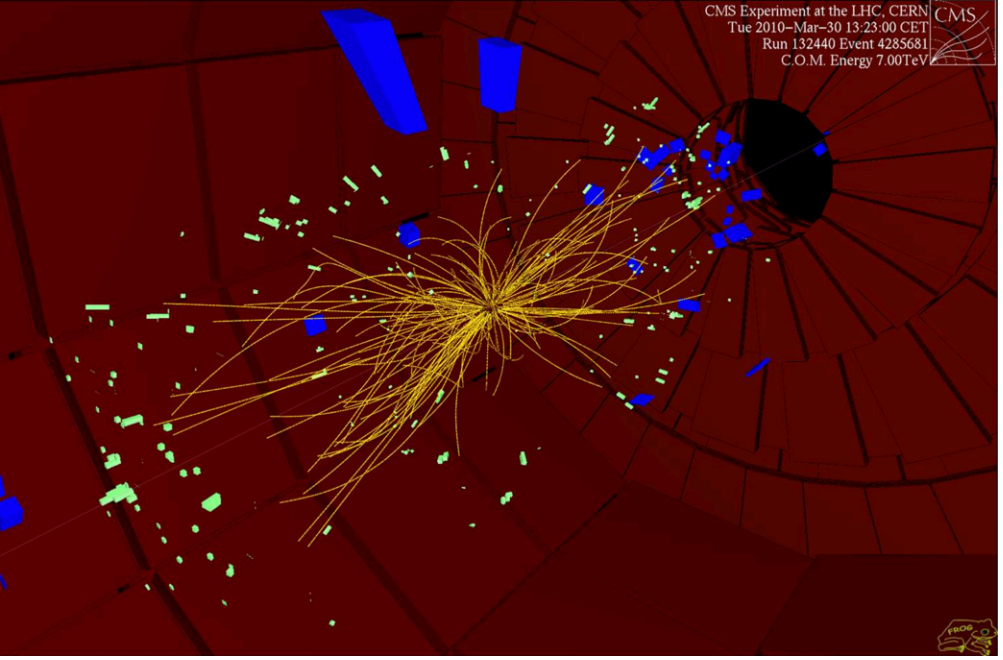

Microelectronic technologies for HEP Instrumentation

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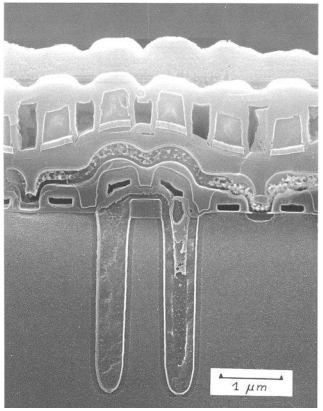
Alessandro.Marchioro@cern.ch

Do you consume more wheat (rice) or transistors?

- Annual worldwide production of wheat is about 770 M metric-tons (see *Wikipedia*)
- One grain of wheat weights 0.065 gr (also *Wikipedia*)
- Total number of wheat grains: 1.2e16

- # of DRAM (Gb equivalent) chips produced per year is 64 B units (see *DRAMExchange*)
- # Transistors/ Gb: 1e9



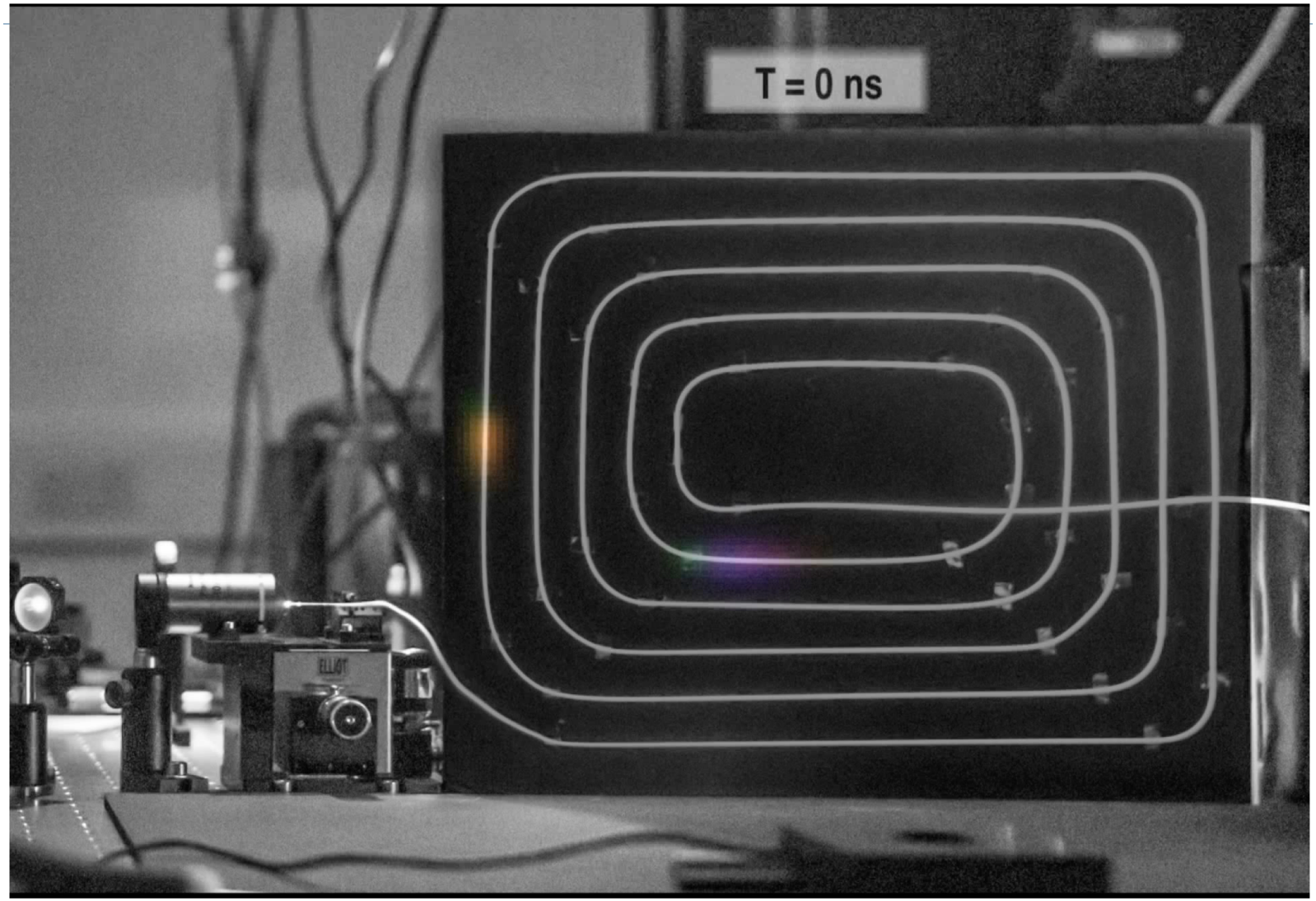
- Total number of transistors (in DRAMs only) is: 6.4e19

Topics

- Motivations
- What is microelectronics ?
- Trends and limitations
- What can you do with microelectronics ?
- Take home message


This detector contains ~1,000,000
custom made integrated circuits of
about 20 types, some of them
collecting signals consisting
of a few thousand electrons

Ultra-Fast Imagers

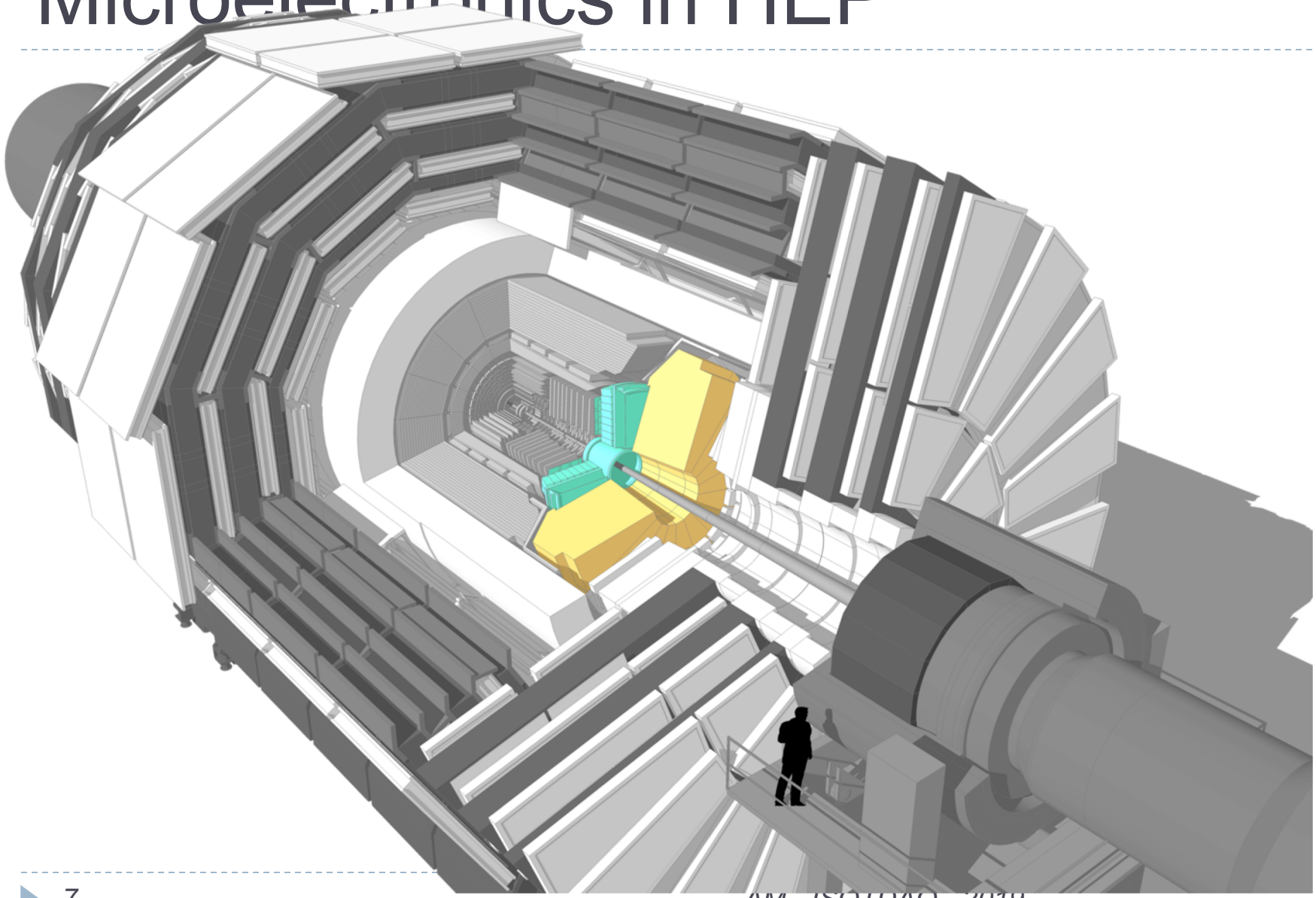


R. Warburton et al., Sci. Rep. 7

Motivations and Trends

- Generation 0.1 (1980's) of chips for experiments where essentially integrated custom amplifiers for sensing detector signals
- The LHC 1.0 generation (late '90s) are full multichannel systems to cover large surfaces of silicon detectors and/or large number of calorimeter channels
  - Pixels and strip electronics are essentially position sensitive detector with little if any high level discrimination capabilities
- Next generation:
  - Larger areas at lower cost
  - Much improved functionality (meaningful data out, not just DN)
  - Digital can help analog (like in so many commercial devices)
    - E.g.: simplify tedious calibration and stability monitoring tasks
  - Embedded processing: digital filtering, particle discrimination, cluster reduction …
    - Energy and/or momentum (vector)
    - Timing
  - Unique digital functionality
    - Example: Associative Memories for Fast track recognition
  - Full channel digital signal processing (but physicists need to be educated…)

Microelectronics in HEP



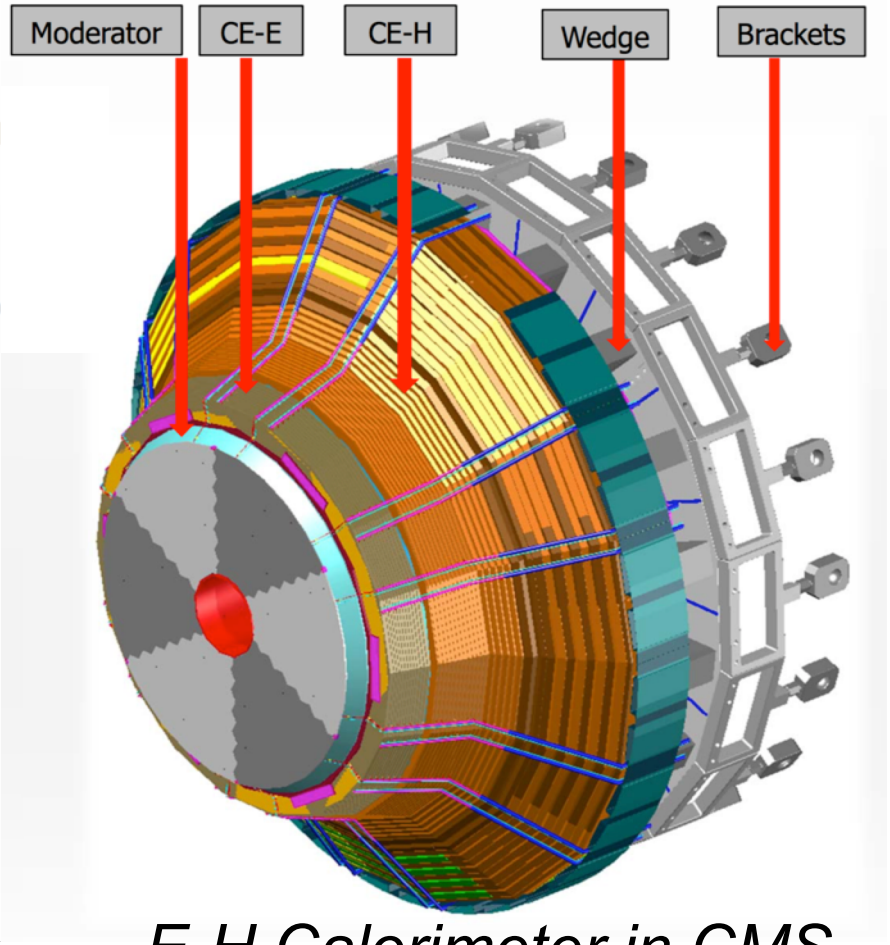
Microelectronics in HEP

Key Parameters:

- *CMS-HGCAL covers 1.5 < η < 3.0*
- *Full system maintained at -30°C*
- *~600m^2 of silicon sensors*
- *~500m^2 of scintillators*

- *6M Si channels, 100K custom chips:*
  - *0.5 / 1.1 cm^2 cell size*
  - *~27000 Si modules*

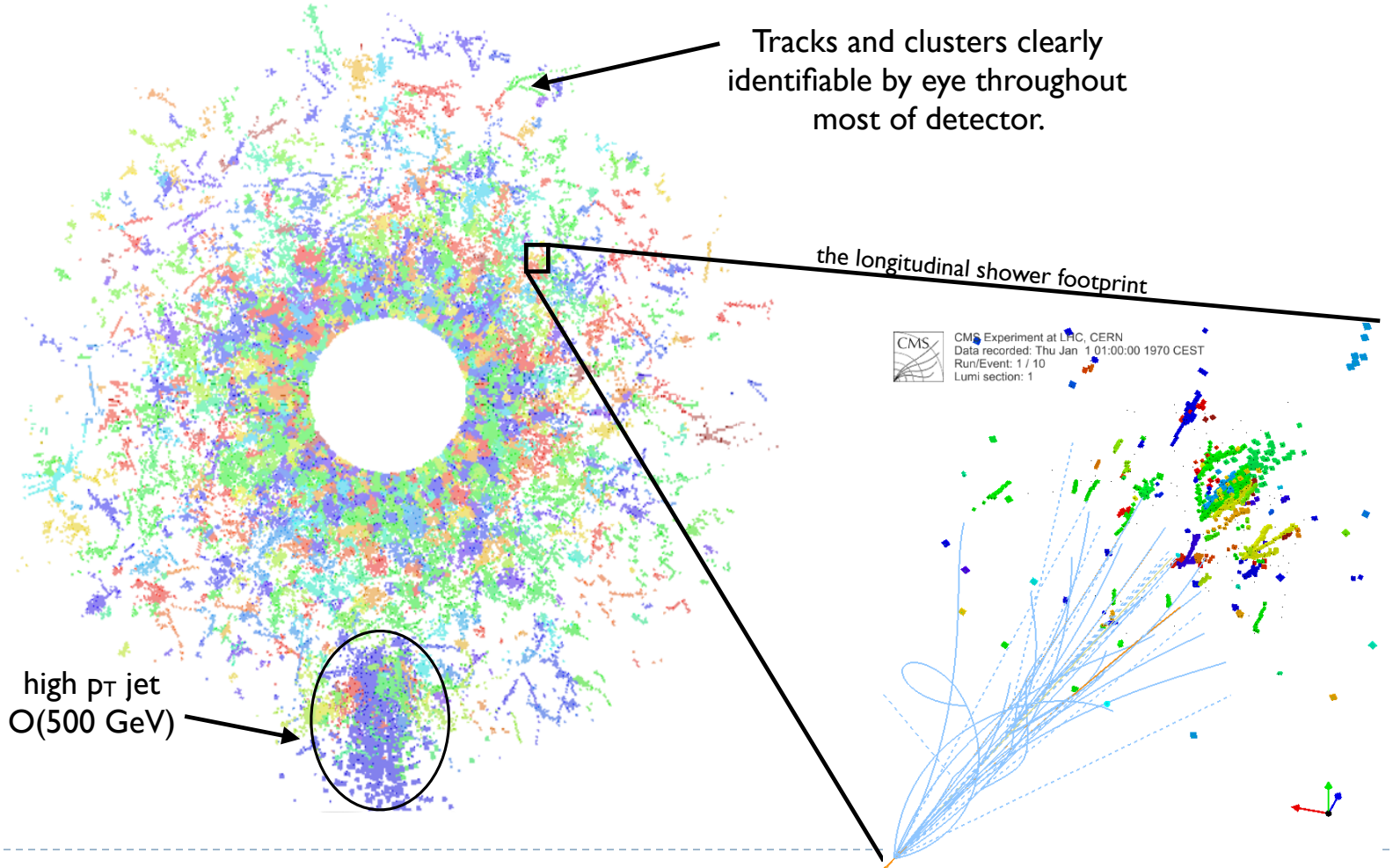
  - *30 x 6 10^6 x 40 10^6 =*
    7.2 10^{15} bits/sec
  - *~16 bit dynamic range*
  - *220 KW*



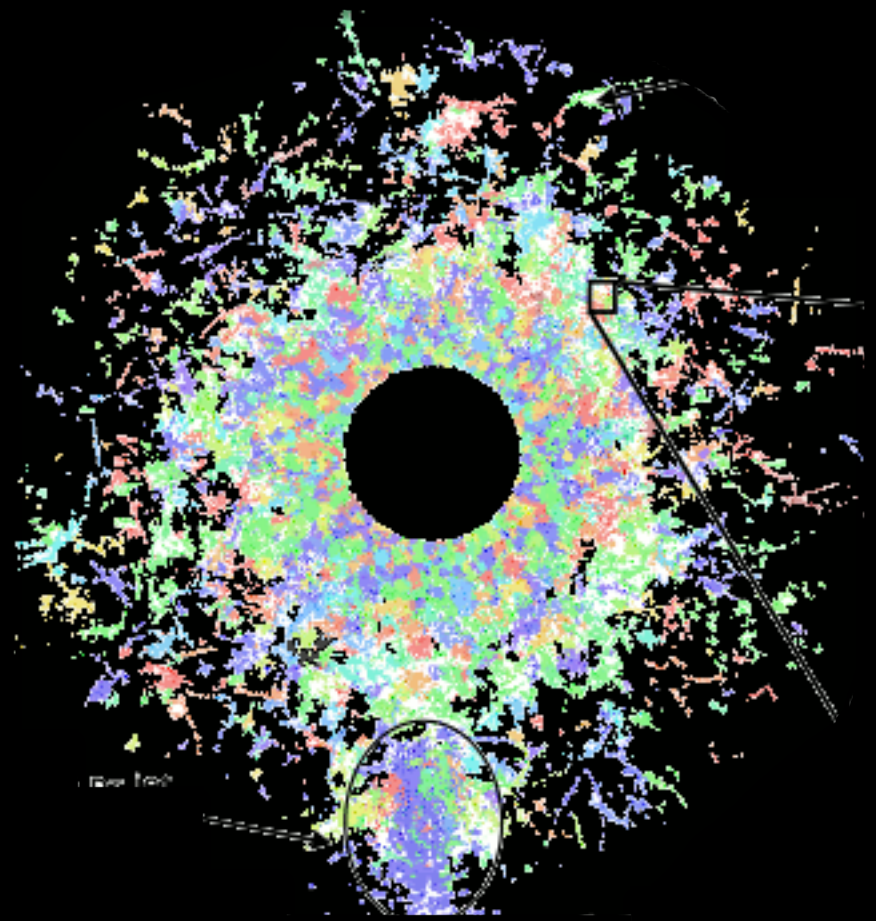
E-H Calorimeter in CMS

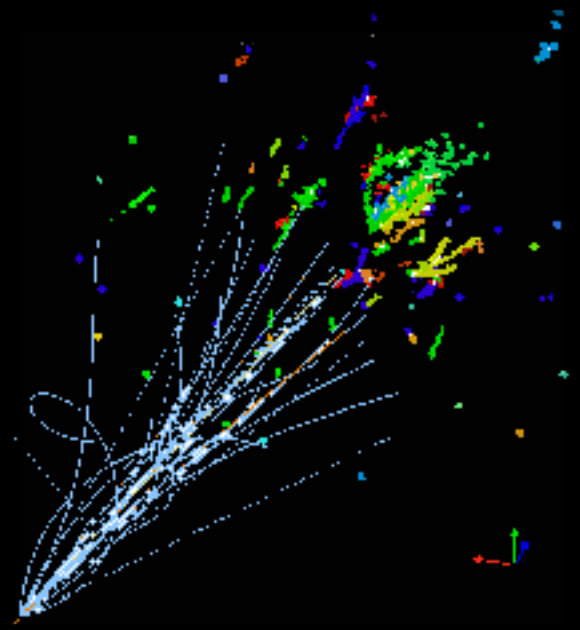
Electronic Camera

Simulation of HL-LHC pileup events in CMS

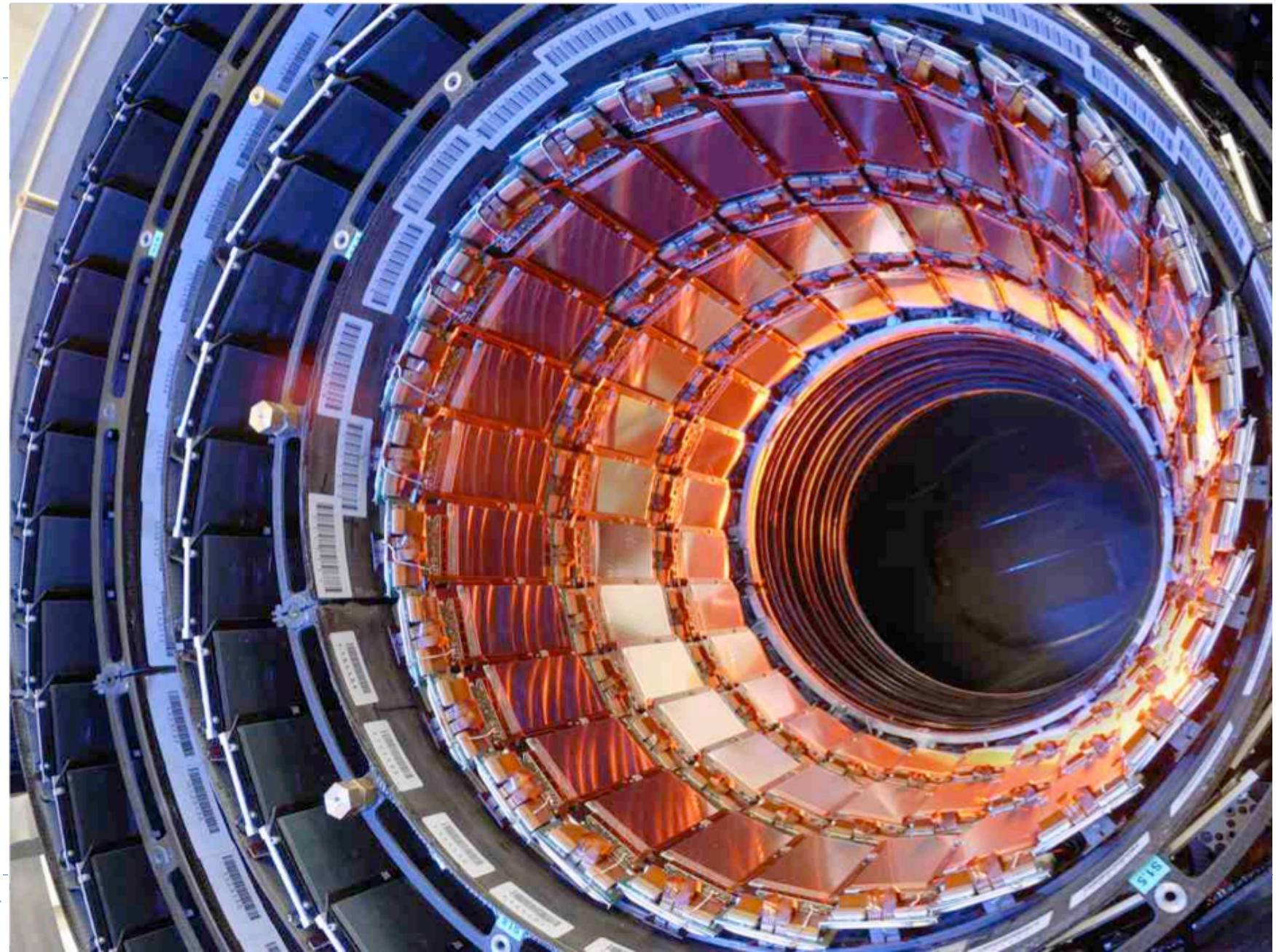


Electronic Camera

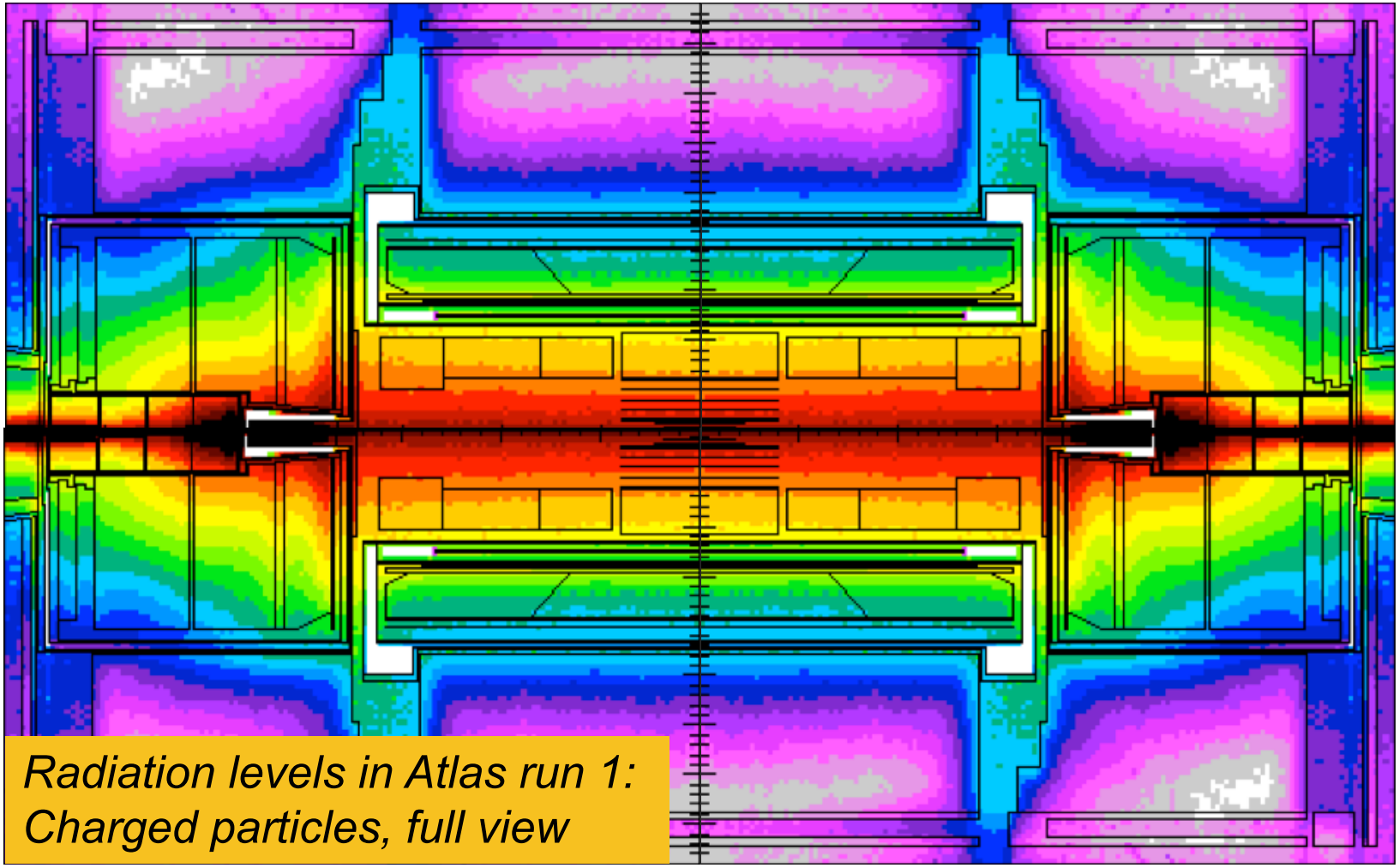




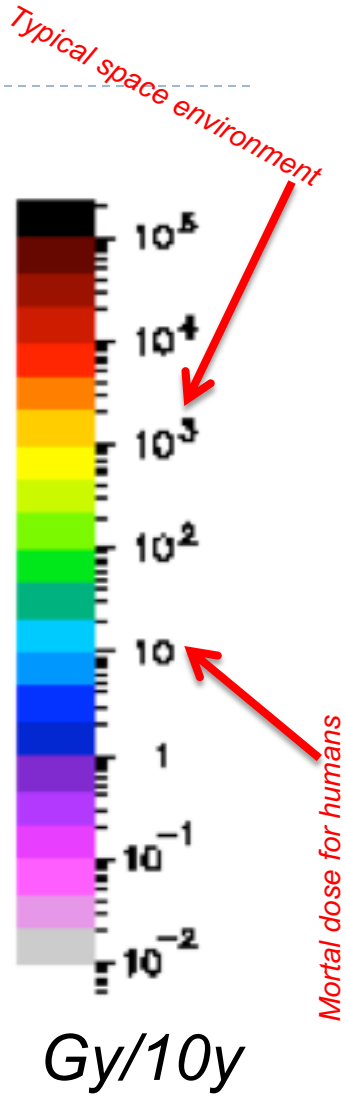
Extra wishes



Un-friendly environment



Radiation levels in Atlas run 1: Charged particles, full view



What is microelectronics?

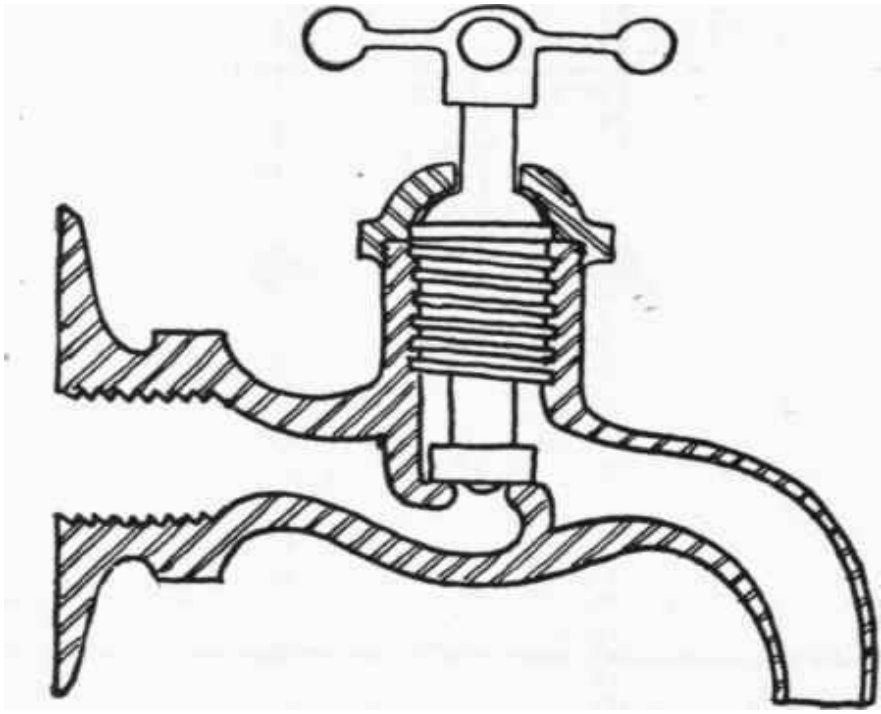
And why is digital important

What is microelectronics?

- Combination of two factors
  - Technology
    - Capability to “print” on a piece of silicon of about 1 cm^2 some 10^9-10^{11} transistors (working mostly as “switches”) of size < 10 nm, each one of which has to work perfectly for 10+ years
    - repeat the above for ~100M pieces
    - … and then sell them for O(10$) / pc.
  - Tools
    - Capability to manage the design and the fabrication of these extremely complex systems designed by teams of 100+ engineers

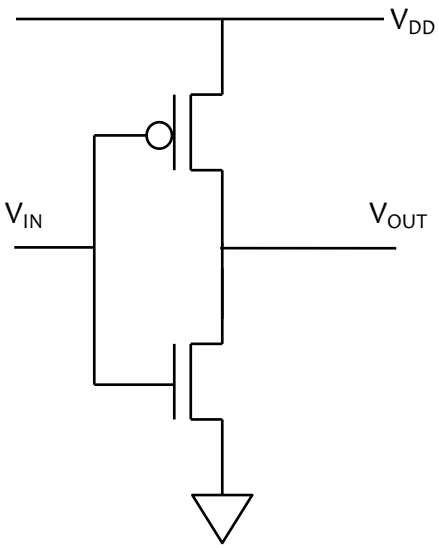
What do we want from a transistor anyway? (sorry analog engineers…)

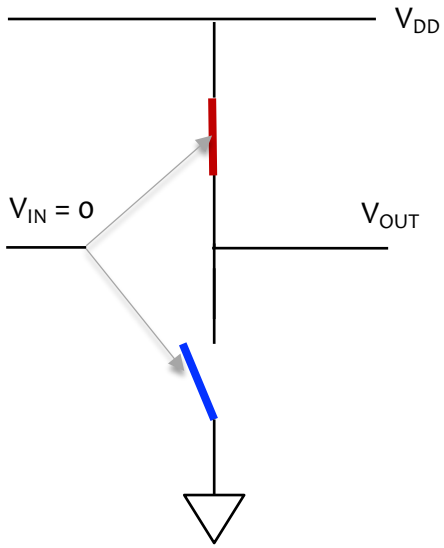
- A transistor (a digital transistor) is a device that "should" have the following characteristics:
  - works as a switch (*on* or *off*), if bi-directional it is even better
  - three terminals: an input, an output, a control
  - makes a "sharp" transition between the two states (open or closed) in a time as short as possible (i.e. carry charge quickly through it)
  - no leakage current when off (I_{on}/I_{off} >(>) 10^6)
  - … while delivering high current when on (drive strongly the load), $I_{on,min}$ ~ 1mA/um
  - the control terminal induces a transition between the two states with a voltage drive (V_{tr}) as small as possible: $P = ½ C V_{dd}^2$ (today V_{tr} ~ 1/3 V_{dd})
  - the control terminal should not be influenced by input/output terminal(s)
  - be physically small (otherwise other "parasitics" ruin the party)
  - must have complementary type (i.e. a second type which is turned on when the first is turned off using the same "control").

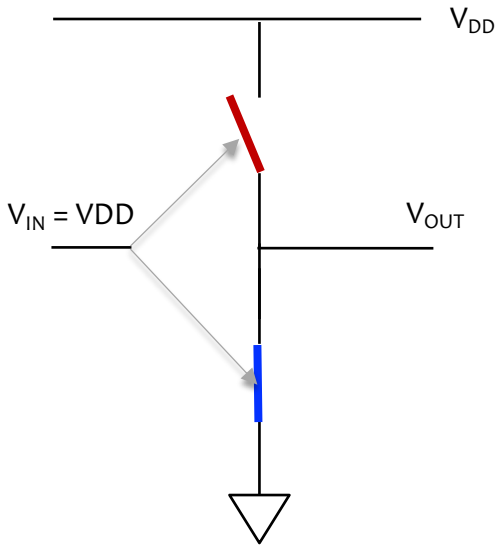


- "Good analog" characteristics are desirable but by far not necessary or even important for the the majority of applications.
  - In fact modern deep-submicron devices have "horrible" analog characteristics and analog designers have a very hard time to achieve what was "easy" 20 years ago

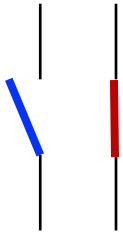
Simple Inverter Gate



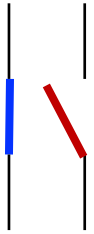




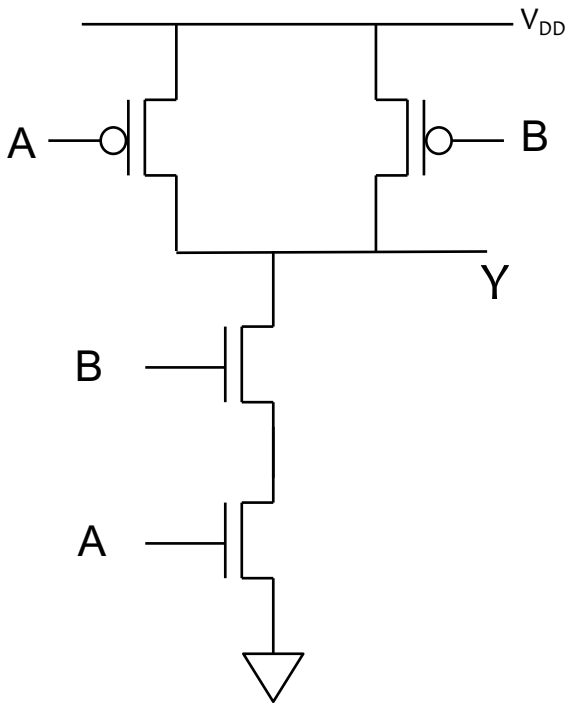
$V_{IN} = 0$ ☛



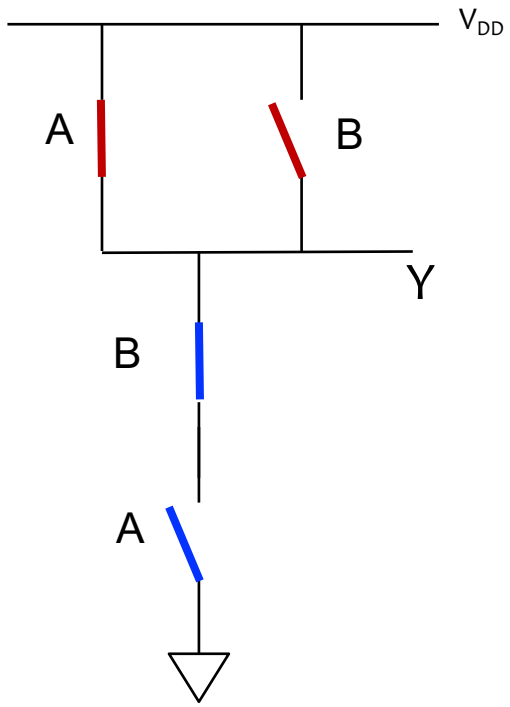
$V_{IN} = V_{DD}$ ☛



Simple NAND Gate

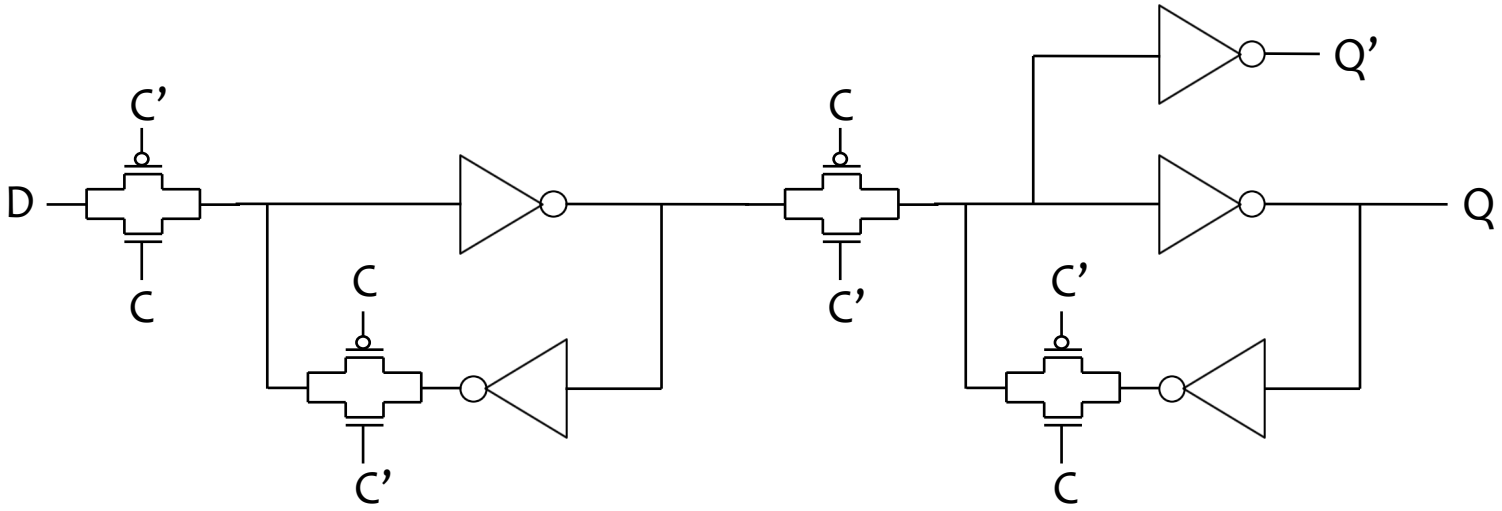


NAND

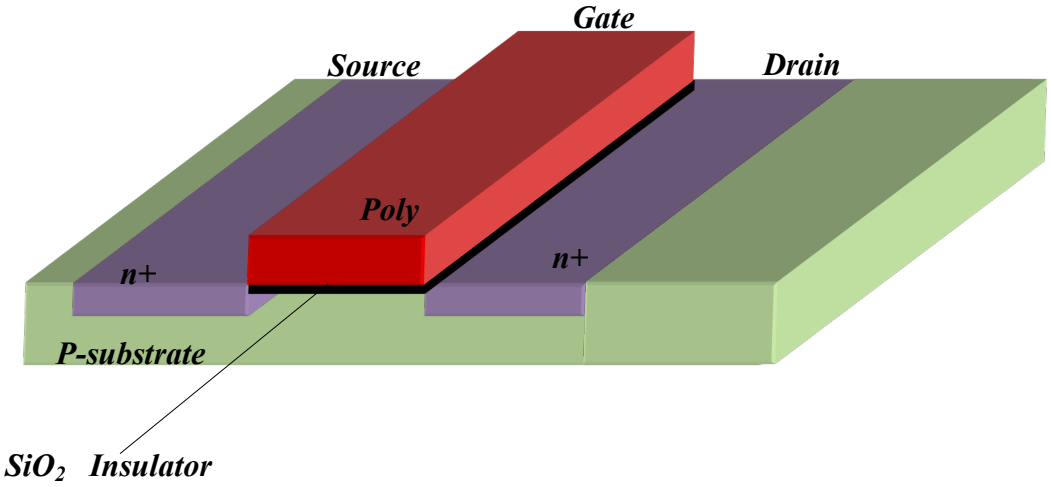


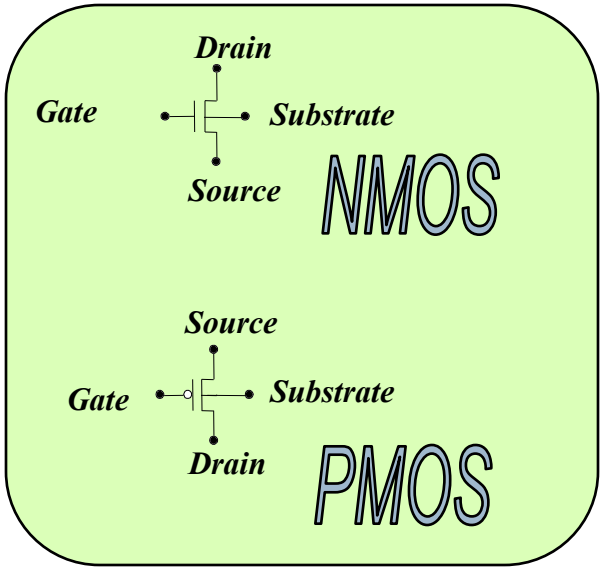
A = 0, B = 1 ☛ Y = 1

Flip-Flop Memory Element

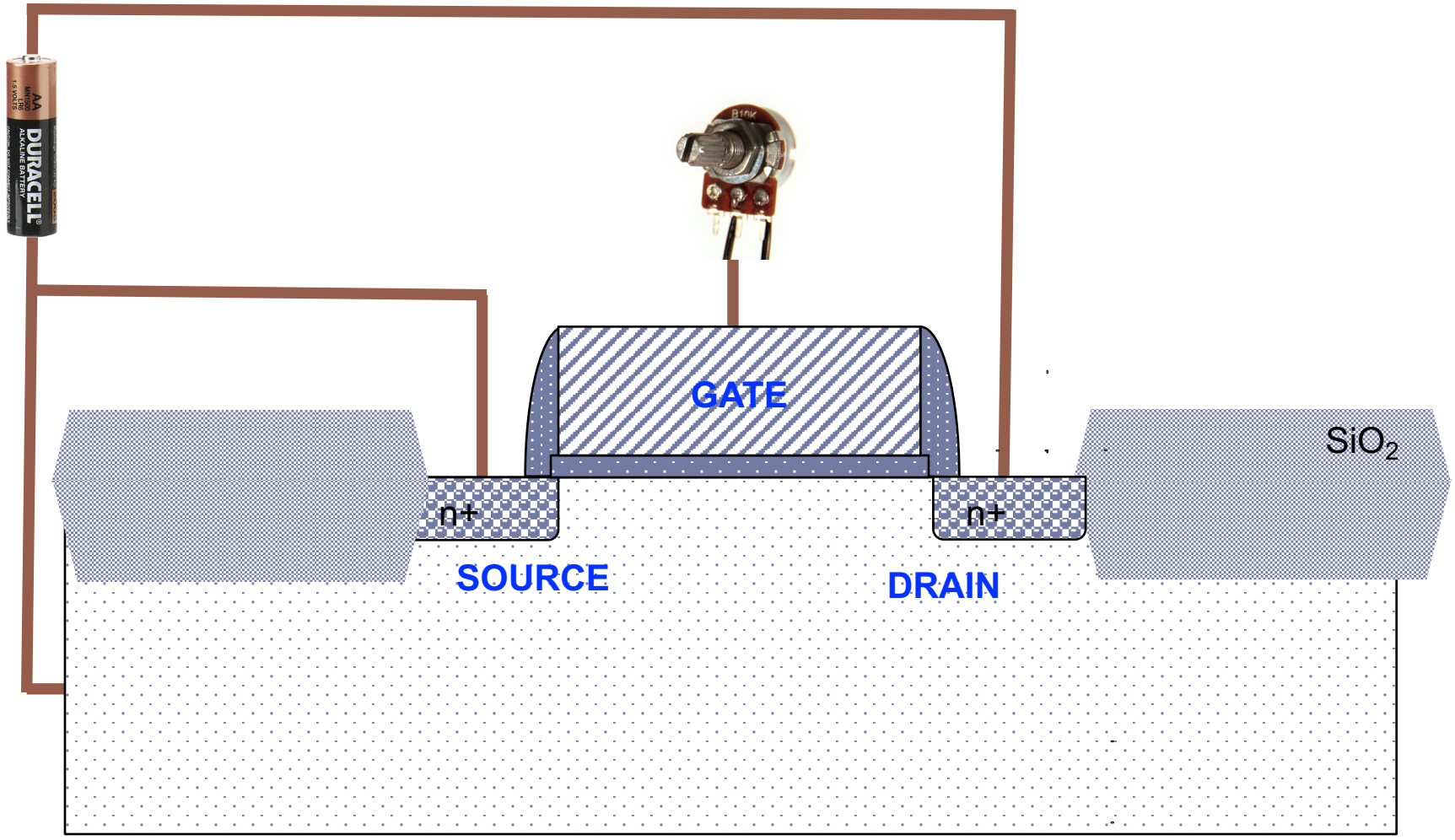


MOS transistors

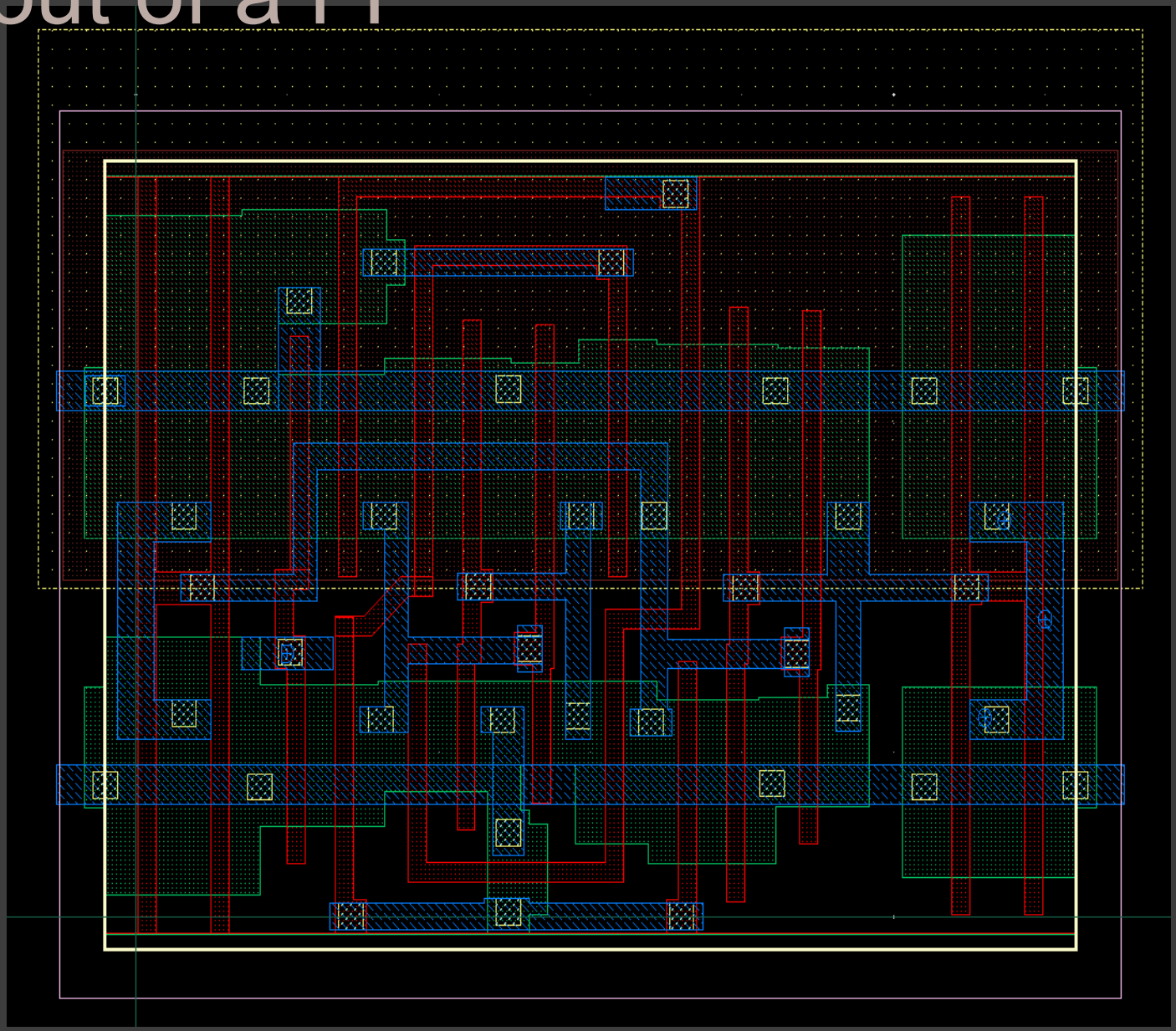




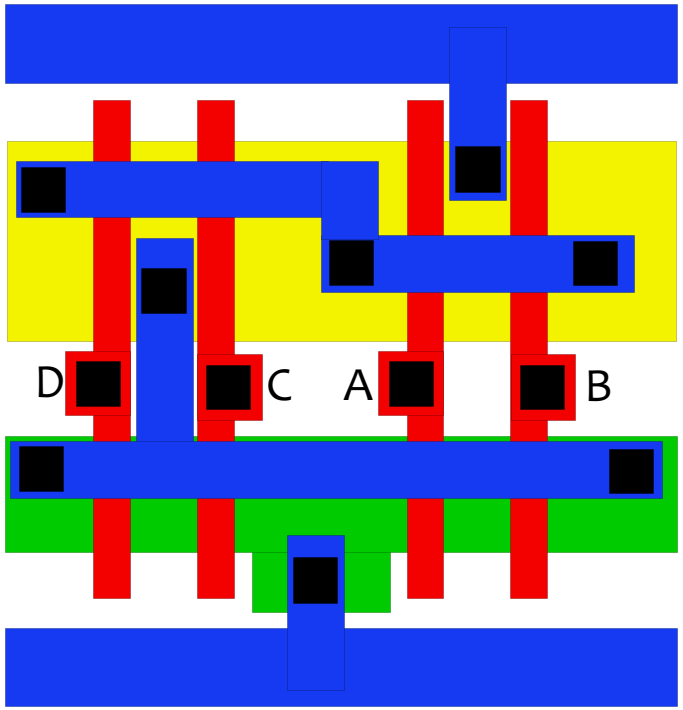
MOS transistor

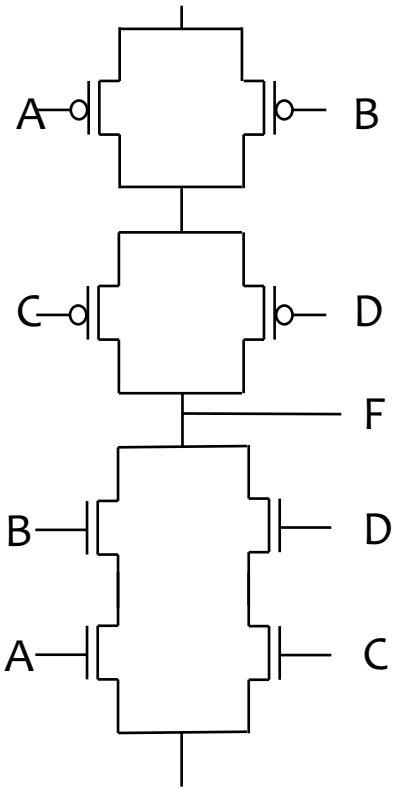


Layout of a FF



Layout of a logic gate





MOS Transistor equations

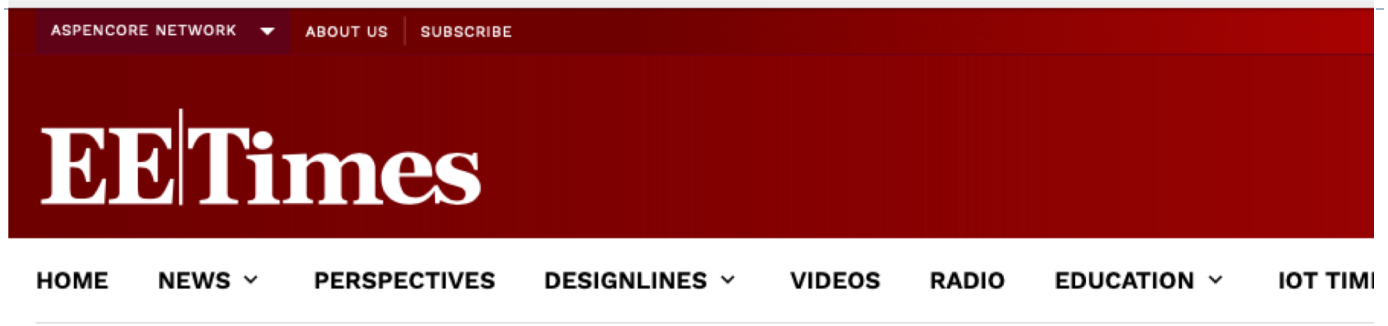
$$I_{ds} = \frac{\mu\varepsilon}{t_{ox}} \frac{W}{L} ((V_{gs} - V_t)V_{ds} - \frac{V_{ds}^2}{2}) \qquad Non-saturation$$

$$I_{ds} = \frac{\mu\varepsilon}{2t_{ox}} \frac{W}{L} (V_{gs} - V_t)^2 \qquad Saturation\ region$$

Geometric parameters
Defined at layout time

Electrical parameters
Depend on circuit behavior

Manufacturing parameters,
can't be changed on a given technology



DESIGNLINES | PROGRAMMABLE LOGIC DESIGNLINE

Report: TSMC's 3nm Fab Could Cost $20 Billion

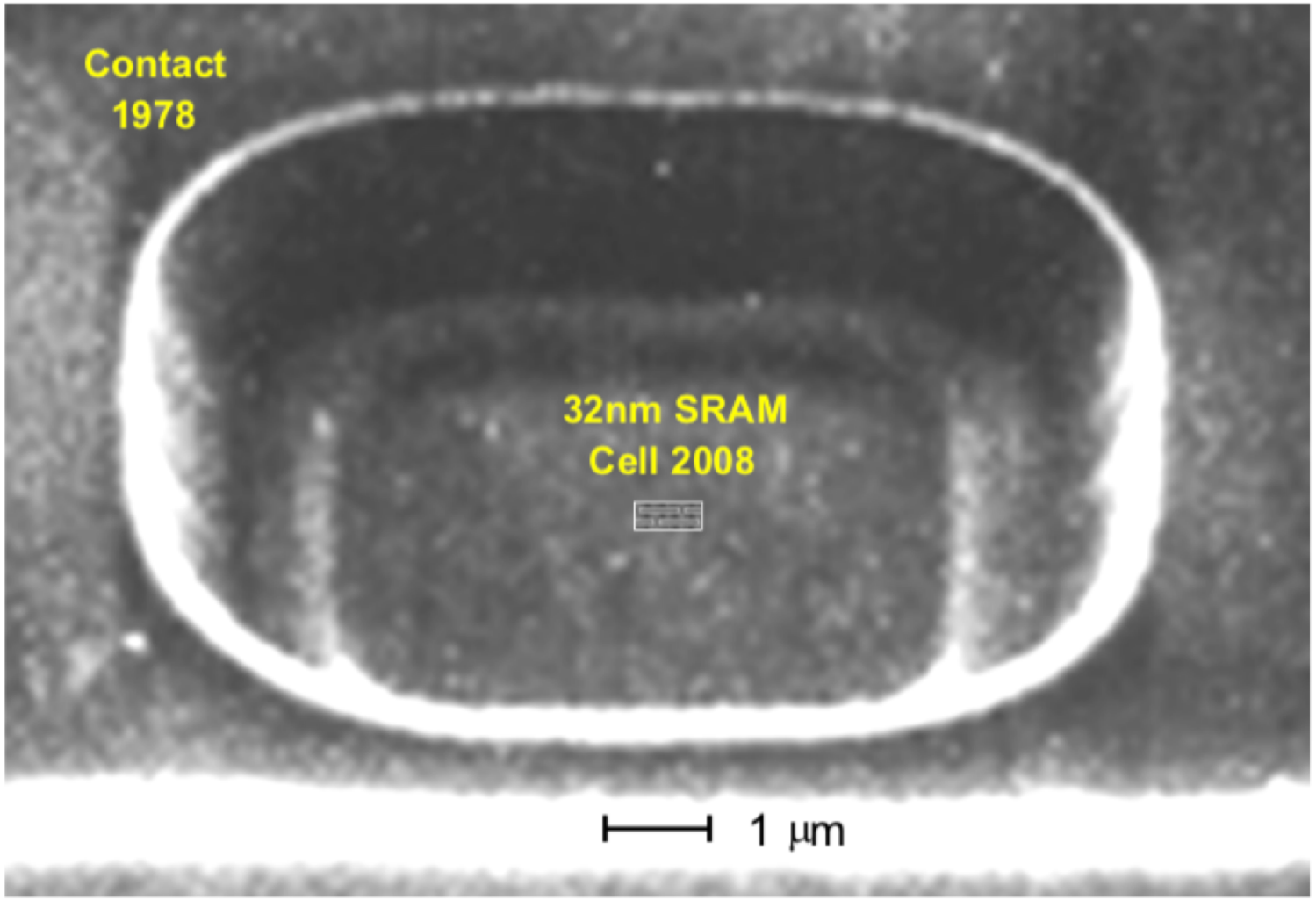
By EE Times, 10.09.17 0

Share Post Share on Facebook Share on Twitter

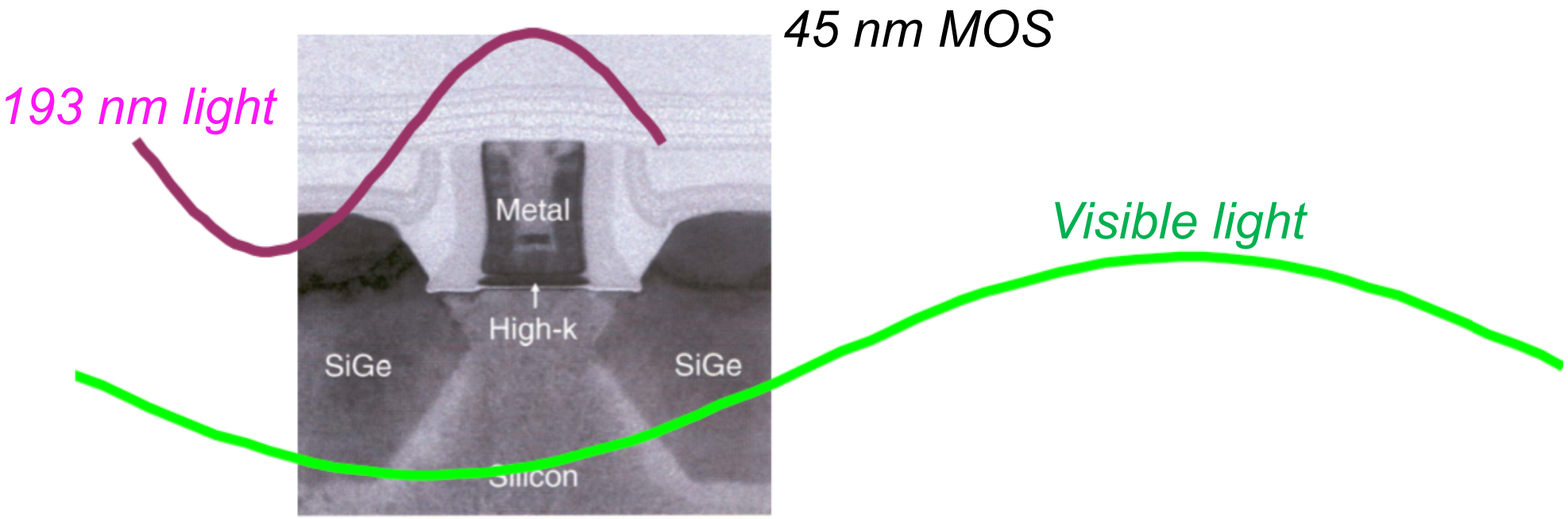
SAN FRANCISCO — A 3mn fab being planned by chip foundry giant TSMC is likely to cost more than $20 billion to build and equip, TMSC Chairman Morris Chang **told the Bloomberg news service.**

TSMC announced last week it would locate what is the world's first announced 3nm fab in the Tianan Science Park in southern Taiwan, laying to rest speculation that TSMC might build the fab in the U.S. or elsewhere outside of Taiwan. TSMC did not give a timeframe for the fab's completetion, but has said in the past it would build a 5- or 3nm fab as early as 2022.

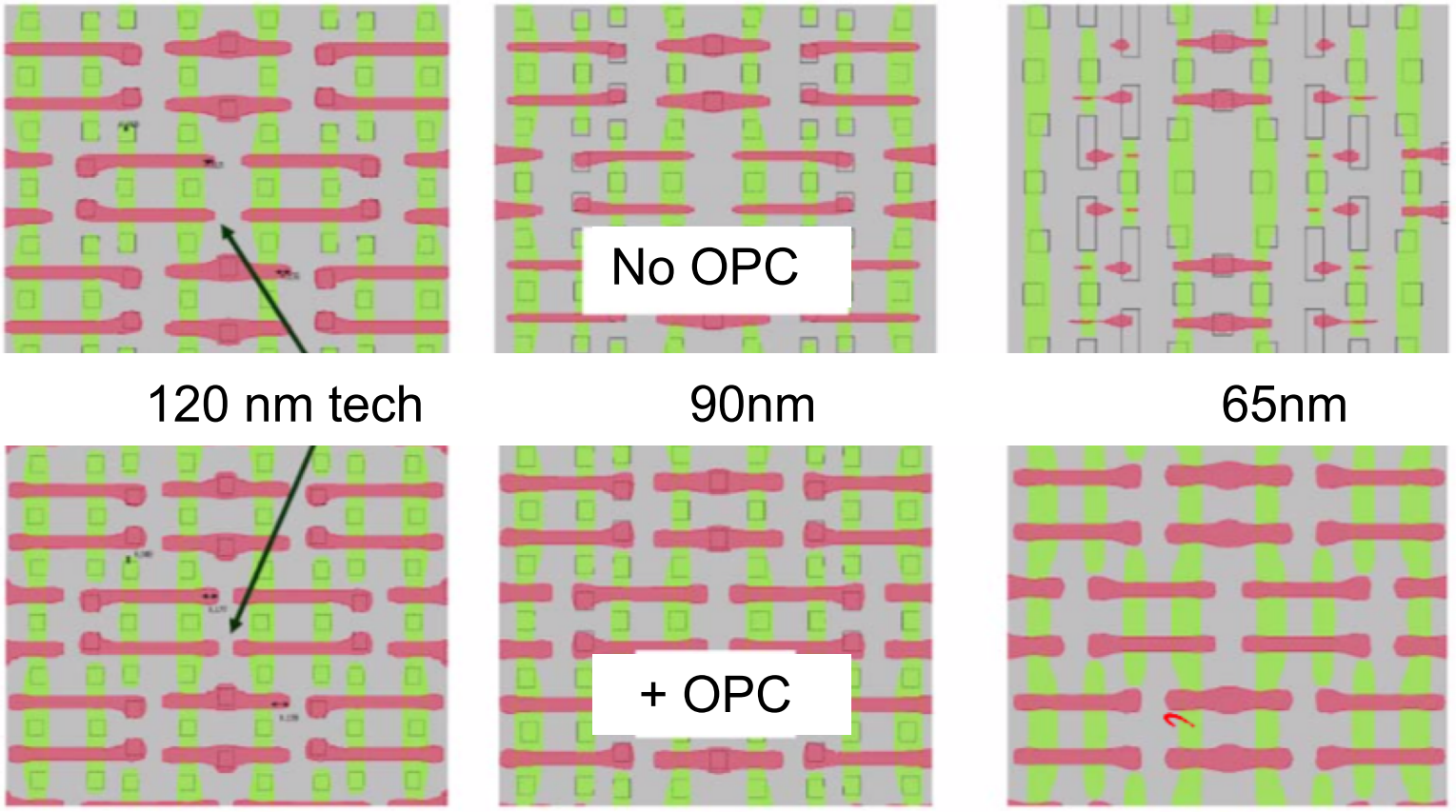
One of the difficulties: Lithography



Lithography (2)

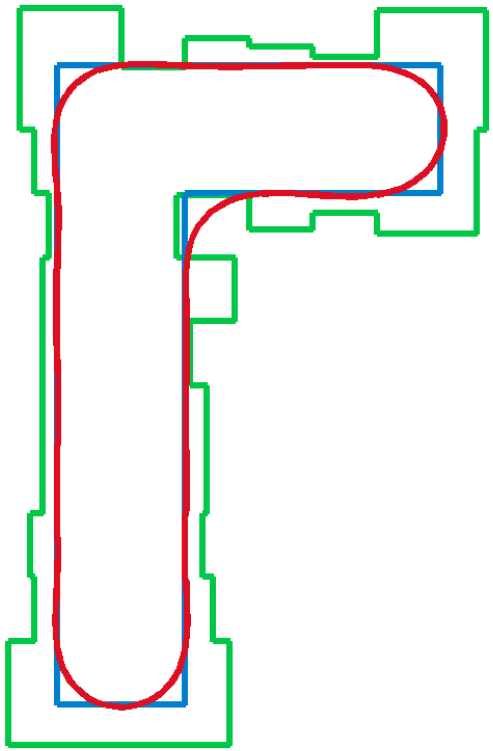


Lithography (3)

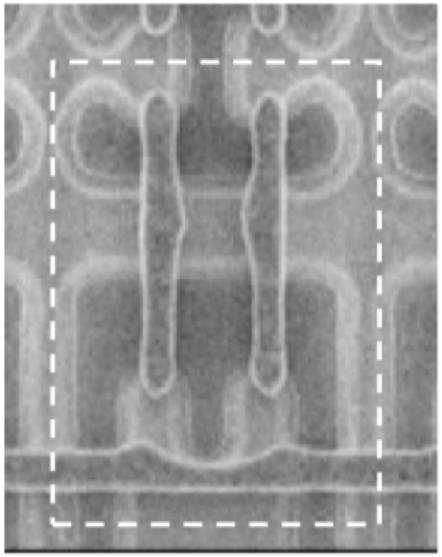


Lithography (4)

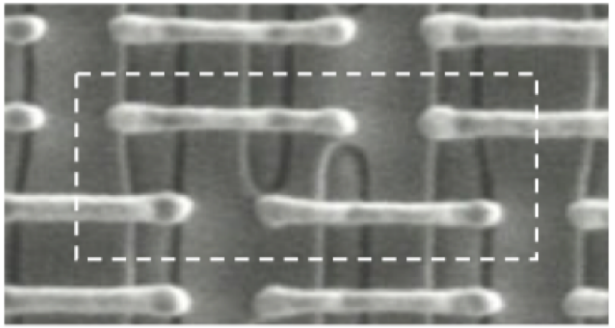
- Optical Proximity Correction Techniques (Computational Lithography)



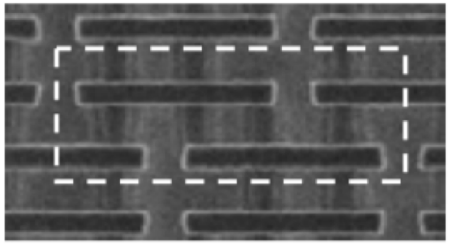
Lithography (5)



90nm – TALL
1.0 μm²

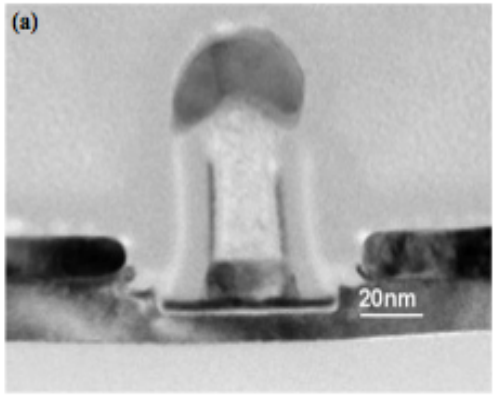


65nm – WIDE - 0.57 μm²

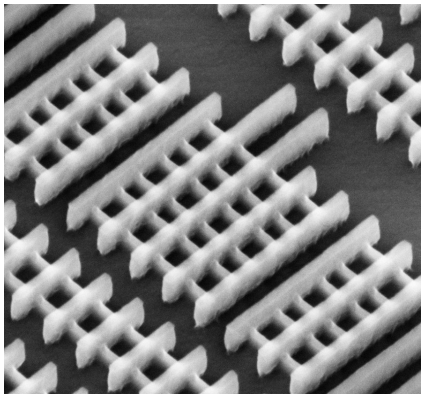


45nm – WIDE
w/ patterning
enhancement 0.346 μm²

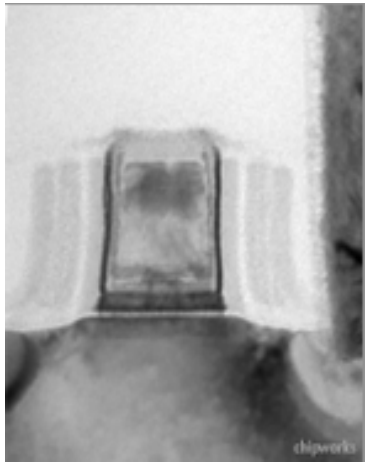
Some advanced devices



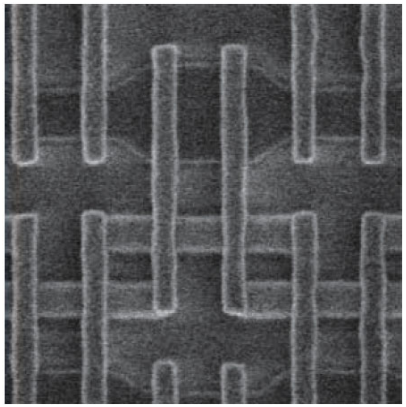
20 nm FDSOI from ST



22 nm TriGate from Intel



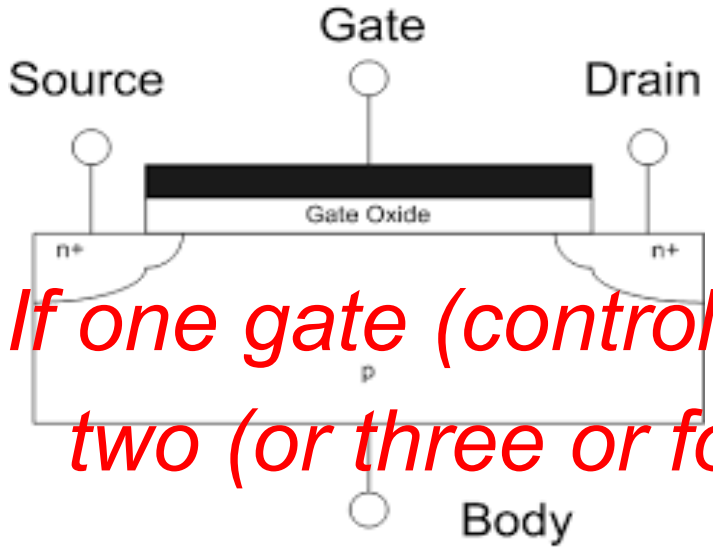
28 nm planar from TSMC



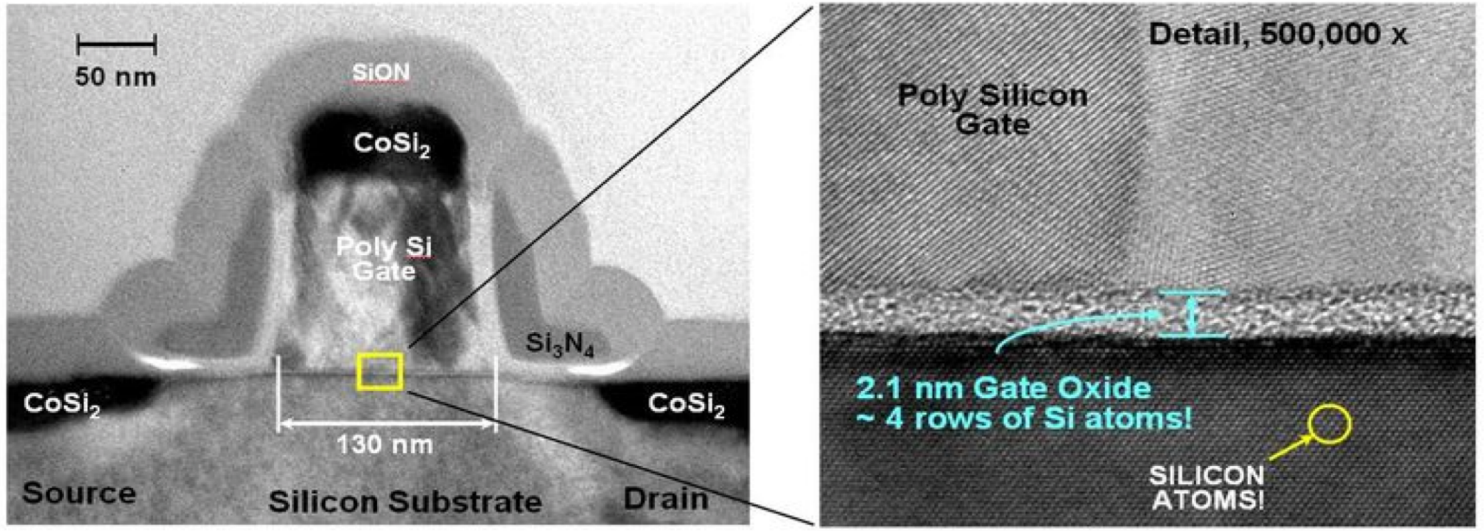
32 nm SOI from IBM

Various sources

Multi-gate devices



If one gate (controlling surface) is good, two (or three or four) are even better



Solid-State Electronics Vol. 27, Nos. 8/9, pp. 827–828, 1984
Printed in Great Britain

0038-1101/84 $3.00 + .00
1984 Pergamon Press Ltd.

CALCULATED THRESHOLD-VOLTAGE CHARACTERISTICS OF AN XMOS TRANSISTOR HAVING AN ADDITIONAL BOTTOM GATE

(*Received* 30 *May* 1983; *in revised form* 24 *August* 1983)

Toshiba 1983

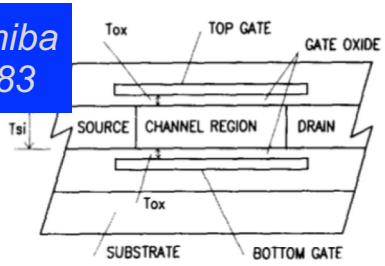


Fig. 1. Schematic cross-sectional structure of an XMOS transistor having an additional bottom gate which is symmetrically placed to a top gate with a channel region between them. "*X*" originates from Greek capital letter of xi as this structure resembles its shape.

Electronic Device Division,
Electrotechnical Laboratory,
Sakura-mura,
Ibaraki, 305,
Japan

T. SEKIGAWA and
Y. HAYASHI

IBM 1994

Figure 1: Schematic views of the double-gate SOI MOSFET's.

IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 38, NO. 6, JUNE 1991 1419

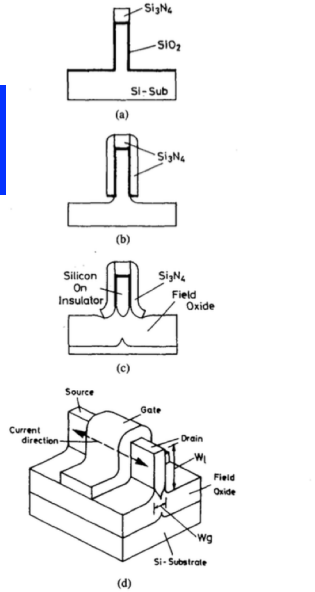
Impact of the Vertical SOI "DELTA" Structure on Planar Device Technology

Digh Hisamoto, *Member, IEEE*, Toru Kaga, *Member, IEEE*, and Eiji Takeda, *Senior Member, IEEE*

***Abstract*—A fully depleted lean channel transistor (DELTA) with its gate incorporated into a new vertical ultra-thin SOI structure is presented. In the deep-submicrometer region, selective oxidation produces and isolates an ultra-thin SOI MOSFET that has high crystalline quality, as good as that of conventional bulk single-crystal devices. Experiments and three-dimensional simulations have shown that this new gate structure has effective channel control, and that the vertical ultra-thin SOI structure provides superior device characteristics: reduction in short-channel effects, minimized subthreshold swing, and high transconductance.**

Hitachi 1989

is required. Moreover, it is evident that these structures are difficult to contact to the substrate, and thus suffer from a substrate floating effect.



ig. 1. (a)–(c) Process flow of selective oxidation. (d) Schematic cross section of DELTA.

Berkely 2000

IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 47, NO. 12, DECEMBER 2000

FinFET—A Self-Aligned Double-Gate MOSFET Scalable to 20 nm

Digh Hisamoto, *Member, IEEE*, Wen-Chin Lee, Jakub Kedzierski, Hideki Takeuchi, Kazuya Asano, *Member, IEEE*, Charles Kuo, Erik Anderson, Tsu-Jae King, Jeffrey Bokor, *Fellow, IEEE*, and Chenming Hu, *Fellow, IEEE*

***Abstract*—MOSFETs with gate length down to 17 nm are reported. To suppress the short channel effect, a novel self-aligned double-gate MOSFET, FinFET, is proposed. By using boron-doped $Si_{0.4}Ge_{0.6}$ as a gate material, the desired threshold voltage was achieved for the ultrathin body device. The quasiplanar nature of this new variant of the vertical double-gate MOSFETs can be fabricated relatively easily using the conventional planar MOSFET process technologies.**

***Index Terms*—Fully depleted SOI, MOSFET, poly SiGe, short-channel effect.**

I. INTRODUCTION

TO DEVELOP sub-50-nm MOSFETs, the double-gate structure has been widely studied. This is because

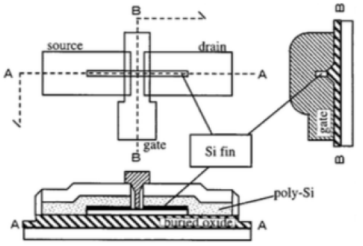
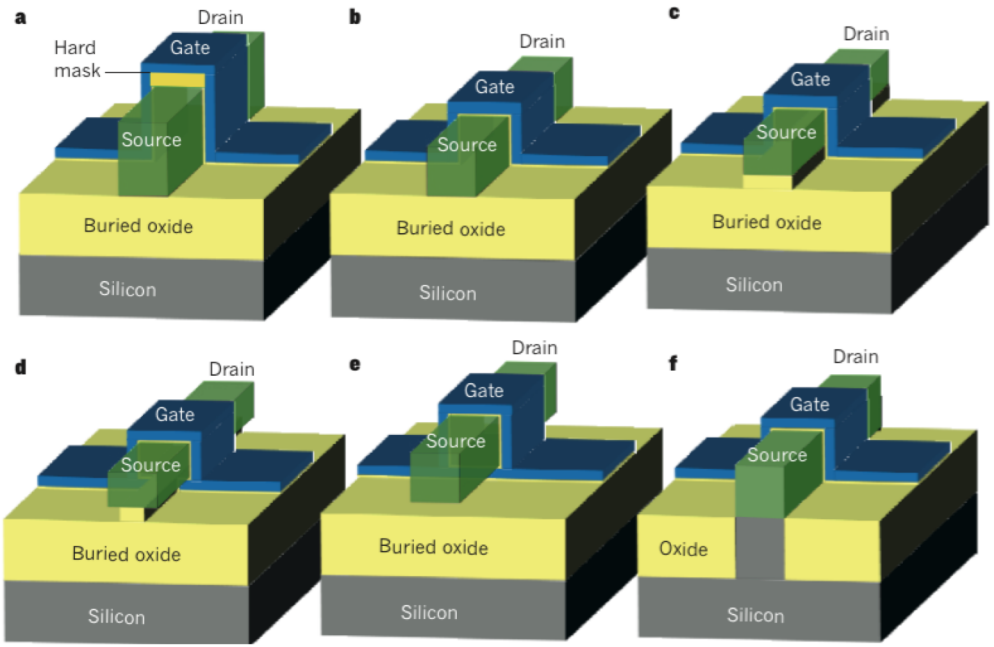


Fig. 1. FinFET typical layout and schematic cross sectional structures.

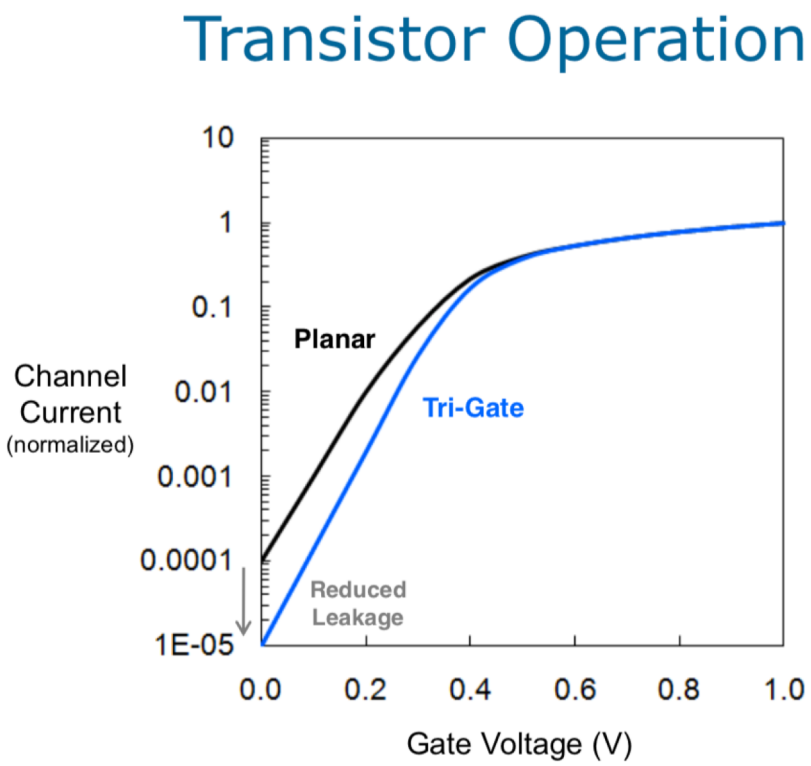
Multi-gate devices

- Intel: Tri-gate
- TSMC, GF, Samsung: Finfets



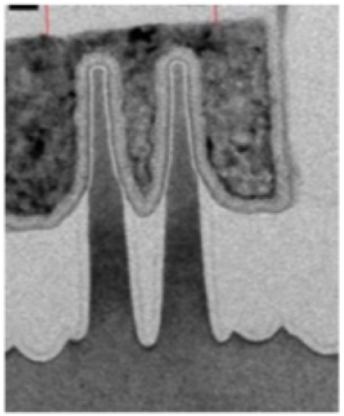
from: Ferain, "Multigate transistors as the future of classical metal–oxide–semiconductor field-effect transistors ",

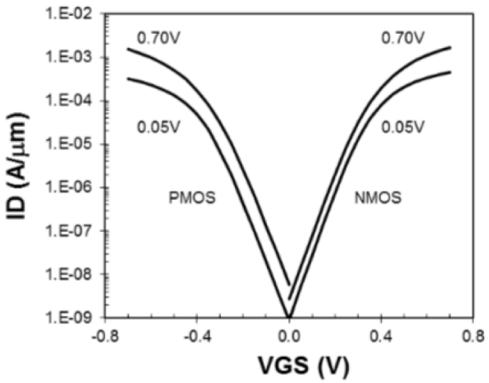
Subthreshold slope improvement

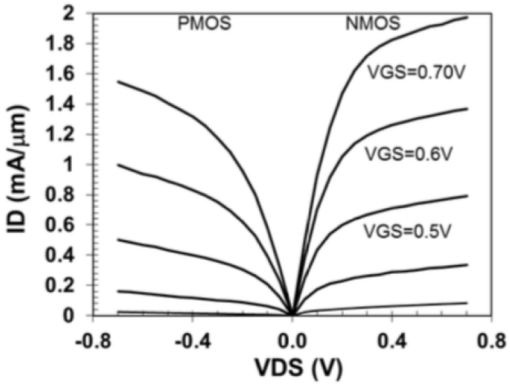


from: M. Bohr (Intel) , Intel's Revolutionary 22 nm Transistor Technology, May 2011

10 nm Finfet

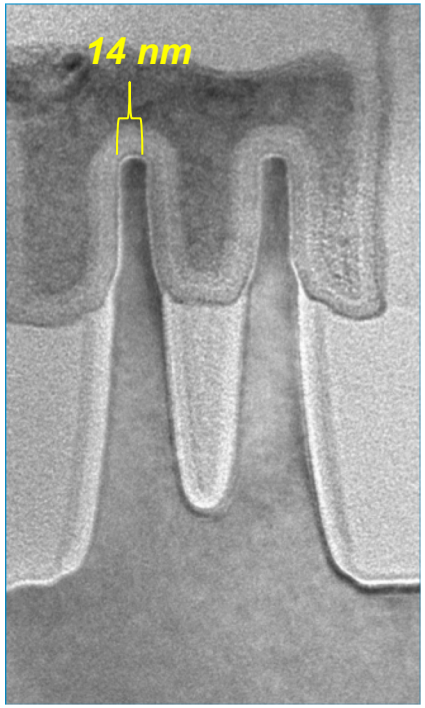




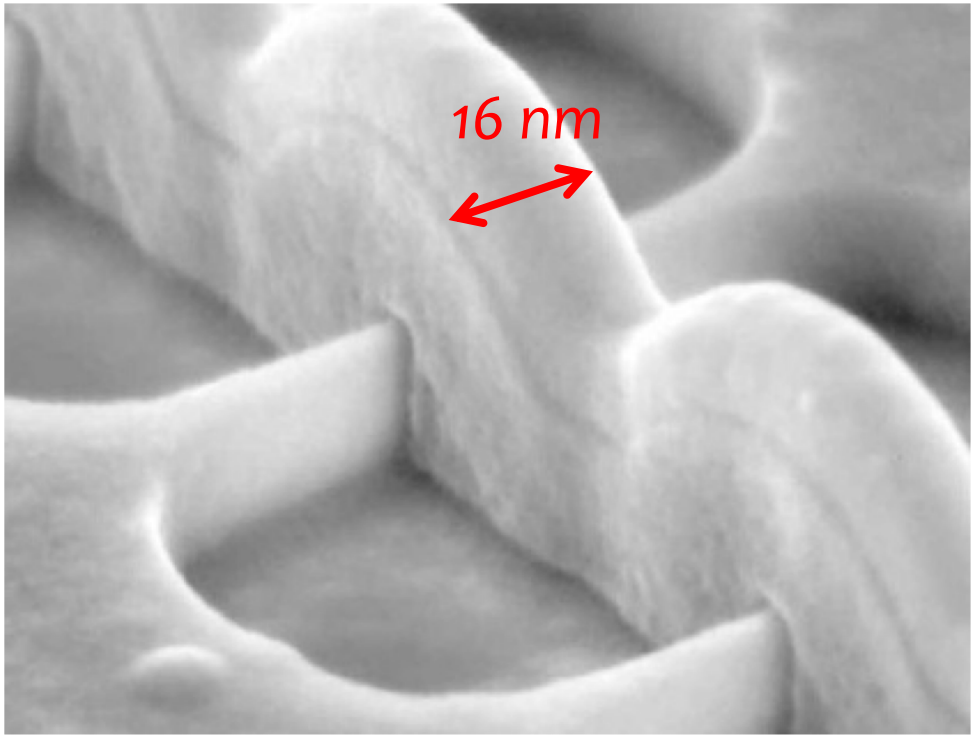


from: A. Auth (Intel), A 10nm High Performance and Low Power CMOS Technology…, IEDM 2017

State of the Art examples: FINFETs



Source: Intel

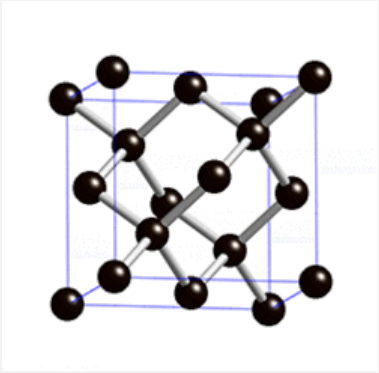


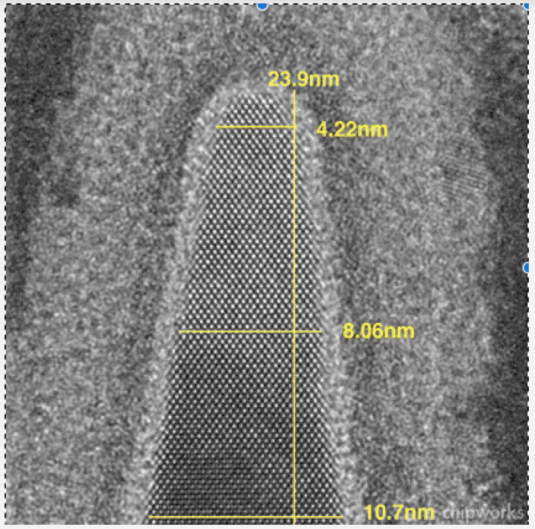
Source: TSMC

Typical FinFET dimensions

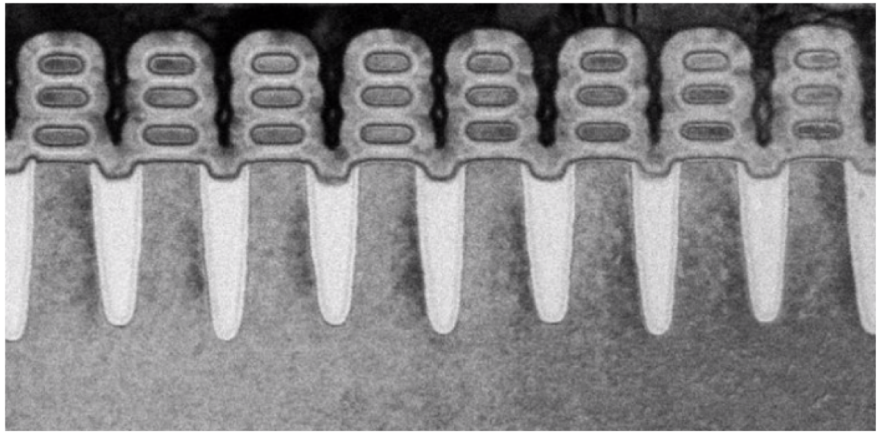
From the ITRS 2011 report

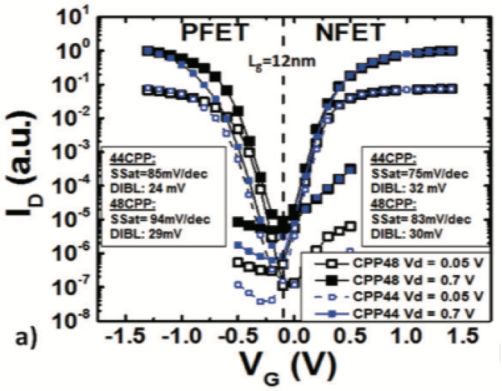
Year of Production	2013	2015	2017	2019	2021	2023	2025	2028
FinFET Fin Width (new) (nm)	7.6	7.2	6.8	6.4	6.1	5.7	5.4	5.0





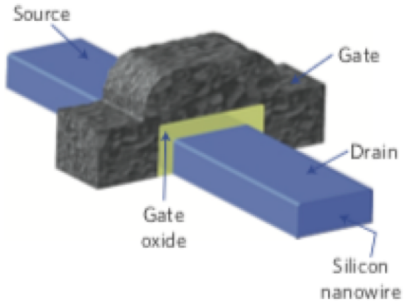
FINFET++ = GateAllAround (GAA)

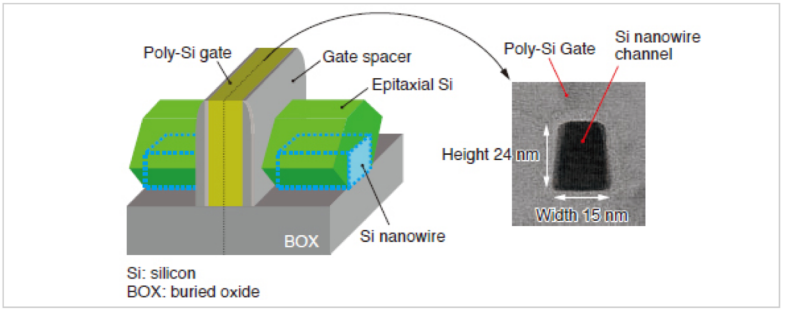


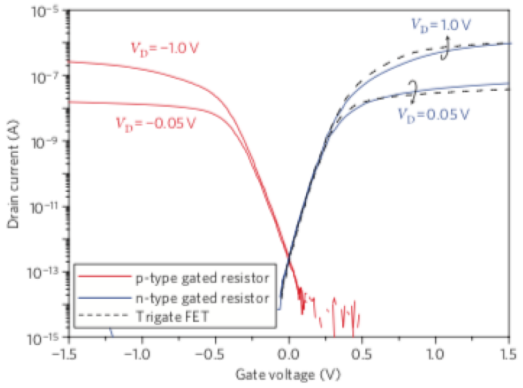


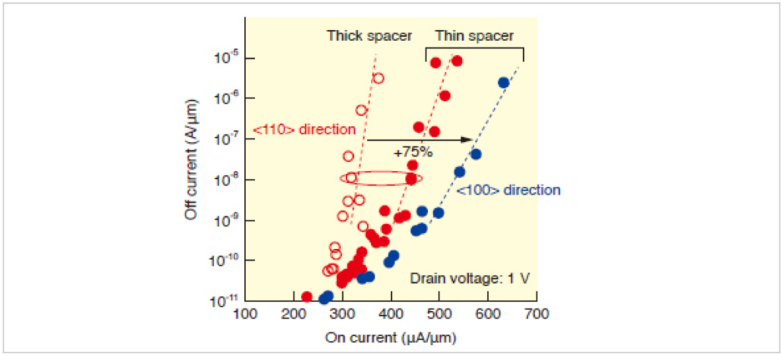
From N. Loubet – IBM –
Stacked Nanosheet Gate-All-Around Transistor to Enable Scaling Beyond FinFET – VLSI Symp 2017

Junction-Less (Nanowire) Devices





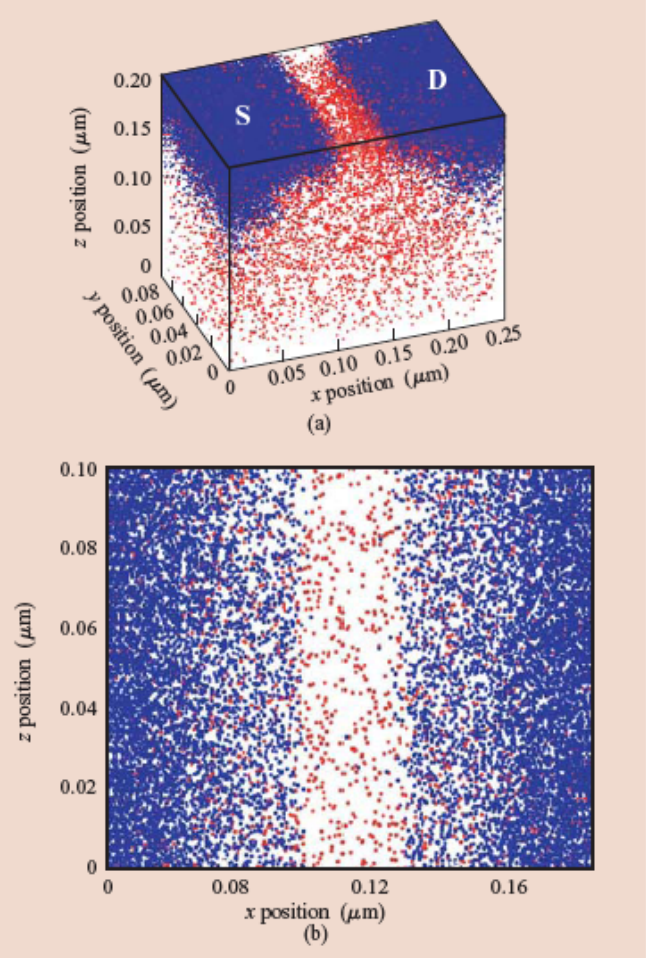




from: J.P. Coling et al, Nanowire transistors without junctions
NATURE NANOTECHNOLOGY. Vol 5. March 2010

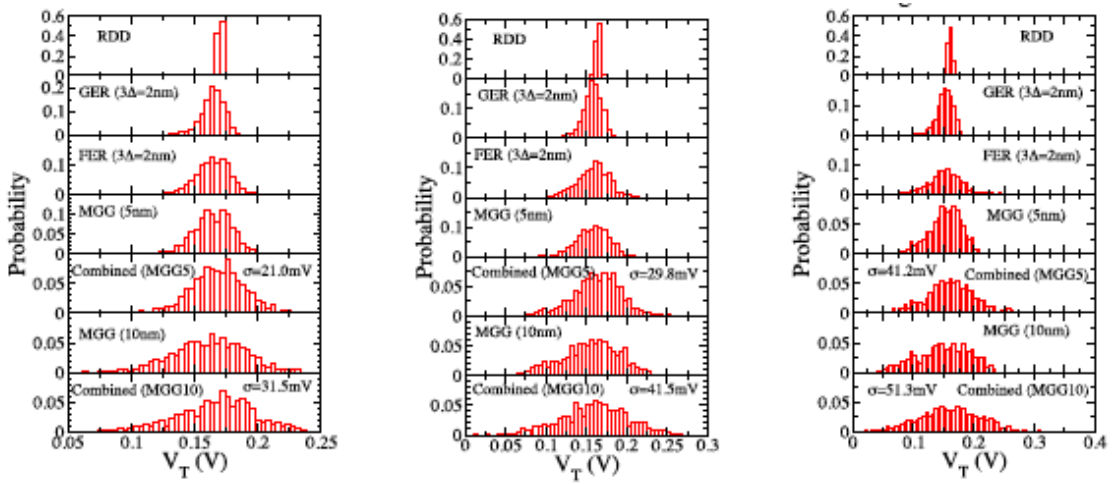
from: Toshiba, Silicon Nanowire Transistor for Ultralow-Power LSIs
in https://www.toshiba.co.jp/rdc/rd/fields/11_e10_e.htm

Atomic Scale Variability



Atomistic view of dopants in 50nm transistor

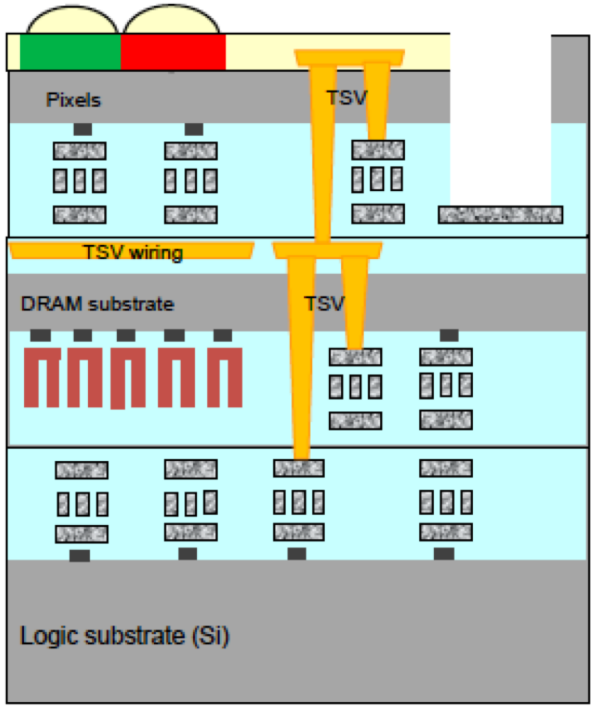
from K. Bernstein et al., IBM J. Res. & Dev. Vol. 50 No. 4/5, 2006

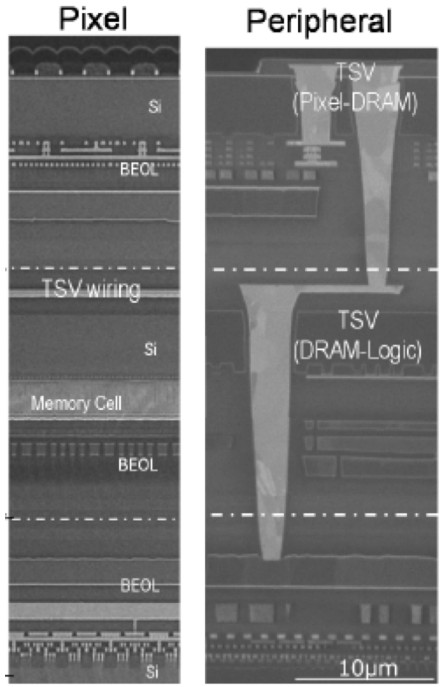


Distribution of Vt on three generations of FinFETS, 20nm, 14nm, 10nm

from X. Wang et al., IEDM 2011,

3D technology





3 um

90 nm sensor tech

30 nm DRAM tech

40 nm logic tech

from: H. Tsugawa et al., - Sony - Pixel/DRAM/logic 3-layer stacked CMOS imagesensor technology - IEDM 2017

How to consume less energy in computation

Less energy per computation

- Power consumption in digital circuits is determined by three factors:
  1. The energy necessary to charge/discharge the input of the next level of logic and the interconnecting wire
  2. The energy wasted by the switching device because of simultaneous conductance of the NMOS and PMOS devices during a transition
  3. The energy wasted by leakage currents through the transistors (the switches are unfortunately not "*ideal*") even in static conditions

Power consumption in (digital) chips

$$P = \frac{1}{2} C\, V_{dd}^2\, \alpha\, f + I_{leak} V_{dd} + \Delta\tau_{sw}\, I_{sc} V_{dd}$$

V_{dd}: $supply\ voltage$
α: $activity\ factor$
C: $load\ capacitance$
f: $switching\ frequency$
I_{leak}: $leakage\ current$
I_{sc}: $short\ circuit\ current$
$\Delta\tau_{sw}$: $fraction\ of\ time\ in\ sc\ mode$

Improving in energy saving

- Make devices smaller:
  - C decreases
    - … but up to a point as interconnect C becomes rapidly dominant and actually start to increase
  - V_{dd} decreases
    - … but also up to a point, as threshold voltage behavior is limited by intrinsic physics and not by technology
  - Something drastic is required to save energy!

Any better transistor?

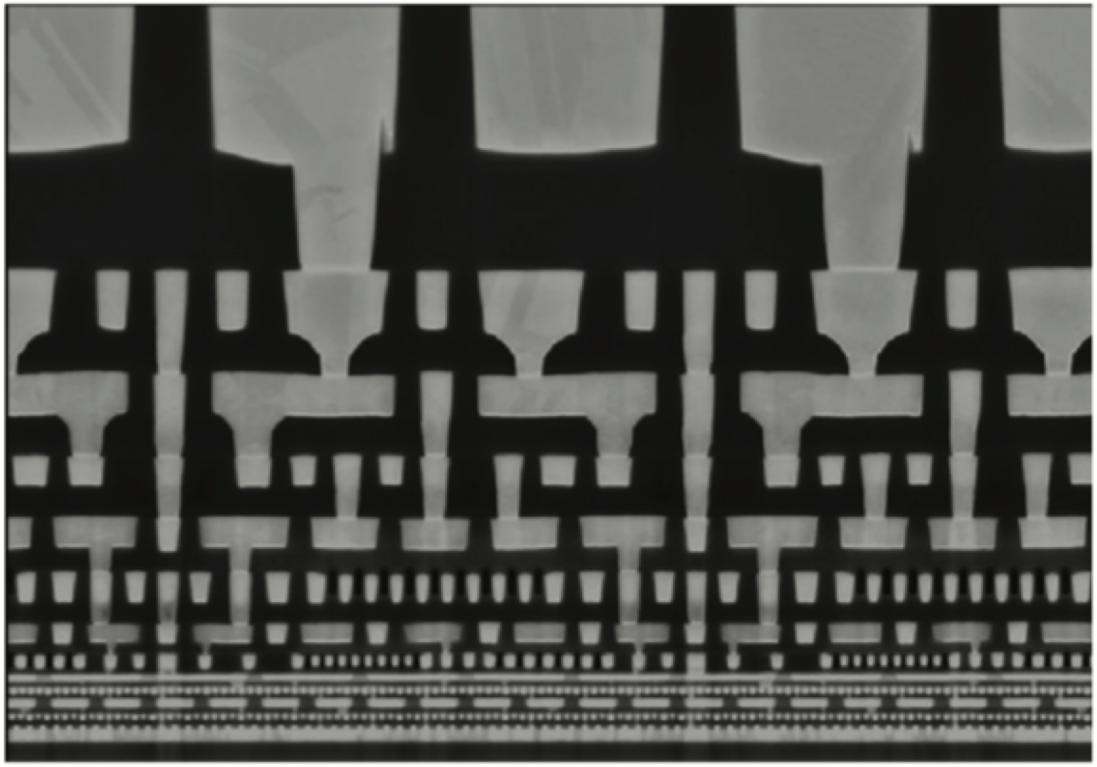
Today's devices make transitions around their threshold voltages which are determined by some fundamental physics related to the Boltzmann constant. Such devices require at least an input voltage change of 60 mV to increase their current by a factor of 10.

Devices with "very steep" transition regions between the OFF and the ON states are being researched, among these:

1. "Ferroelectric" (negative capacitance) transistors
2. Tunnel transistors
3. …

If available in the coming years these would lead to supply voltages in the 100-200 mV region and a power saving of about one order of magnitude

Who is more important: Transistors or wires?

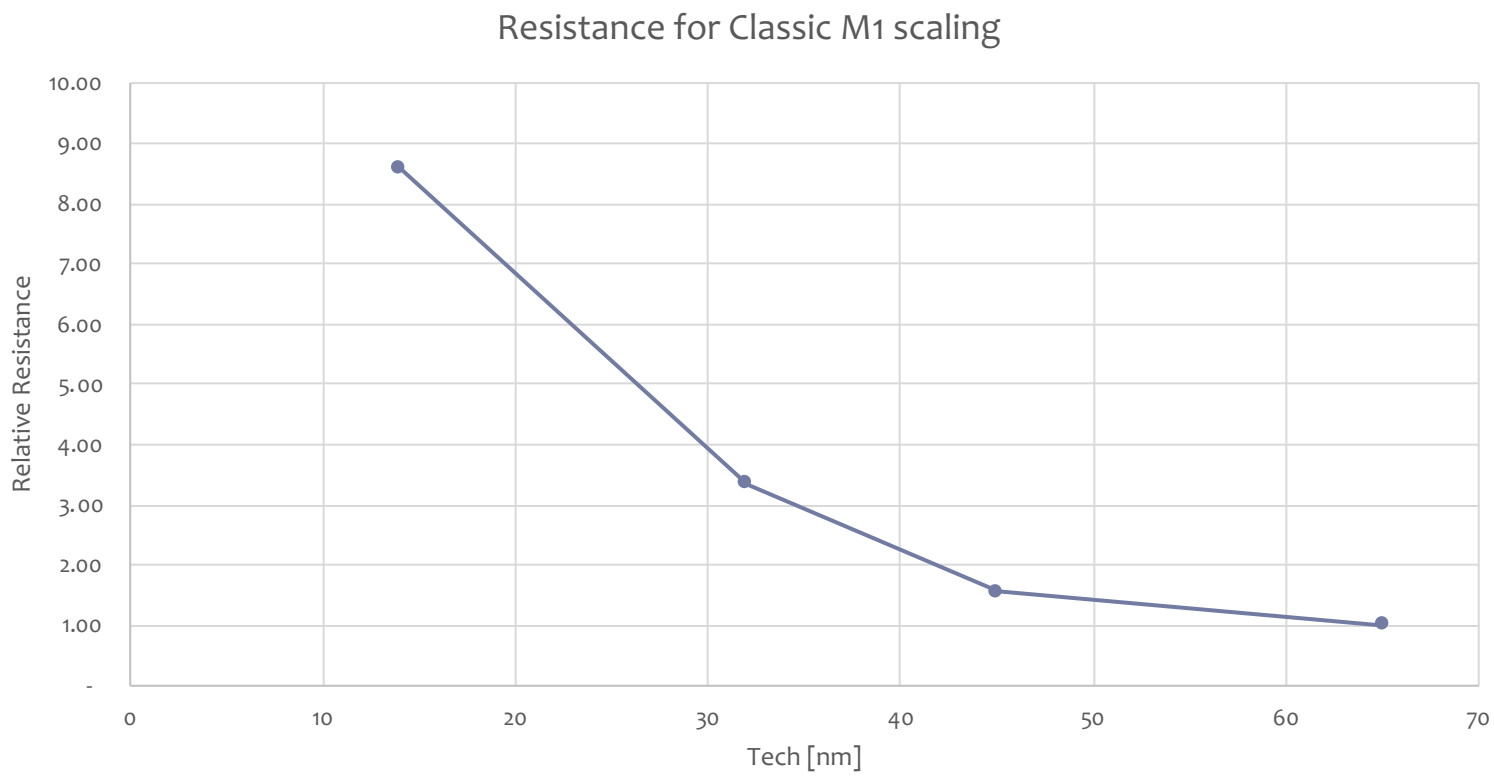


Metal	Pitch [nm]	Metal tickn.[nm]
0	56	40
1	81	42
2	73	40
3	76	37
4	80	75
..		
11	1000	1000

A 14 nm FINFET process metal stack

from K. Fischer – Intel – Low-k Interconnect Stack with multiple-layer gap.., IITC Conf. 2015

Wire resistance in “classical” scaling



Ultra-scaled metals

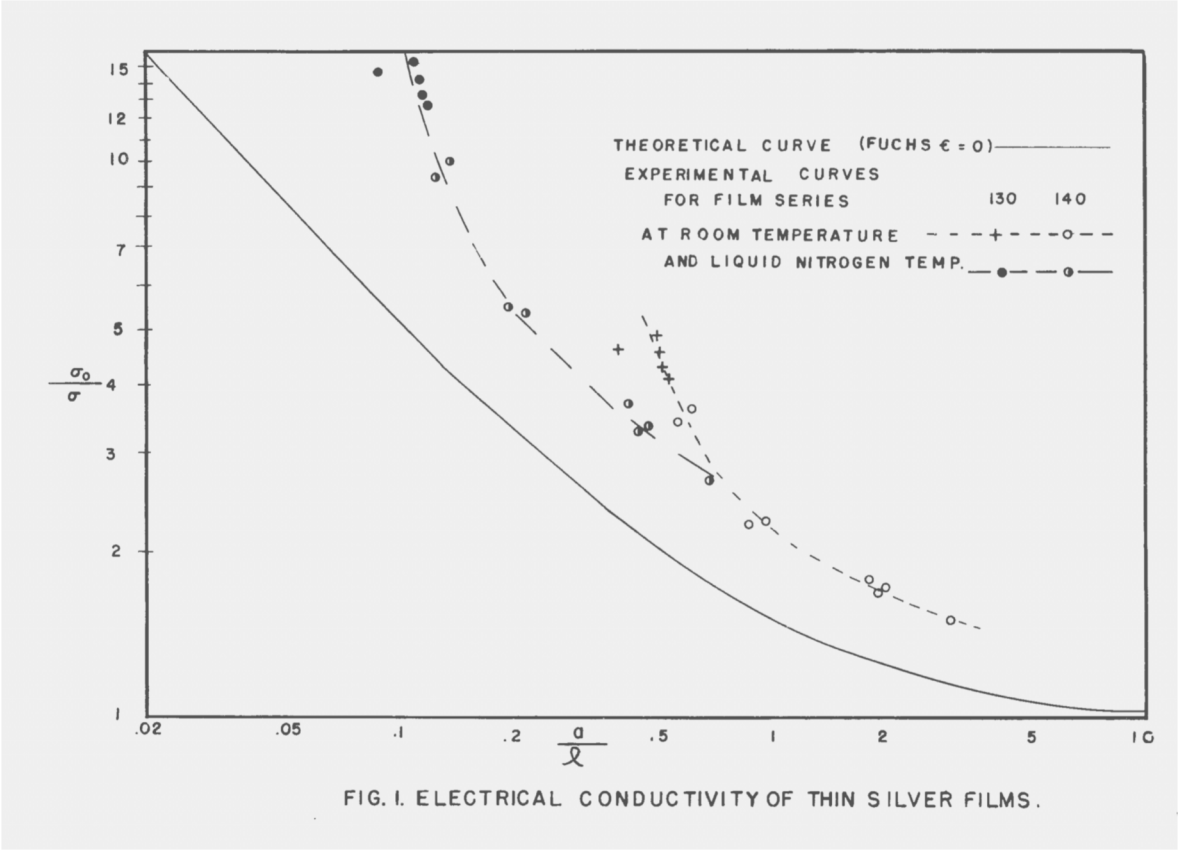
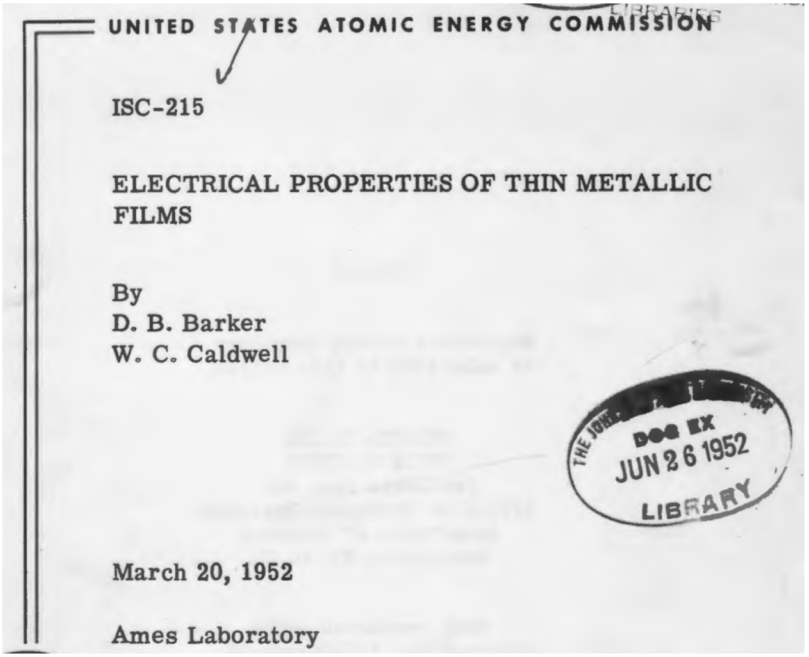


FIG. I. ELECTRICAL CONDUCTIVITY OF THIN SILVER FILMS.



UNITED STATES ATOMIC ENERGY COMMISSION

ISC-215

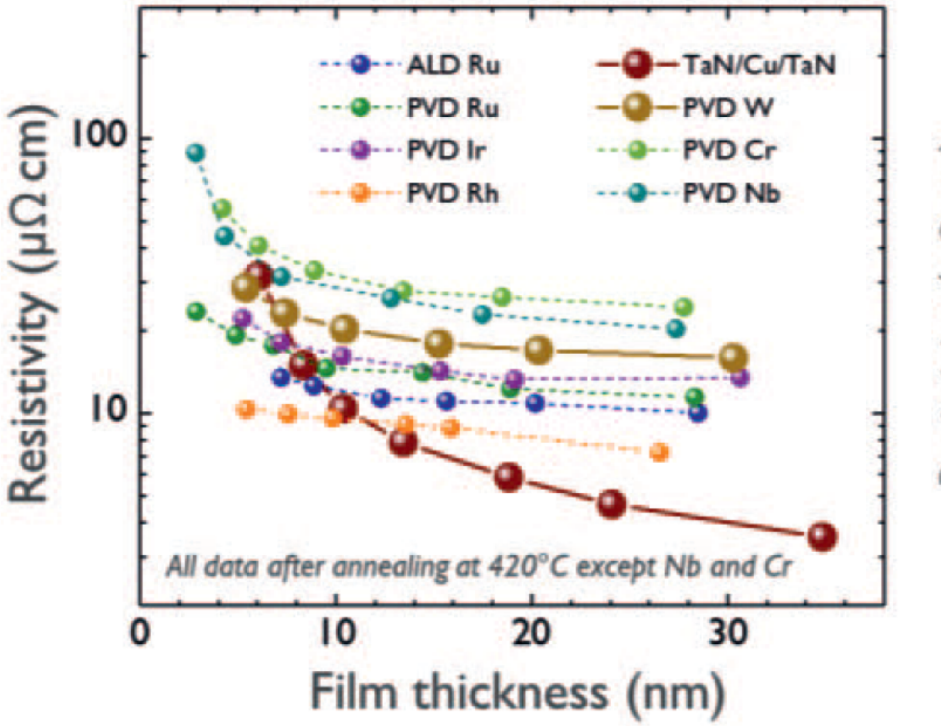
ELECTRICAL PROPERTIES OF THIN METALLIC FILMS

By
D. B. Barker
W. C. Caldwell

March 20, 1952

Ames Laboratory

Ultra-scaled metals (2)



from K. Croes, IEDM 2018

Summary on technologies

- Moore's Law worked for more than 50 years with spectacular results
- But fundamental limitations are being encountered in many areas
  - Thinness of materials
    - Leakage currents
    - Resistances (and Line Edge Roughness)
    - Difficulties in fabrication
    - Random dopants distribution
    - …
  - Cost of fabrication
- Another factor of 10 possible with 'brute force scaling'?
  - Hard to bet, but probably not
- Fundamental research is nevertheless very active to develop new materials that allow switches to be built through new phenomena

What can you do if you master microelectronics?

Possibilities

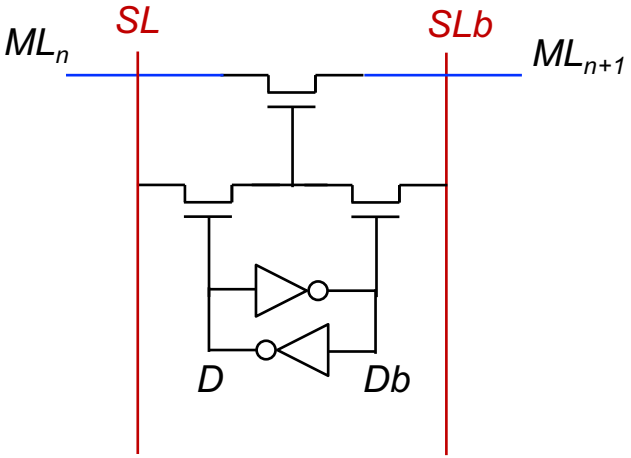
- Increase sensor area/volume
  - A PET scanner is bigger than a dental imaging machine
  - And if you want to equip 500-1,000 m^2 of silicon, you better bring the cost/m^2 down
- Resolution
  - Space
  - Signal amplitude
  - Time
- Functionality
  - Combined space and time information
  - Add redundancy for robustness to ambient-generated errors
- Intelligence (not AI, sorry)
  - Feature extraction

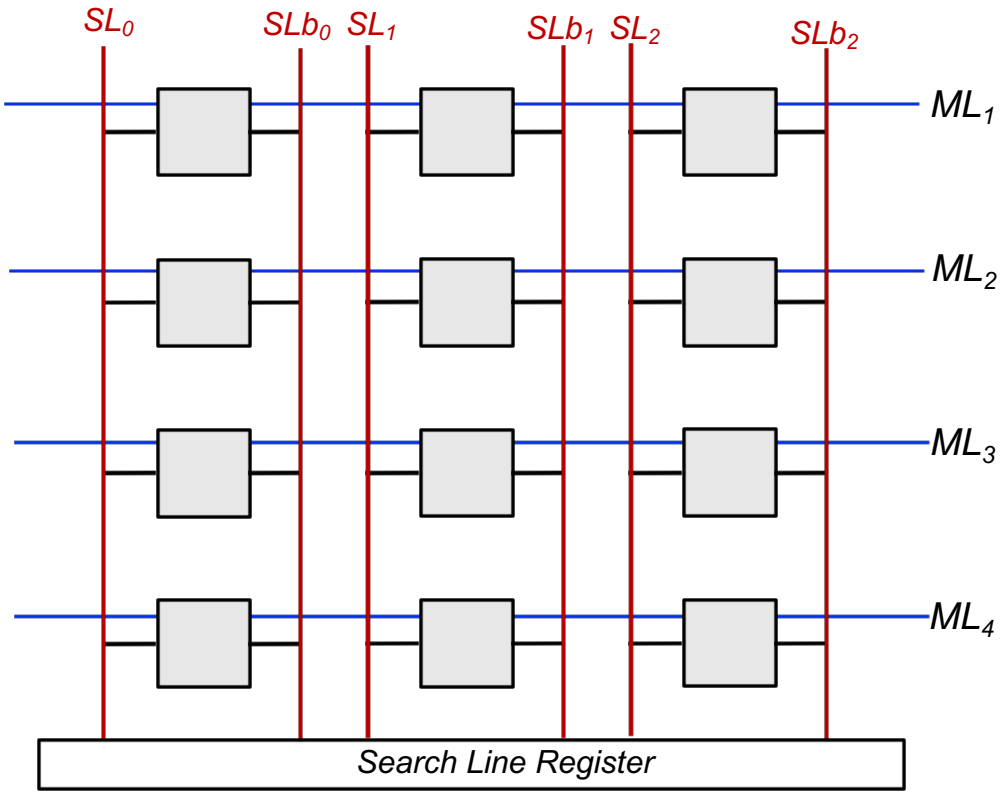
Calibration point

- Are 500 m2 of silicon really that much?
  - One 200 mm diameter wafer gives a ~ 14x14cm^2 sensor
  - 500 m^2 corresponds to about 25,500 wafers of 200mm
    - [is a 5 years construction time ok?]
- Today one of the largest imaging sensors manufacturer with about 25% of the world market is producing about 80,000 200mm wafers/month
  (ref: http://www.sony.net/SonyInfo/News/Press/201502/15-009E/)

Special functionality

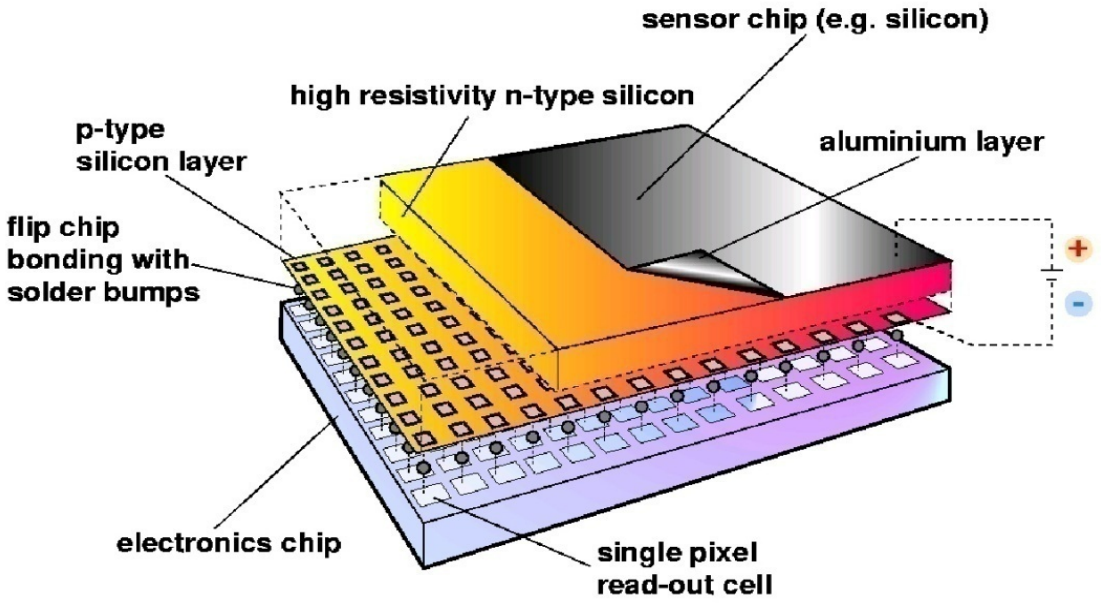
Associative memory

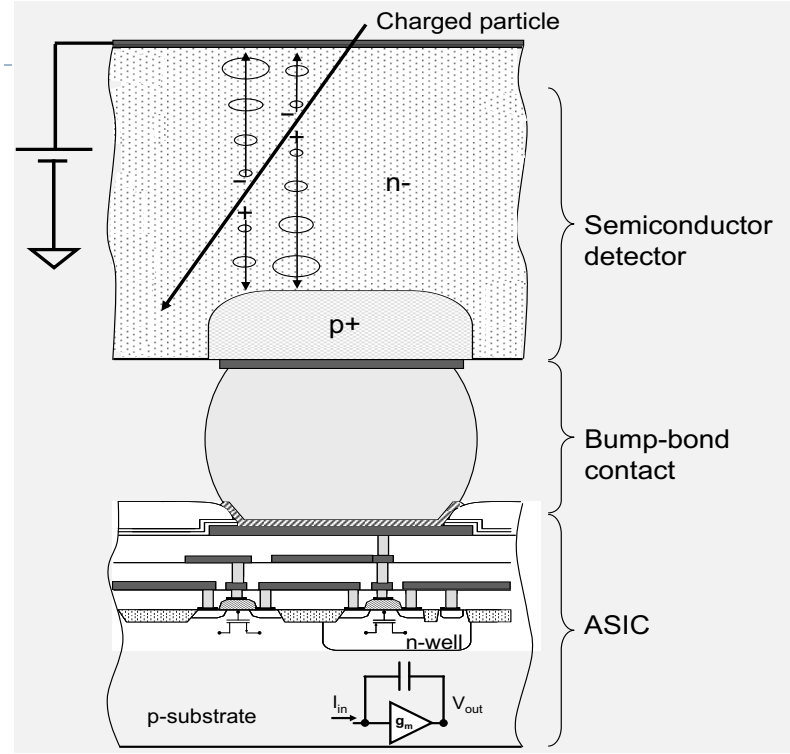




More Resolution

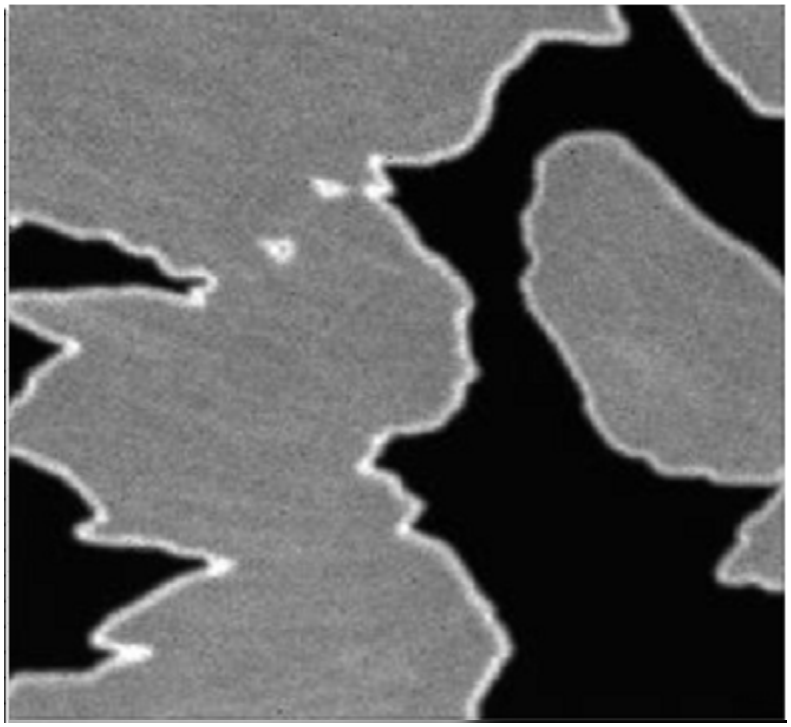
Hybrid Silicon Pixel Detectors

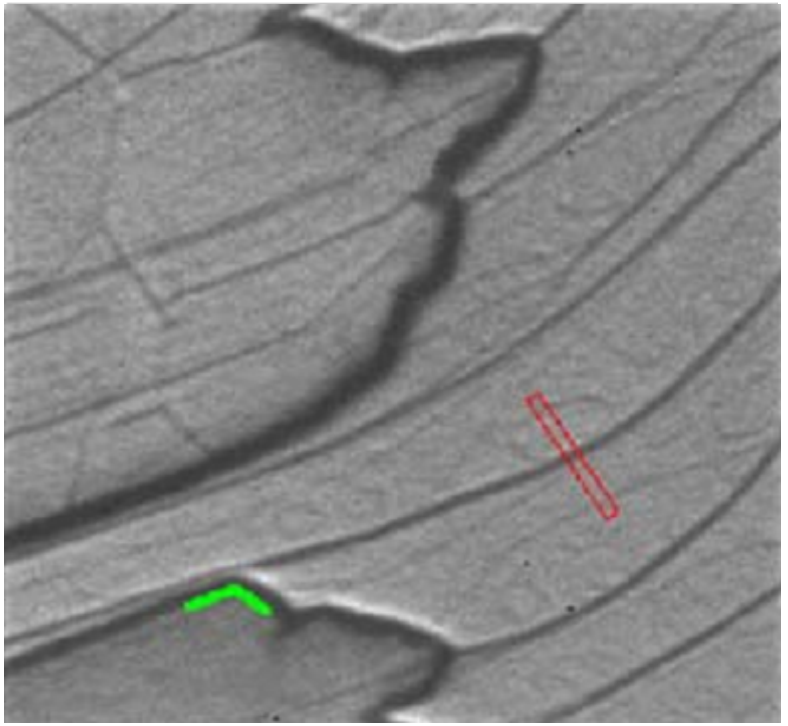




- *Fill factor is 100%*
- *Fully depleted sensor*
- *Extremely high SNR easy to reach – "noise free imaging"*
- *Sensor material can be optimized for different applications*
- *CMOS high density can be used allowing on-pixel signal processing*

Better image resolution: more of the same





Medipix2 Images

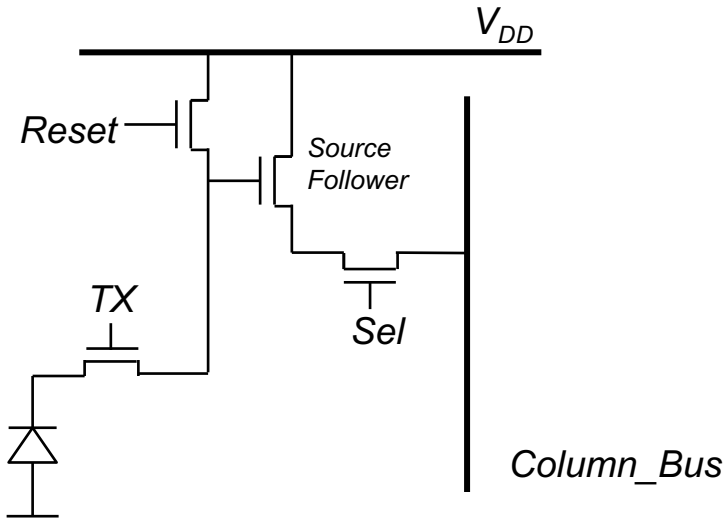
I. Sikharulidze, J-P Abrahams and co-workers
'Medipix2 applied to low energy electron microscopy', Ultramicroscopy 110 (2009) 33 – 35

More Functionality

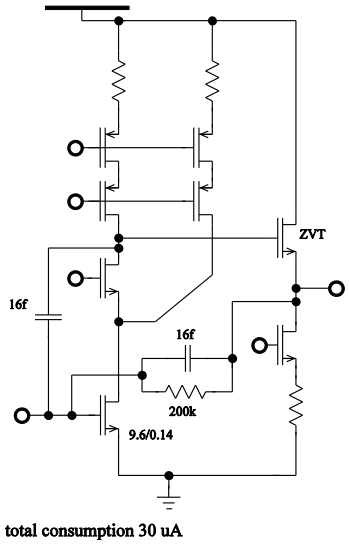
Comparison of HEP sensor with visual imager

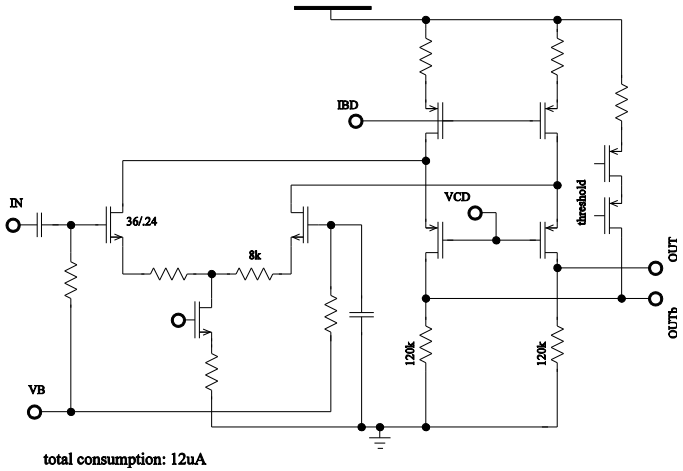
Feature	HEP Tracker	High Volume Visual Imager
Data rate	40 M ev/sec	~100 ev/sec
Spatial resolution	~100 um	~1 um
Time resolution	< 1 ns	~ 1 msec (but higher for TOF sensors)
Surface	10-100 m^2	10 cm^2
Smallest primary signal	> 100-1000 e^-	Few e^-
Power / cm2	<0.1 W	0.1 W
Manufacturing	Monolithic and hybrid	Monolithic and hybrid (stacked)
Radiation environment	Yes	No
Micro-Technologies used	Advanced	Very advanced
Assembly technologies used	Advanced	Very advanced

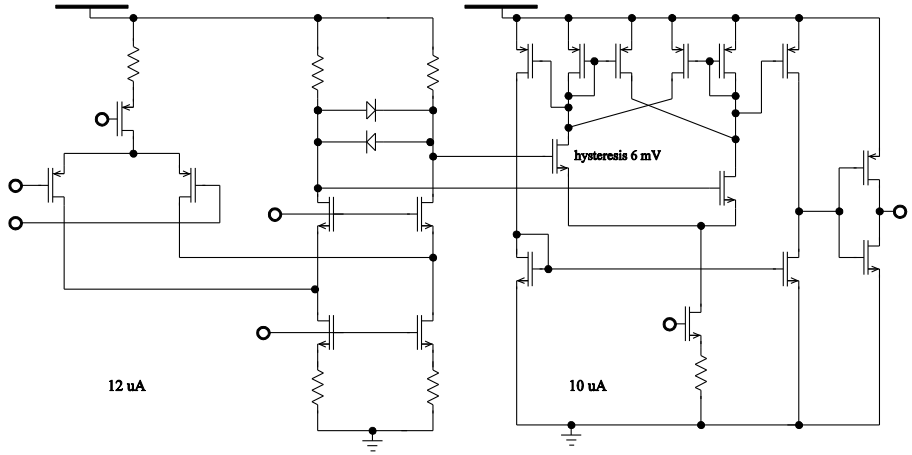
Visible imagers: CMOS 4-T basic structure



HEP Pixel FE



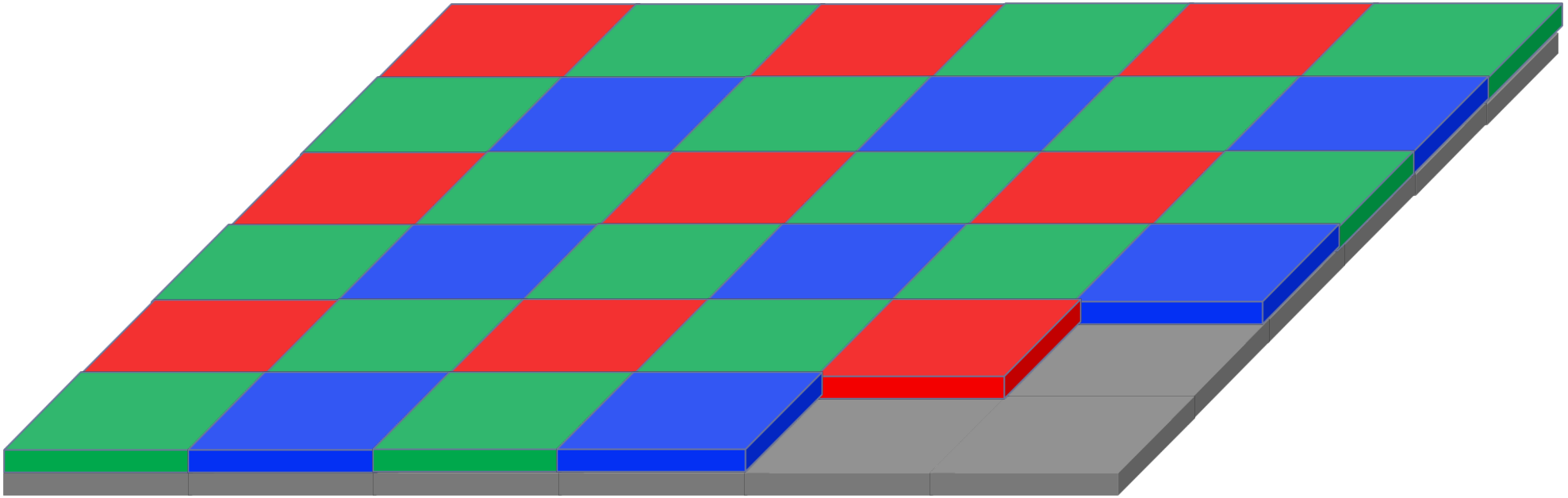




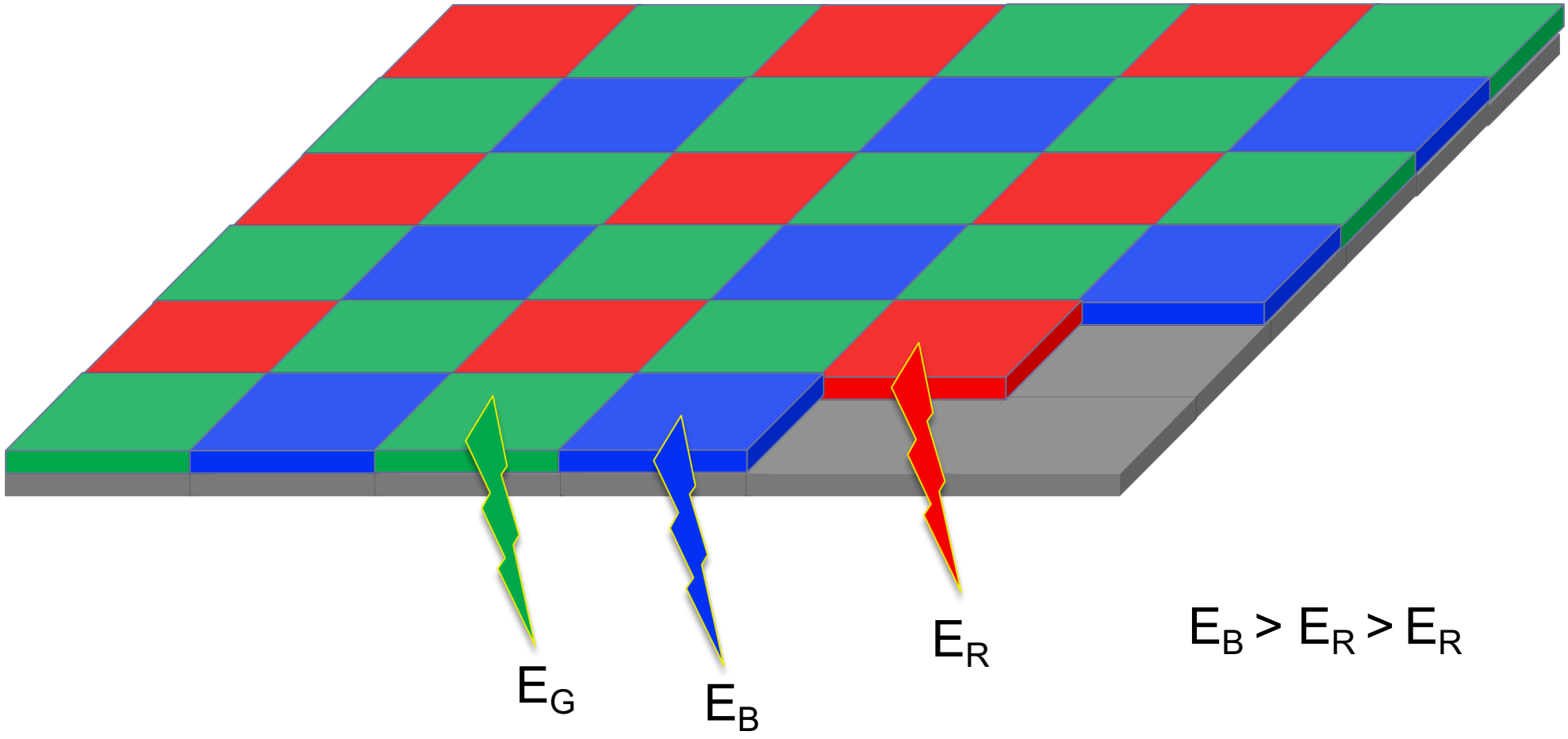
FE: Preamp + Shaper + Discriminator for CMS Macro-Pixel, 65nm CMOS, courtesy of J. Kaplon

Adding colors

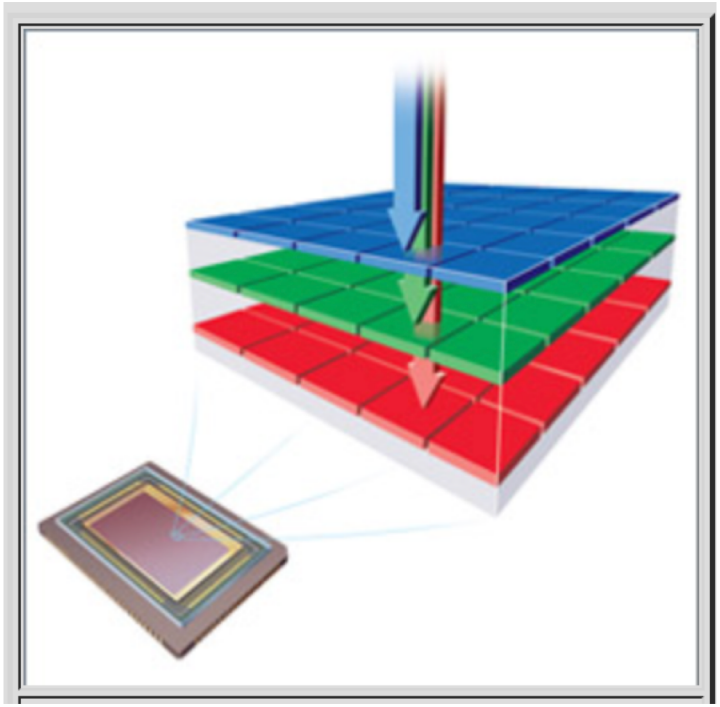
Bayer Pattern in Photography



Bayer Pattern

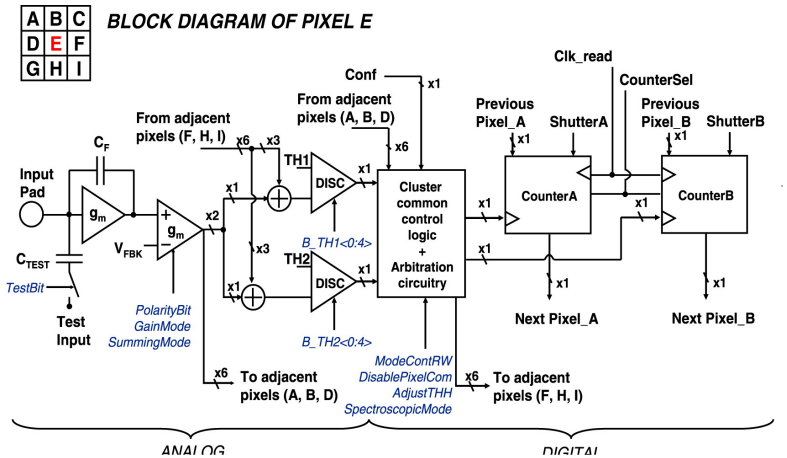


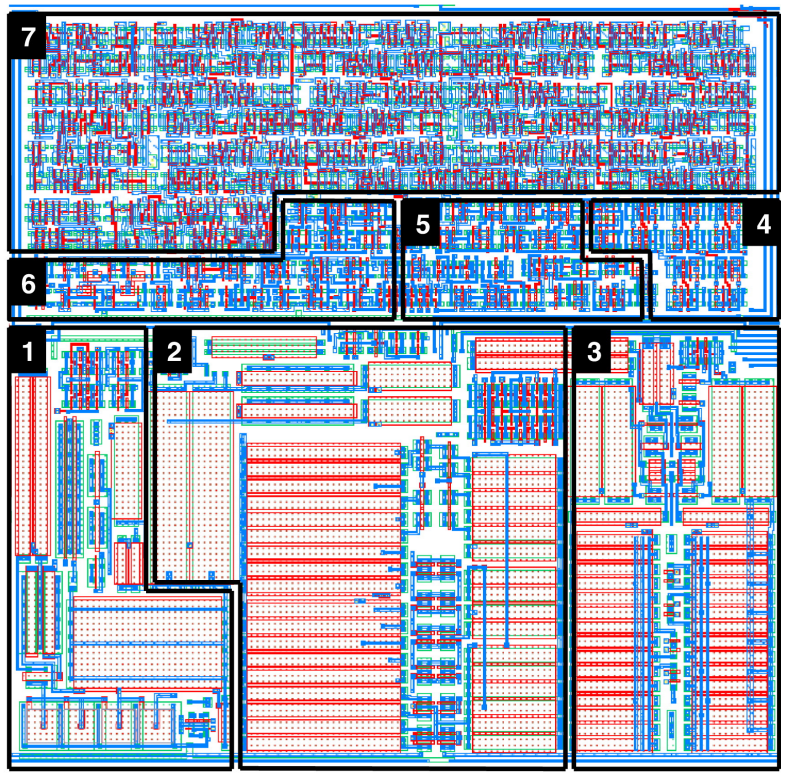
Energy(i.e. color) discrimination by penetration



from Foveon: http://foveon.com/article.php?a=67

Medipix3

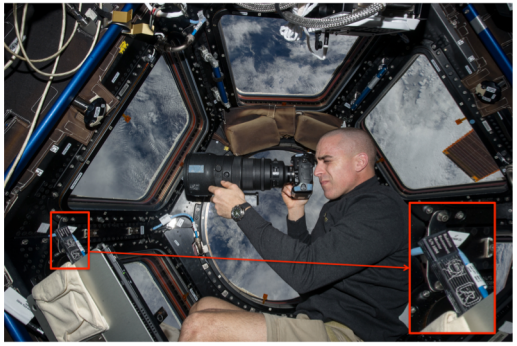


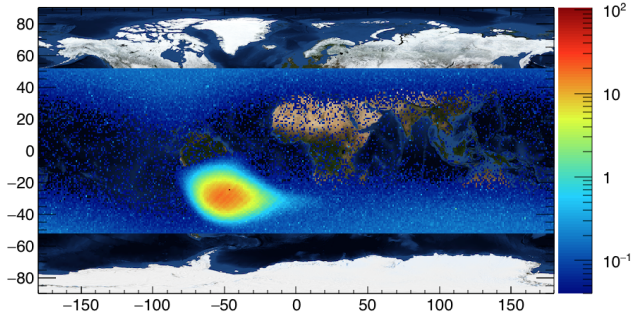


55 µm

Some applications of Medipix and Timepix

Space weather and dosimetry

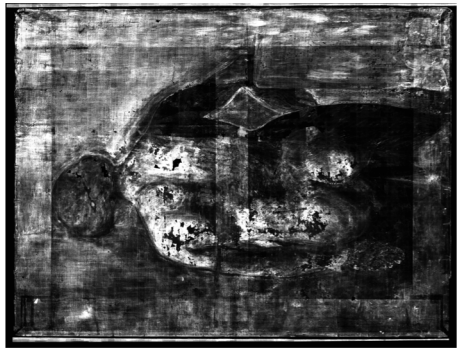




Mixed field radiation monitoring and dosimetry

NASA/Univ. Houston/IEAP Prague

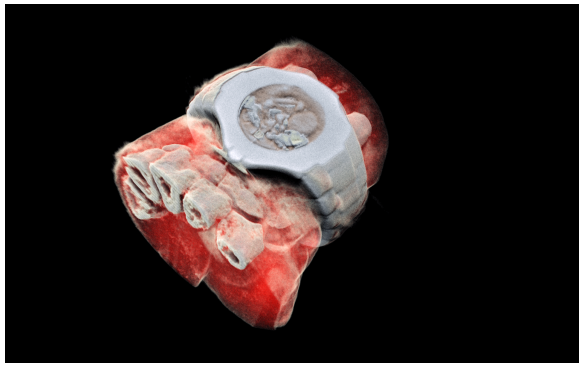
Cultural heritage studies



Investigation of art using colour X-ray imaging

InsightArt, Prague

Medical colour X-ray imaging

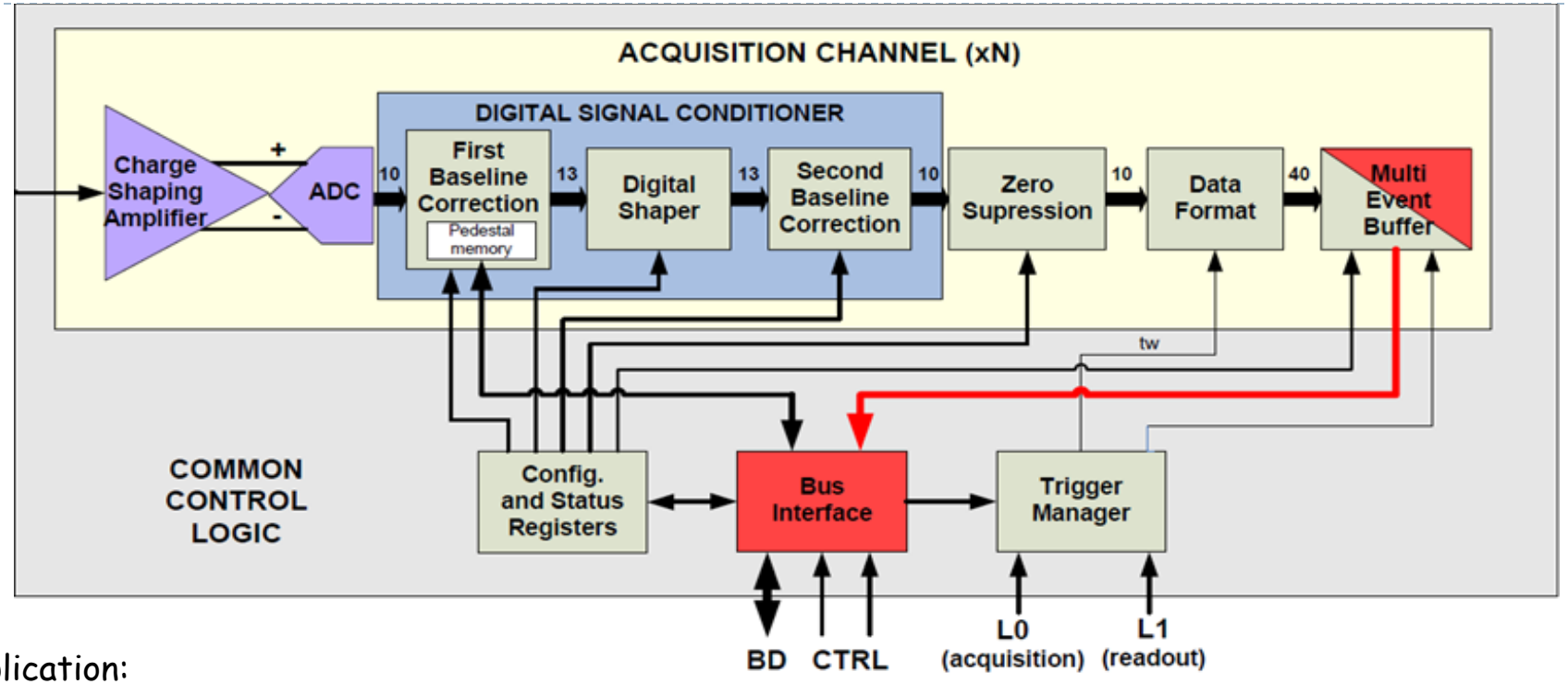


World first colour X-ray image of a living human

- *Clearer images*
- *Lower dose*
- *Material separation*

MARS Bioimaging, NZ

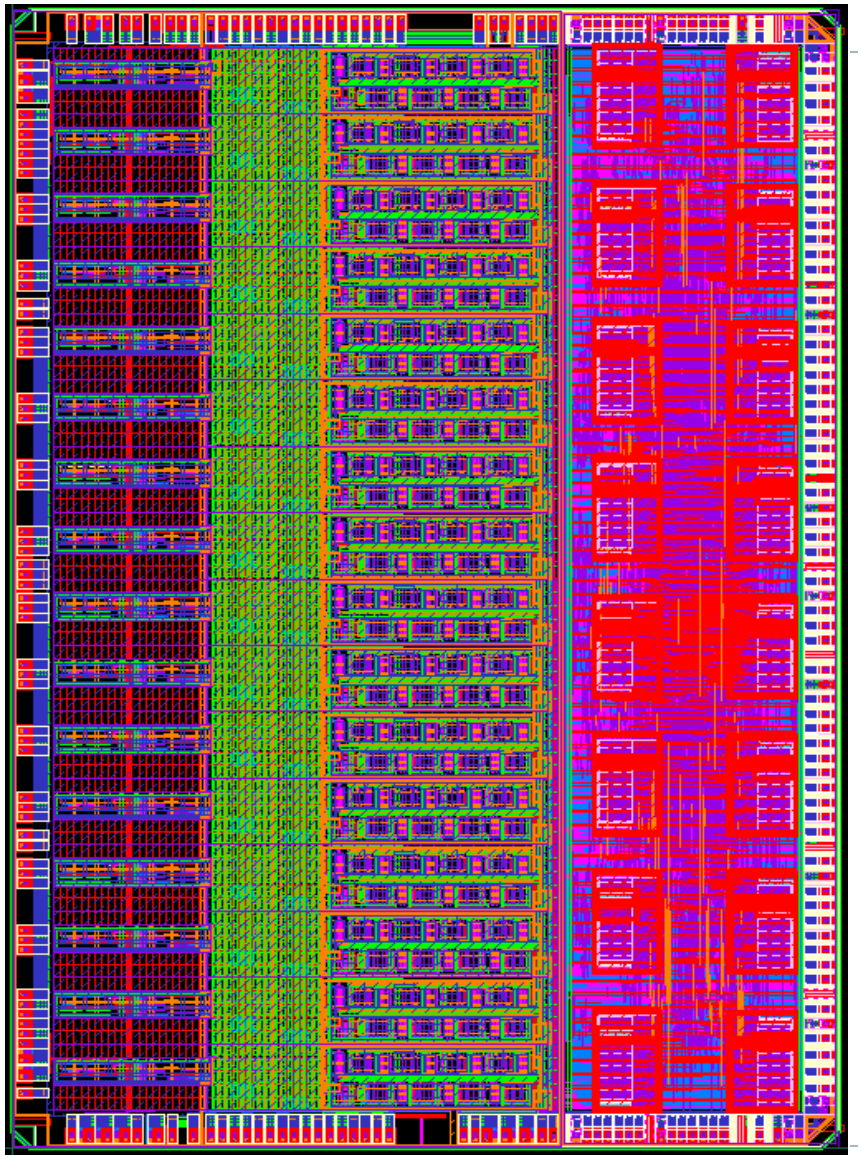
S-ALTRO: a fully integrated DSP per channel



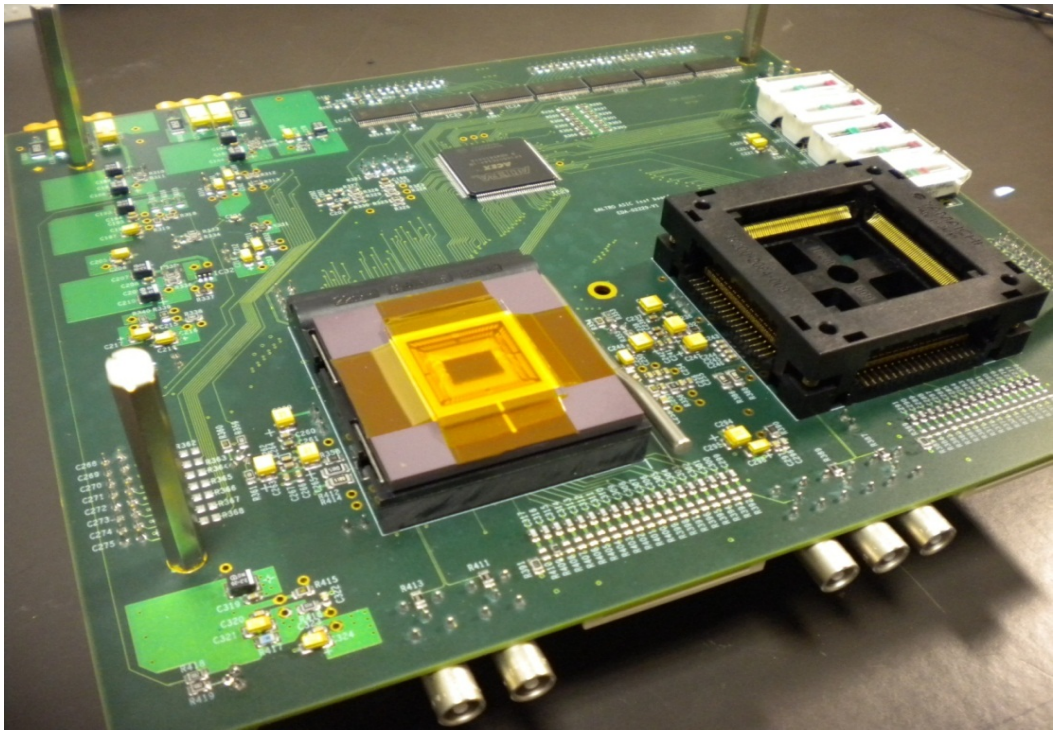
Courtesy of M. De Gasperi, CERN

- Application:
  - readout of the Linear Collider TPC
  - tests of GEM and MicroMegas.
- Technology: CMOS 130nm with 8 metal layers.
- ADC: 10bit, 40MHz sampling
- Advanced DSP capabilities (removal of systematic patterns, baseline offsets and fluctuations, digital signal shaping to correct signal tails or distortions) enable efficient zero suppression.

The 16-channel S-ALTRO Demonstrator

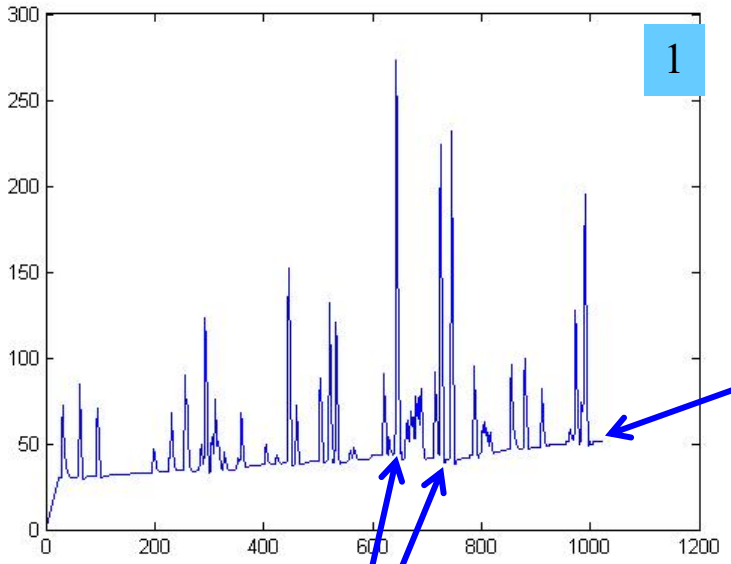


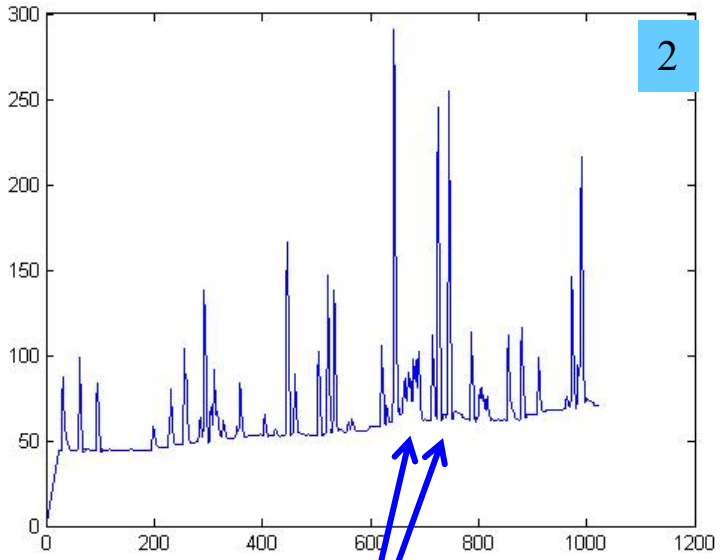
Size: 5750um x 8560um

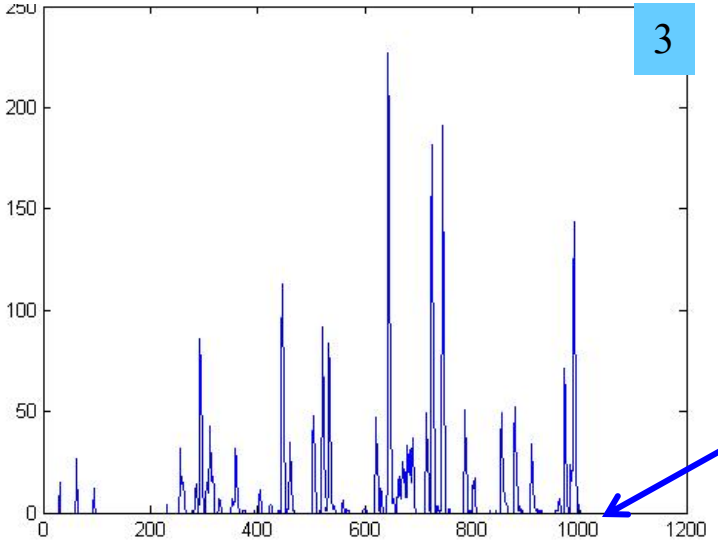


Courtesy of M De Gasperi, CERN

Digital Filtering with S-ALTRO







Baseline Drift

Undershoots

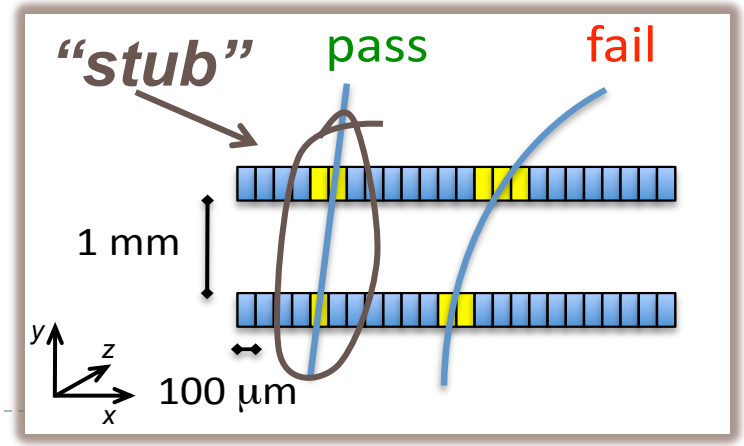
Undershoots Removal

Baseline Drift Removal

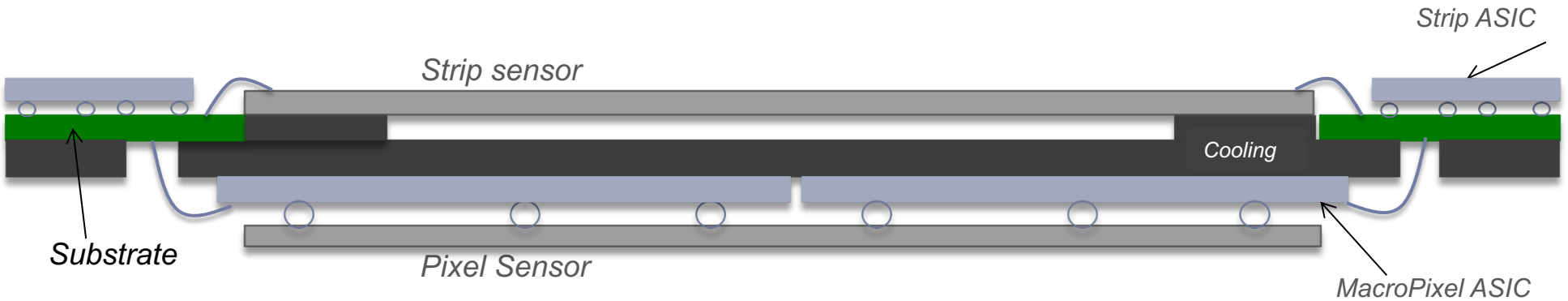
Courtesy of M De Gasoeri, CERN

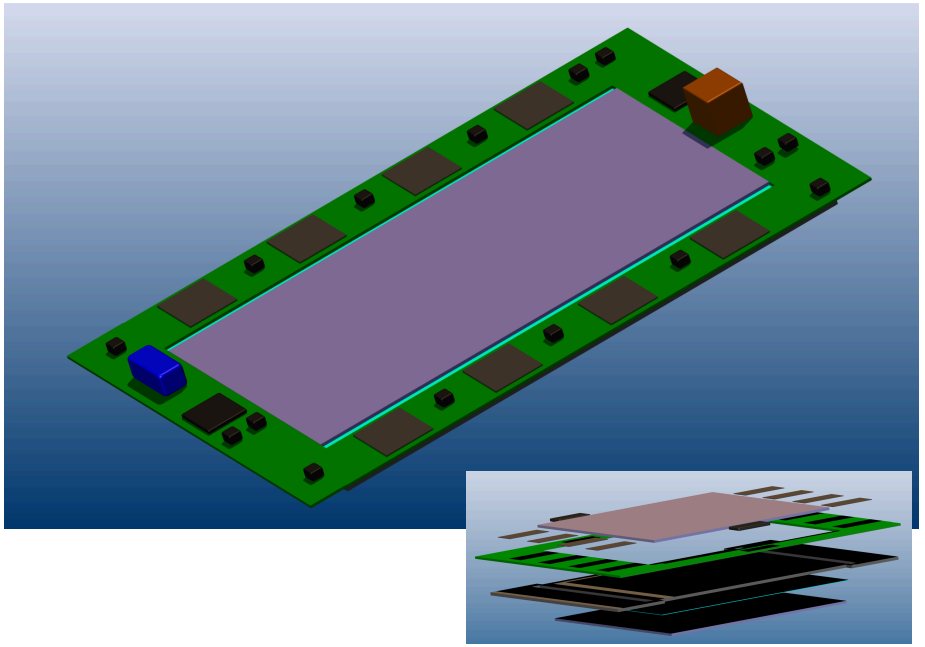
Feature extraction in tracker

- General concept
  - Silicon modules provide at the same time “Level-1 data” (@ 40 MHZ), and “readout data” (@ 100 kHz, upon Level-1 trigger)
  - Level-1 data require immediate rejection of low-p_T (i.e. slow) tracks
    - To reduce the data volume, and simplify track finding @ Level-1
      - Design modules with p_T discrimination (“p_T modules”)
  - Correlate signals in two closely-spaced sensors
    - Exploit the strong magnetic field of CMS

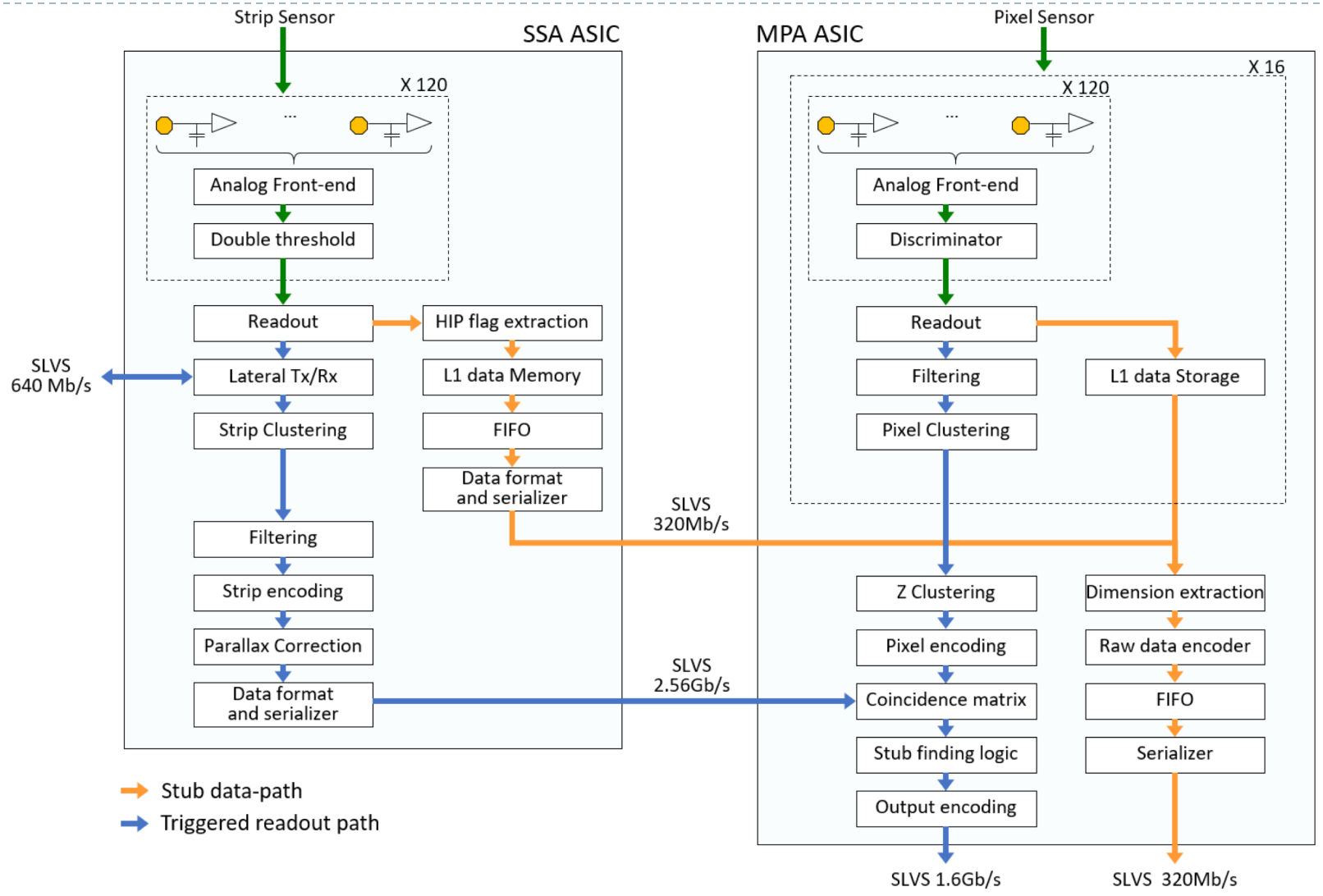


Simplified cross-section





“Stub” Extraction in MPA-SSA chips



“Intelligent” detector: what is it?

- Currently detectors provide:
  - Points in space
  - Energy in space
- But physicists actually want:
  - Tracks
  - Momentum
  - Energy/particle
- The CMS tracker is the first detector that can provide directly and “promptly”:
  - Momentum discrimination
  - Direction “vectors”

Concluding

(The Sermon)

Final observations

- Detectors and data acquisition systems can be substantially improved or even totally revolutionized with more functionality that can be added through integrated custom electronics
  - Intelligent detectors with:
    - > 10 m^2 surface covered entirely by pixels
    - > 100 m^2 trackers
    - ~1,000 m^2 calorimeters
  - are now technically possible (and within budget!)
- Limitations?
  - No technical show-stopper (provided proper design organization is available!)
    - Speed, size and power of CMOS @ 65-28 nm is today often sufficient, but further miniaturization will not hurt
    - Power is to be controlled (exactly as for most commercial applications)
  - But we need to learn how to manage:
    - High cost of modern advanced processes
    - Complexity of design and associated high risk of failure

Conclusions

- Powerful technologies and tools are here today, you have to invent how to use them to create new instruments.
  - Local computational power can be implemented with
    - Low power microelectronics (i.e. a commercial technology)
    - and imagination (i.e. YOU)

- If you are at this school, you have already developed a sense of gratification and pleasure by ”creating” new systems (for system designers), programs (if you mainly use “computers”) and new firmware (FPGA designers).

- *ASIC design can add a new dimension of “creativity” to your bag of tools.*

THANK YOU!