Custom In-Lab Temperature Control for the RD53 Chip

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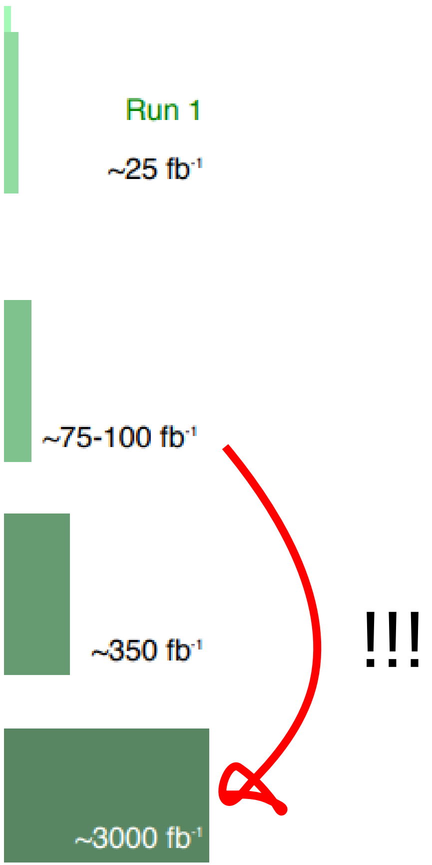
Roadmap

Integrated Luminosity

2009		LHC startup, √s 900 GeV
2010		
2011		√s=7+8 TeV, L~6x10[33]cm[-2]s[-1],
2012		
2013	LS1	Go to design energy, nominal luminosity - Phase 0
2014	LS1	
2015		
2016		√s=13~14 TeV, L~1x10[34]cm[-2]s[-1],
2017		
2018	LS2	Injector + LHC Phase I upgrade
2019		
2020		√s=14 TeV, L~2x10[34]cm[-2]s[-1],
2021		
2022	LS3	HL-LHC Phase II upgrade:
2023		
...		
2030?		√s=14 TeV, L~5x10[34]cm[-2]s[-1],

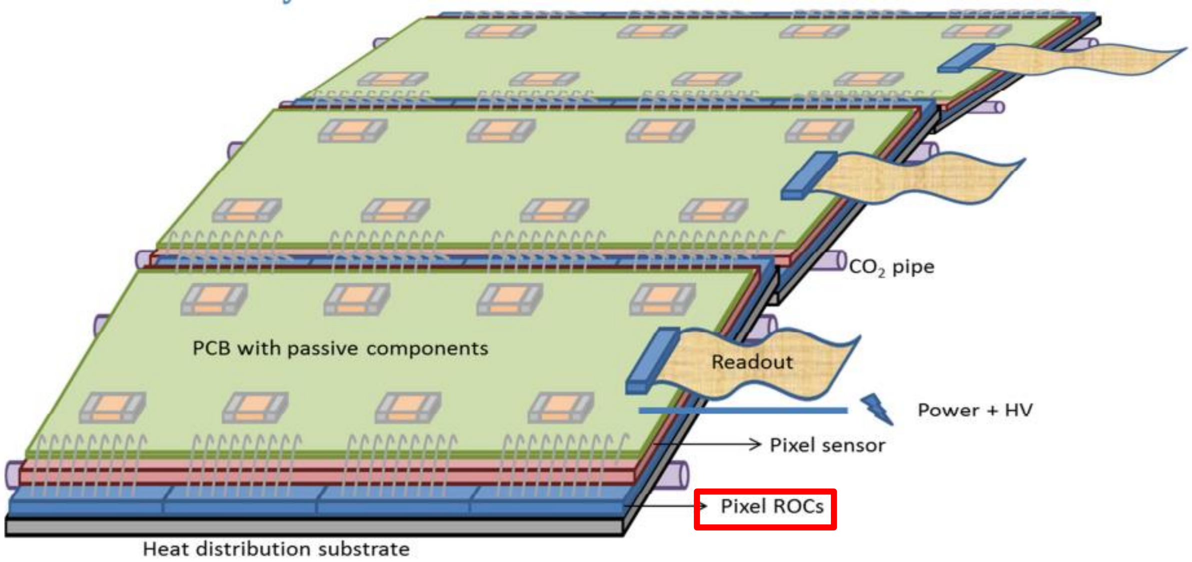


Complete Overhaul of Si Trackers

- Located in the innermost layer
- Si detectors track paths of charged particles.
  - How will they be affected by the upgrades?
    - Must be completely replaced in phase II upgrade!
    - In addition, phase II tracker will support:
      - Spatial resolution x4
      - Radiation dose x2 (Hostile!)
      - Hit rate x7
      - Trigger latency x0.2
      - … and more

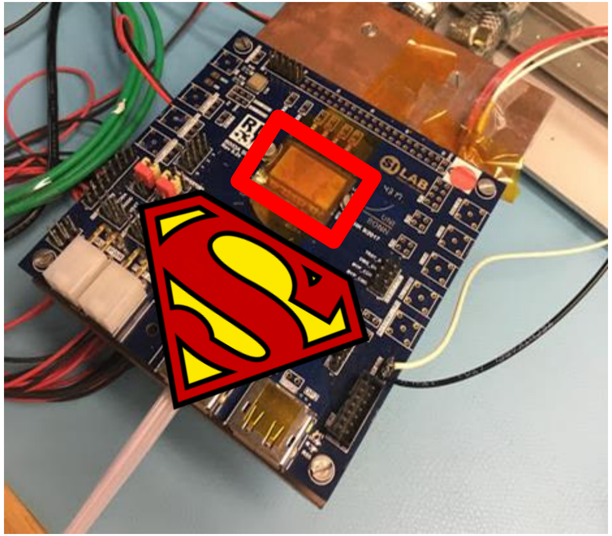
Immense Challenge for the Read-Out Chip (RoC)

- Spatial resolution x4
- Radiation dose x2 (Hostile!)
- Hit rate x7
- Trigger latency x0.2
- … and more



- The RoC faces:
  - 100x higher readout rate!
  - Hostile radiation
  - … and more

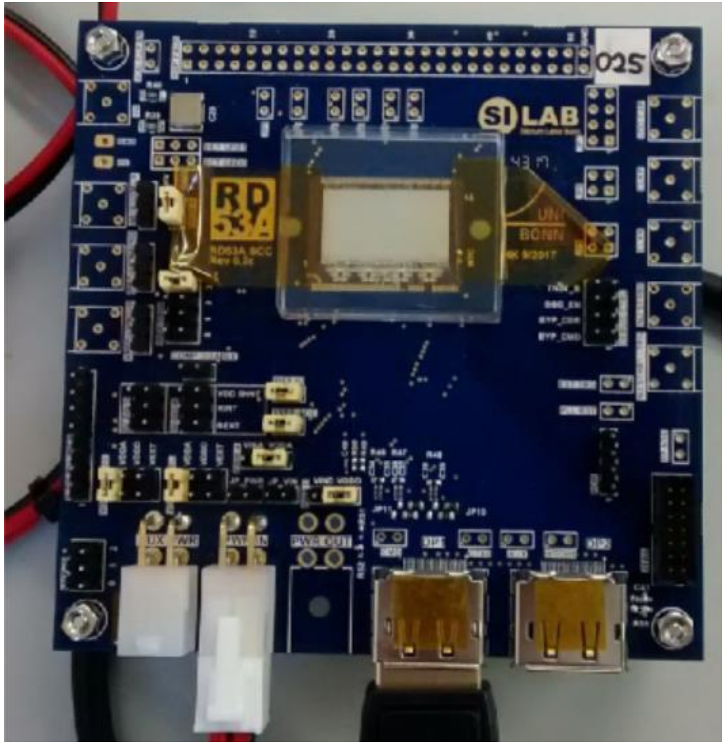
But Who Could do Such a Thing?!



Introducing: The RD53 Read-Out Chip (RoC)!

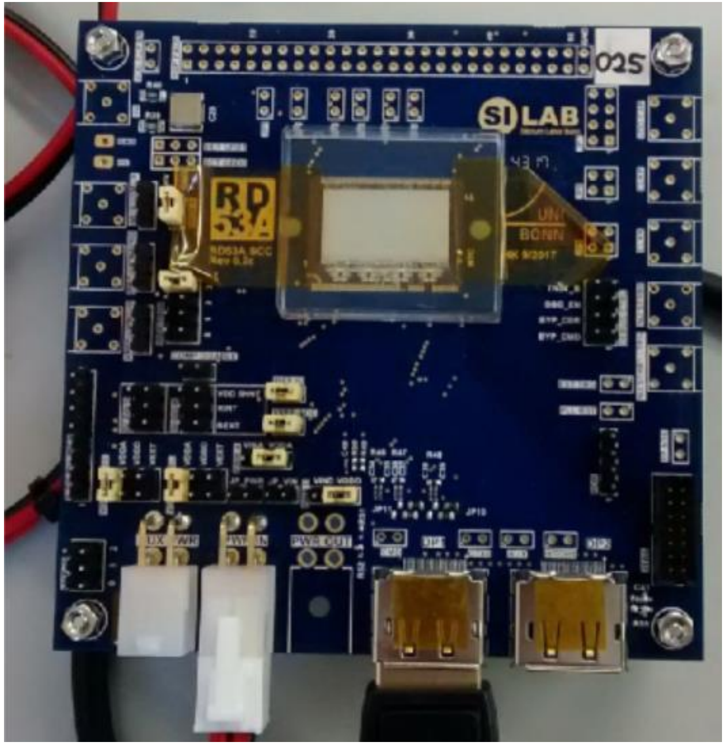
- 4 years of R&D to reach this point
- Able to handle extremely high hit rates, (3GHz/cm^2), hostile radiation (1 Grad over 10 years), and a 100x higher readout rate compared to current experiment
- Now entering testing phase

Testing Requires Cooling



- The chip produces 2-8 W of heat
- Requires a heat sink to function
- Good practice: keep temperature a controlled variable!
    - ---> Implement a temperature control system

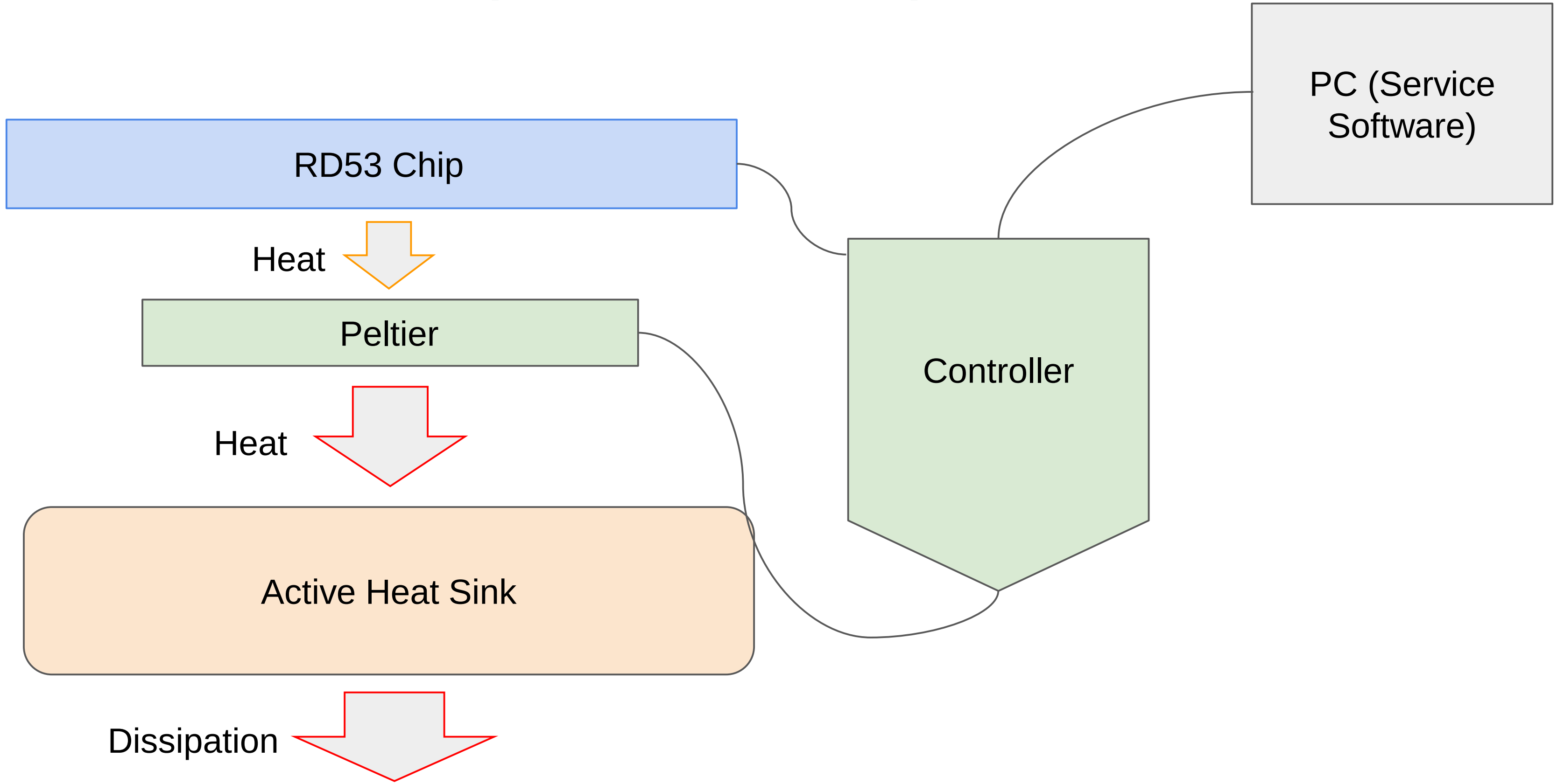
In-Lab Temp Control: Design Goals



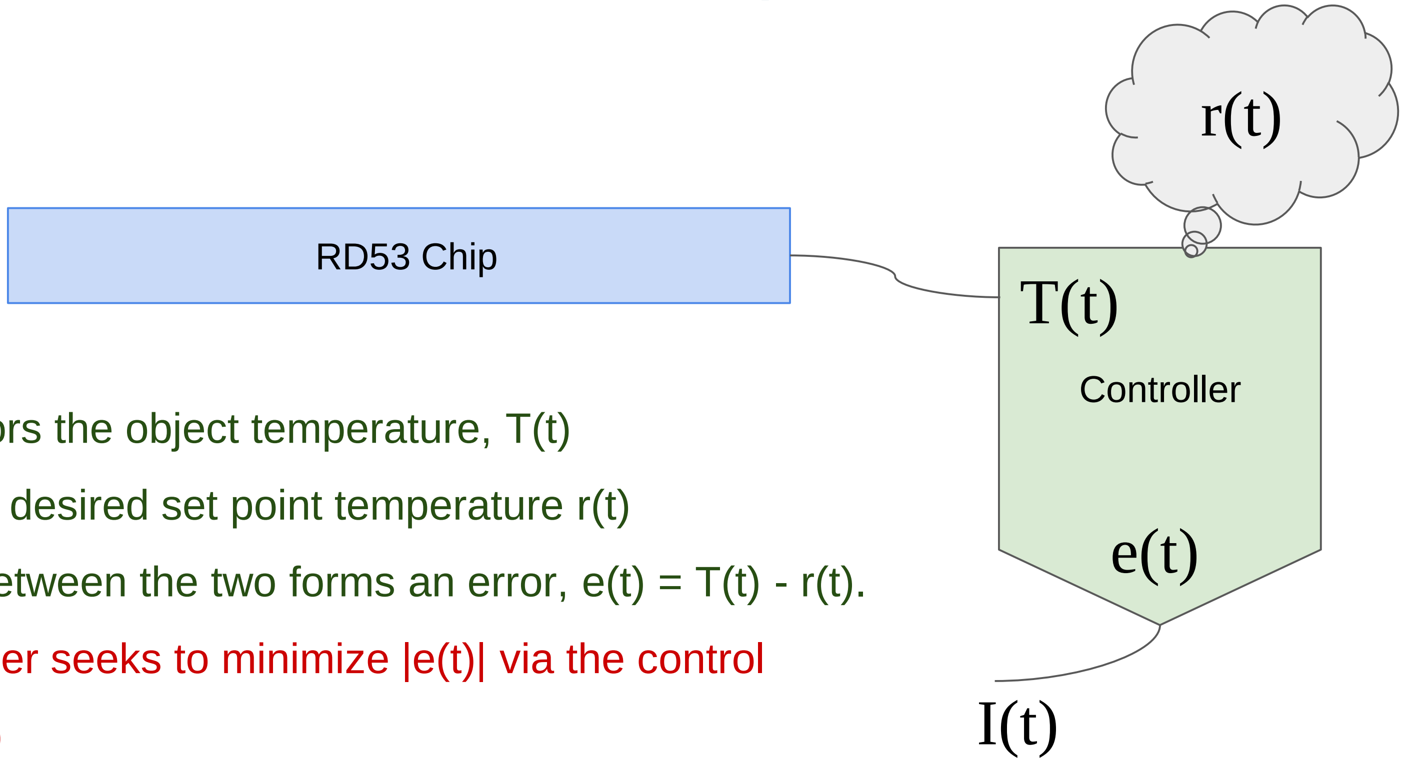
The system should be able to

- ☐ Remove up to 8W of chip power
- ☐ Operate at chip temperatures at or below room temperature with protection when around dewpoint.
- ☐ Most important point - Remain *stable* while within specified operating zones.
- ☐ Come to equilibrium quickly (<5 mins)
- ☐ Cool multiple chips (goal: 4)

Top-Level Setup

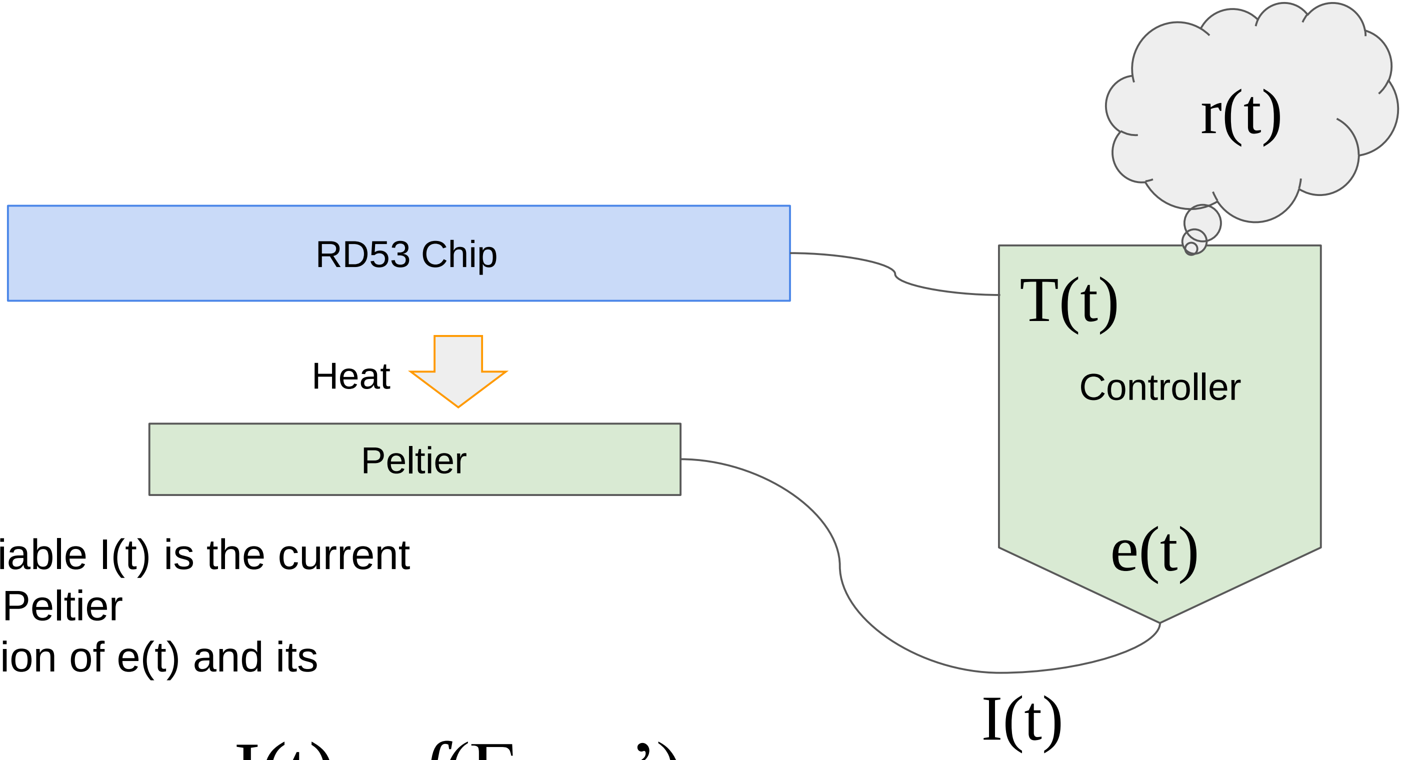


Control Process Principles



- Controller monitors the object temperature, T(t)
- Compares to the desired set point temperature r(t)
- The difference between the two forms an error, e(t) = T(t) - r(t).
  - The controller seeks to minimize |e(t)| via the control variable, I(t)

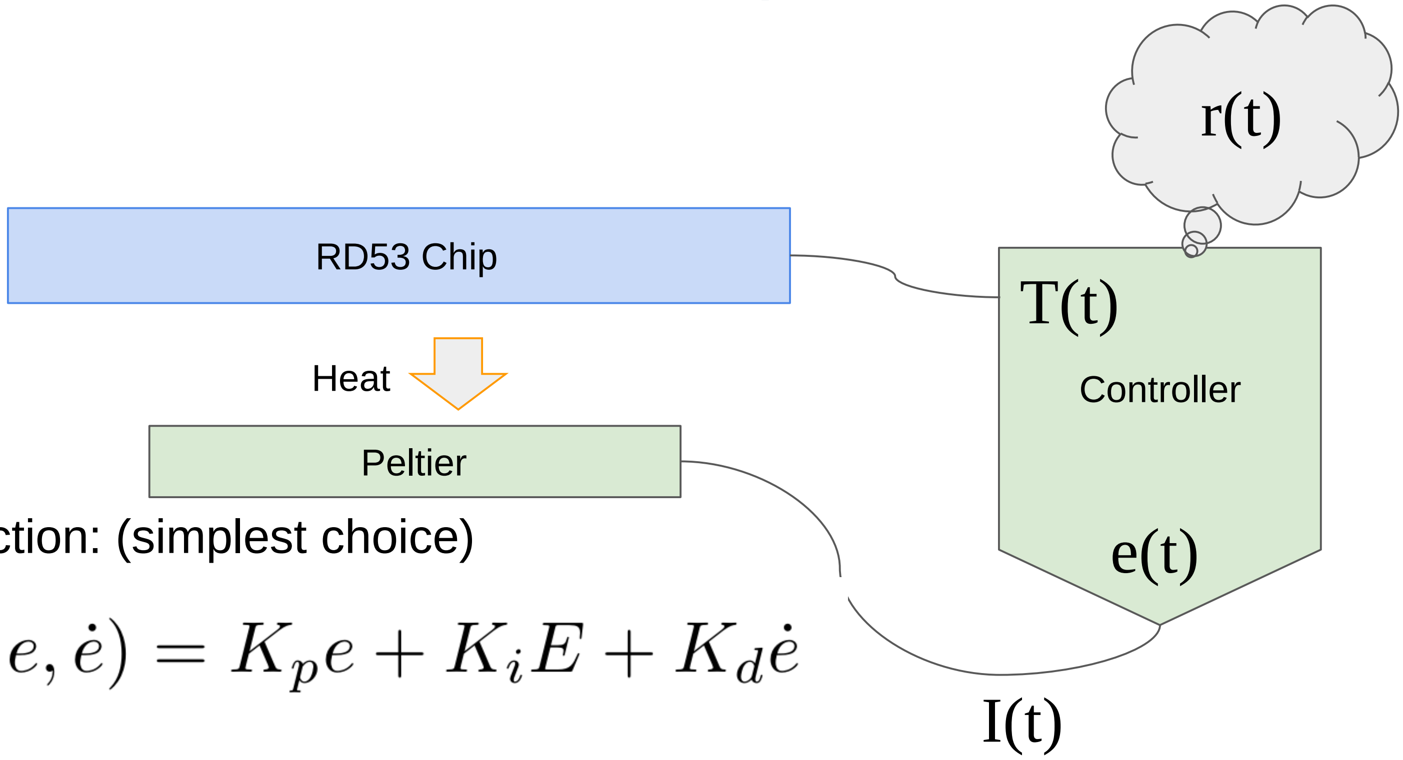
Control Process Principles



- The control variable I(t) is the current supplied to the Peltier
- It is some function of e(t) and its derivatives:

$$I(t) = f(E,e,e')$$

Control Process Principles



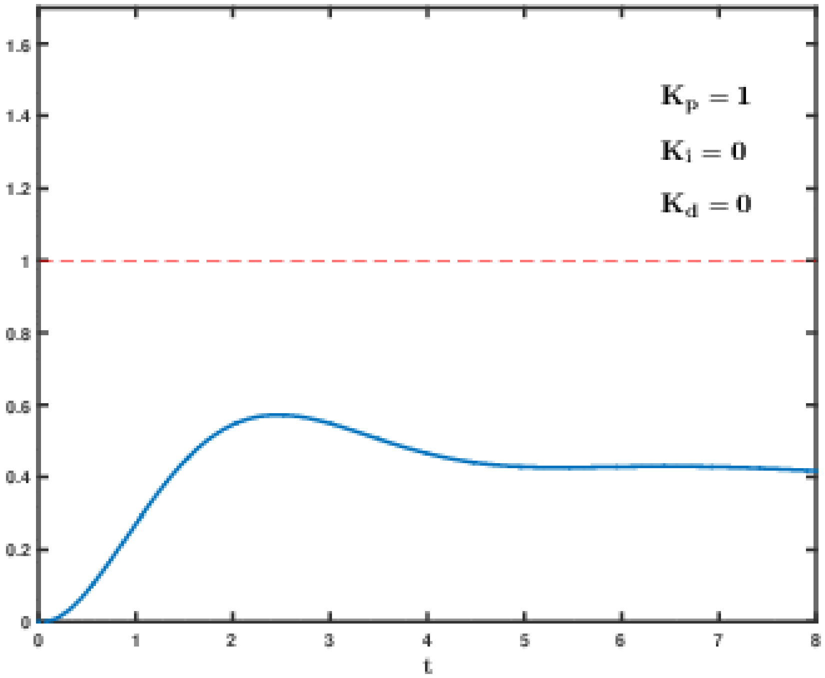
PID Control Function: (simplest choice)

$$I(t) = f(E, e, \dot{e}) = K_p e + K_i E + K_d \dot{e}$$

The constants K_p K_i, and K_d are the *PID coefficients.*

-> Need to be tuned to match the system’s needs.

Control Process Principles



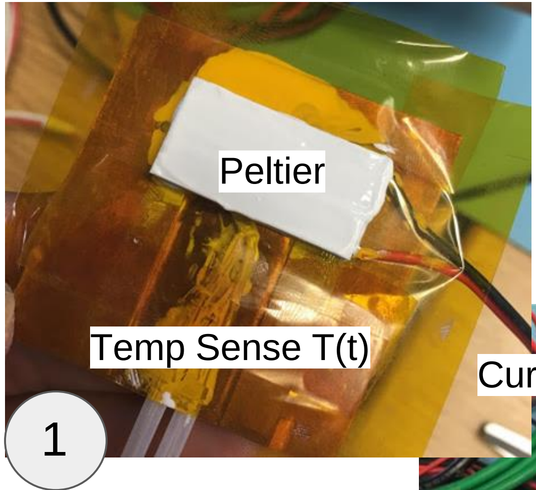
PID Control Function: (simples

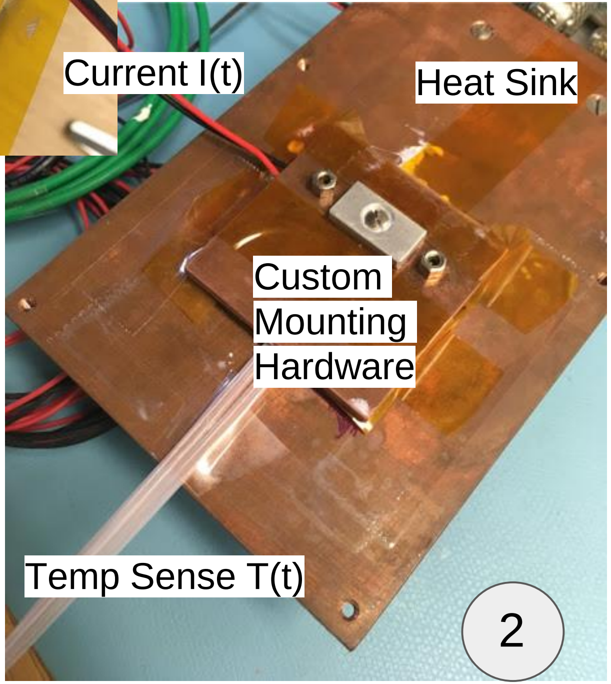
$$I(t) = f(E, e, \dot{e}) = K$$

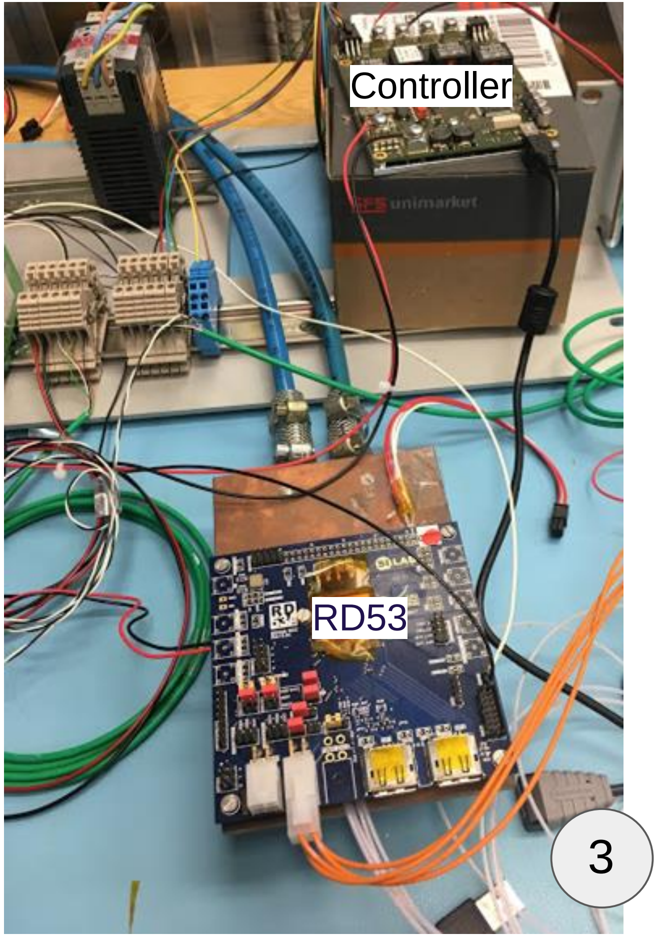
The constants K_p K_i, and K_d are the *PID coefficients.*

-> Need to be tuned to match the system's needs.

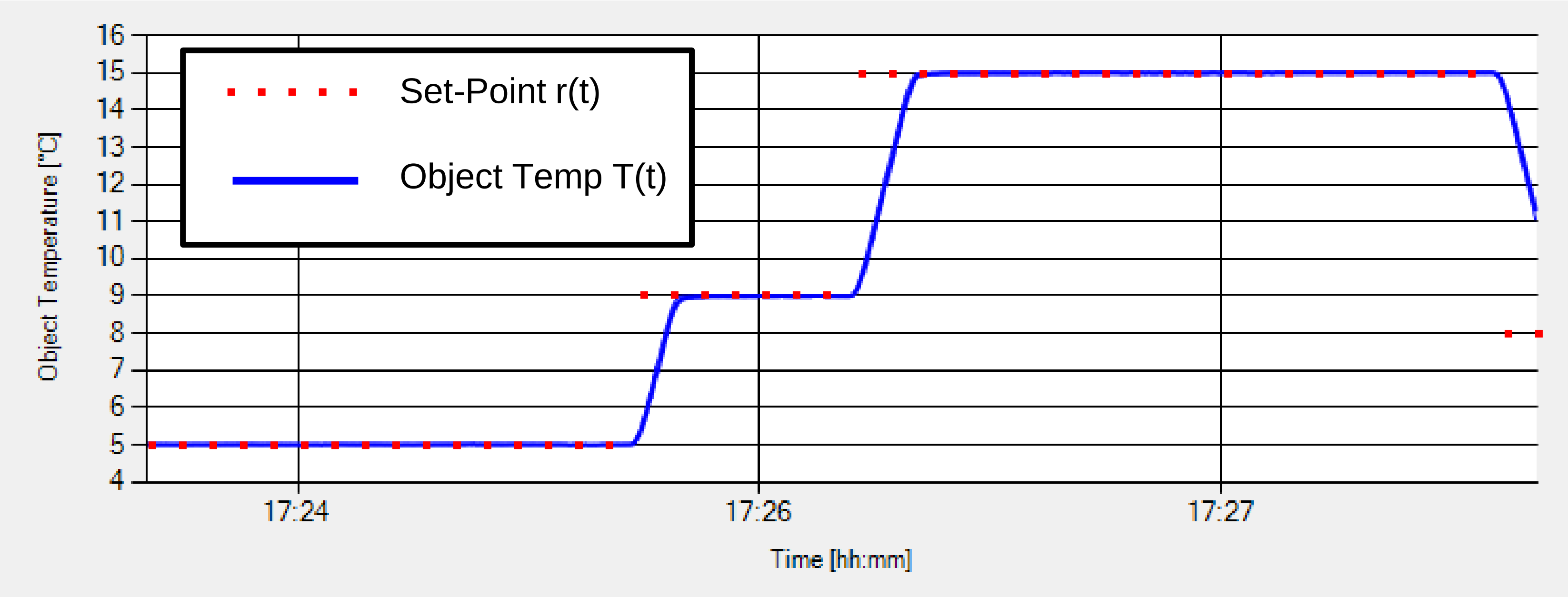
Proof of Concept





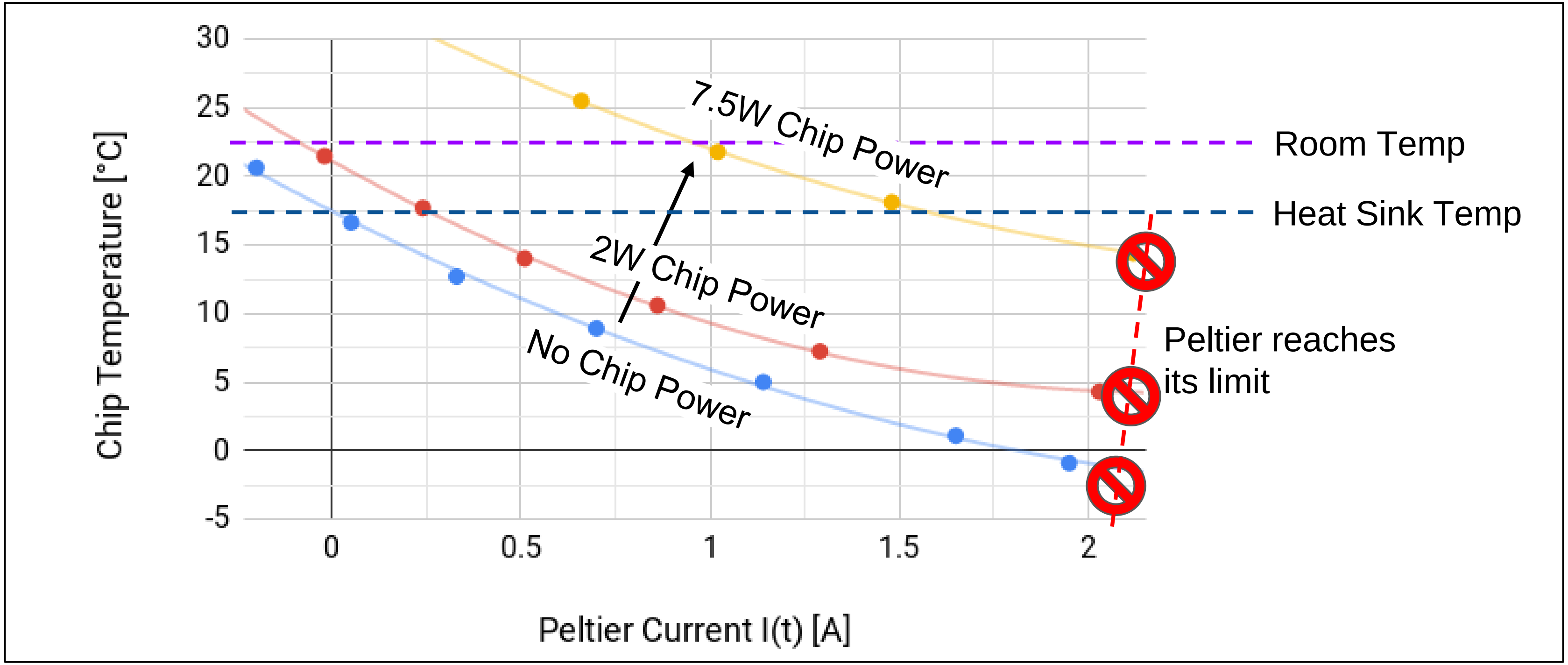


Results: Response



- Control process shows excellent stability
- Reaches equilibrium within 1 minute
- Deviations < 0.01 ^{o}C once stable

Results: Operating Points



- Able to reach -2º C with no load, 4º C with a 2W load, and 14º C with a 7.5W load.
- Could reach lower temperatures with a more powerful Peltier element

Design Goals?

- [x] Remove up to 8W of chip power
- [ ] Operate at chip temperatures at or below room temperature with protection when around dewpoint.
- [x] Most important point - Remain *stable* while within specified operating zones.
- [x] Come to equilibrium quickly (<5 mins)
- [ ] Cool multiple chips (goal: 4)

No dewpoint protection yet

Possible with more hardware

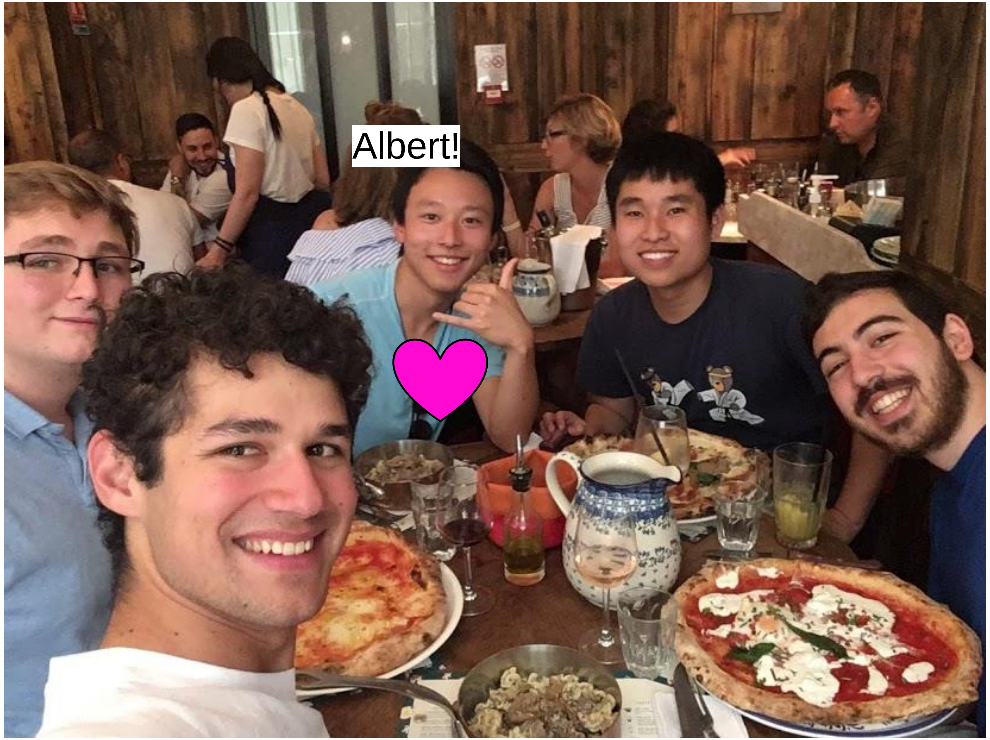
Future Work

Fig: A Happy Grad Student Learns How to Assemble the Temperature Control System

- Order enough hardware for four chips
- Improve temperature sensor accuracy
- Protect against dewpoint (dry box)

University of Michigan

Thanks for Listening!



extra

References

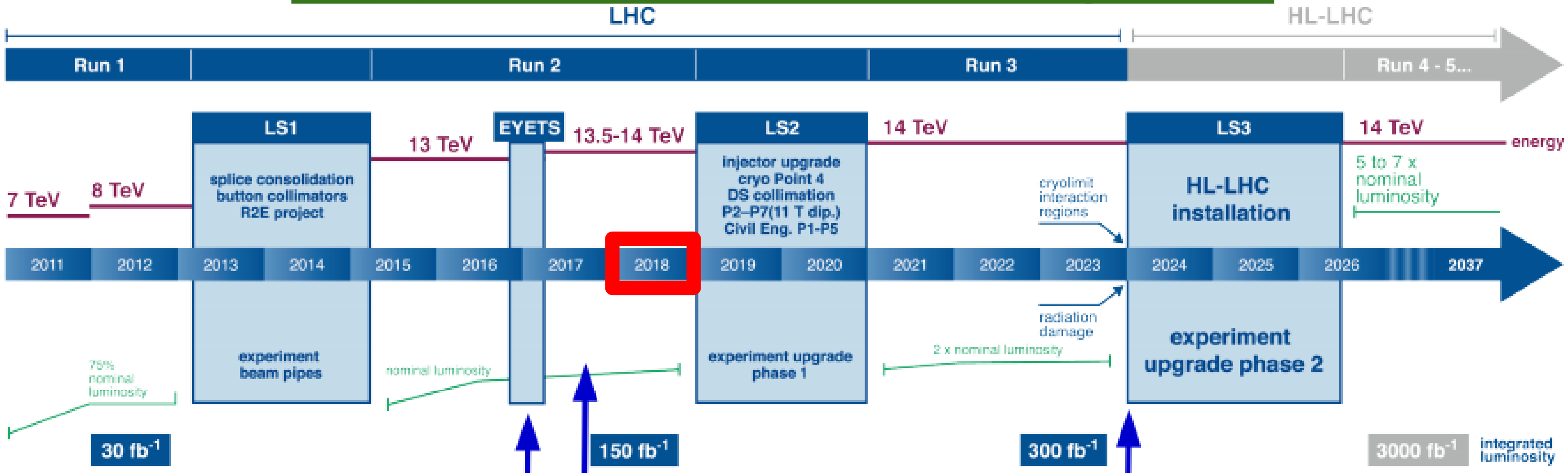
[1] CMS Collaboration. “*Technical Proposal for the Phase-II Upgrade of the CMS Detector”*, CERN-LHCC-2015-010 ; LHCC-P-008 ; CMS-TDR-15-02. CMS Collaboration ; CERN. Geneva. The LHC experiments Committee ; LHCC. 2015.

[2] CMS Collaboration, “*Precise determination of the mass of the Higgs boson and studies of the compatibility of its couplings with the standard model”*, Technical Report CMS-PAS-HIG-14-009, CERN, Geneva, 2014.

[3] CMS Collaboration, “*Projected Performance of an Upgraded CMS Detector at the LHC and HL-LHC: Contribution to the Snowmass Process*”, arXiv:1307.7135.

[4] "File:PID Compensation Animated.gif." *Wikimedia Commons, the free media repository*. 27 Nov 2016, 00:50 UTC. 16 Aug 2018, 10:11 <https://commons.wikimedia.org/w/index.php?title=File:PID_Compensation_Animated.gif&oldid=220826476>.

Approved LHC Program



Nominal luminosity
$= 1\text{x}10^{34}\ \text{cm}^{-2}\text{s}^{-1}$

CMS Phase II
Tracker TDR

CERN-LHCC-2017-009

Start of the CMS
Phase II upgrade

Installation of Phase I
pixel detector