ASICs for the BLM system upgrade

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Project contribution

The BLM ASIC project is carried out as a collaboration between the Micro Electronics (EP-ESE-ME) and the Beam Loss (BE-BI-BL) sections with the support of R2E.

EP-ESE-ME:

- Luca Giangrande
- Jan Kaplon
- Pedro Leitao

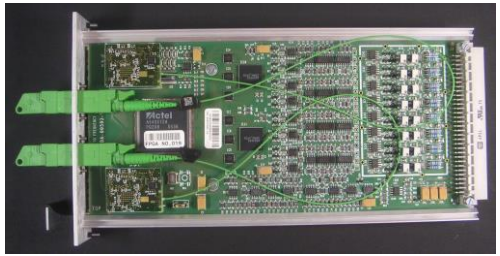
BE-BI-BL:

- Ewald Effinger
- Francesco Martina
- Christos Zamantzas

Beam Loss Monitoring system overview

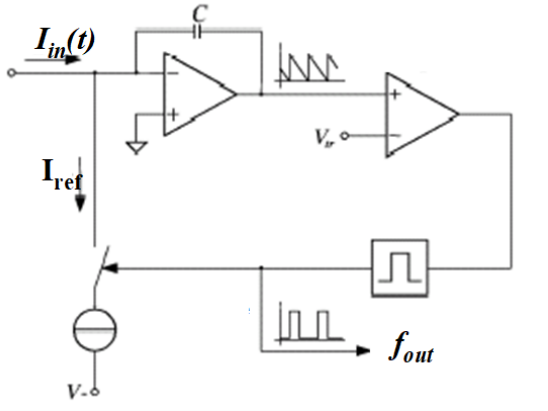
The system measures the radiation levels along the accelerator in order to protect its components and avoid magnets quenching.

- Approximately 4000 gas filled ionization chambers installed throughout the LHC
- Approximately 750 acquisition modules
- Signal cables length up to 800 m



System currently in use

PCB module based on the current to frequency conversion (CFC) principle. Integrator to collect the ionization charge and negative feedback to perform the charge balancing.



Implemented features:

- 8 channels
- Radiation hardness up to 50 kRad (500 Gy)
- Resistance to 100 µs electrical overstress : 10 A or 1.5 kV
- Measurement range: 1 mA ~ 2.5 pA
- No measurement dead time
- Integration time window: 40 µs
- Redundant data transfer

$<I_{in}(t)>$	1 mA	1 µA	1 nA	1 pA
f_{out}	5 MHz	5 kHz	5 Hz	5 mHz

E. Effinger ,“BLM tunnel installation and data acquisition card (BLECF)” ,
http://indico.cern.ch/event/111862/contributions/52722/attachments/37631/54325/AUDIT_E_Effinger-2010.pptx

Requirements for the upgrade

In order to improve the BLM system and to ensure its compatibility with the higher radiation levels expected from the HL-LHC upgrade the following requirements have been defined:

- Measurement range: 1 mA ~ 1 pA (i.e. 9 decades or 180 dB)
- **Integration time window: 10 µs**
- **Radiation tolerance: > 100 Mrad (i.e. 1 MGy)**
- **Electrical compatibility with LpGBT chip**
- Operational for out-of-range input currents
- Reliability against SEU and EMI
- Compatible with 50m long coaxial cabling (characteristic impedance 50 Ohm, 85 pF/m)

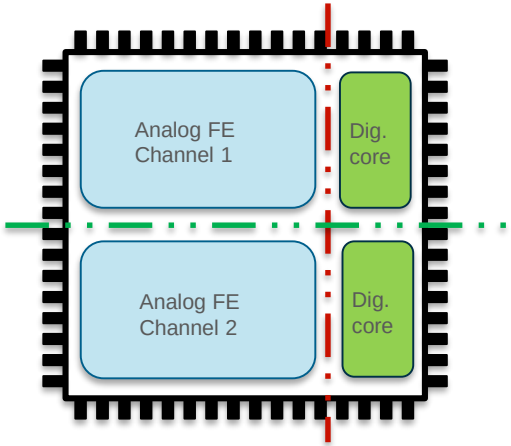
ASICs development

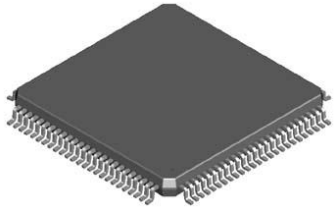
Two fully functional **custom** chips are being developed in order to evaluate the performance of two different architectures within a realistic environment:

- Asynchronous reference-less CFC with auxiliary voltage ADC
- Oversampling Delta-Sigma ADC with dynamic clock rate control

ASICs common features:

- Technology standard CMOS 130 nm qualified at CERN for 200 Mrad
- Supply voltage 1.2 V (possibly higher for analog)
- Two analog readout channels per chip
- Triplicated digital circuitry with majority voting
- Directly compatible with LpGBT (e-Link)
- Double communication channels for redundancy
- Chip dimensions 4x4 mm
- To be housed in a standard 64 pin Quad Flat Package (10x10 mm)

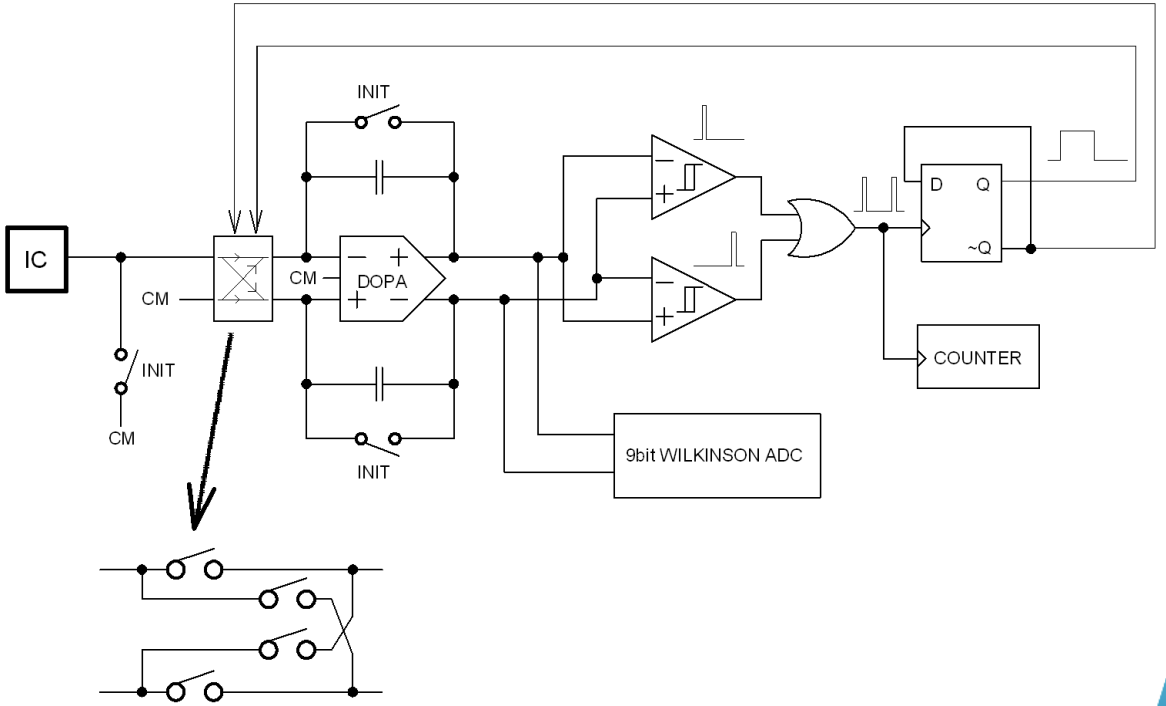




CFC ASIC Architecture

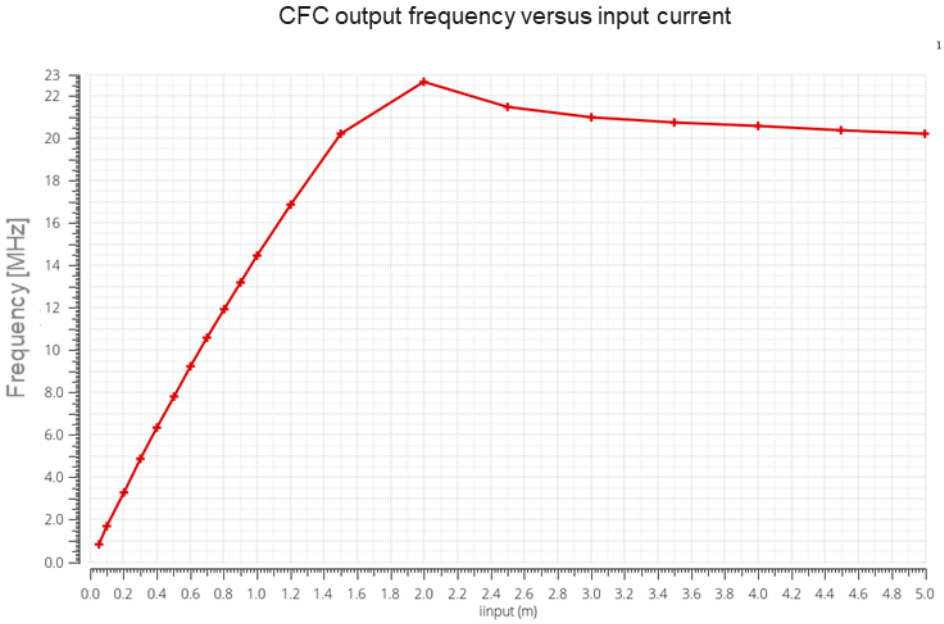
Fully differential asynchronous current to frequency converter with alternating input switches.

9 bit voltage ADC (Wilkinson) for faster response at low input currents (sampling rate 10 µs, LSB 12.5nA).



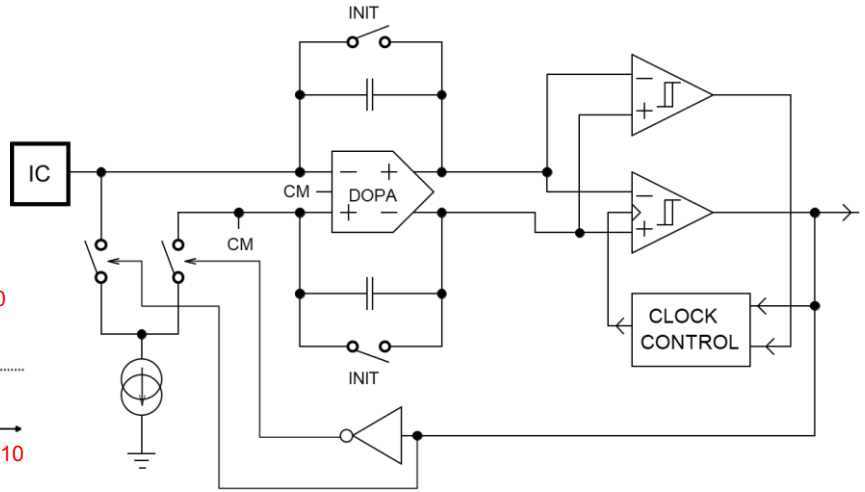
CFC ASIC simulated performance

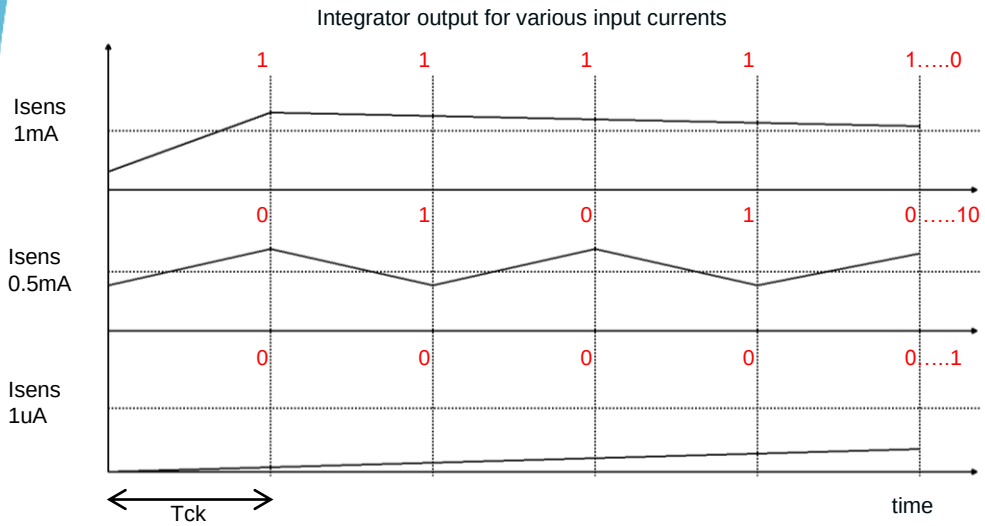
- Current consumption (per analog channel): 15 mA
- Monotonic characteristic up to 1.5 mA
- INL before calibration in the higher range (1 mA ~ 1 pA): 15 %
- INL before calibration in the lower range (10 µA ~ 1 pA) : 0.5 %
- RMS noise in the 10 µs integration time (voltage ADC): < 2 nA
- CFC conversion factor: 17 GHz/A



ΔΣ ASIC architecture

Multi-range 10 bit ADC based on fully differential first-order single-bit synchronous modulator with dynamic clock rate control.

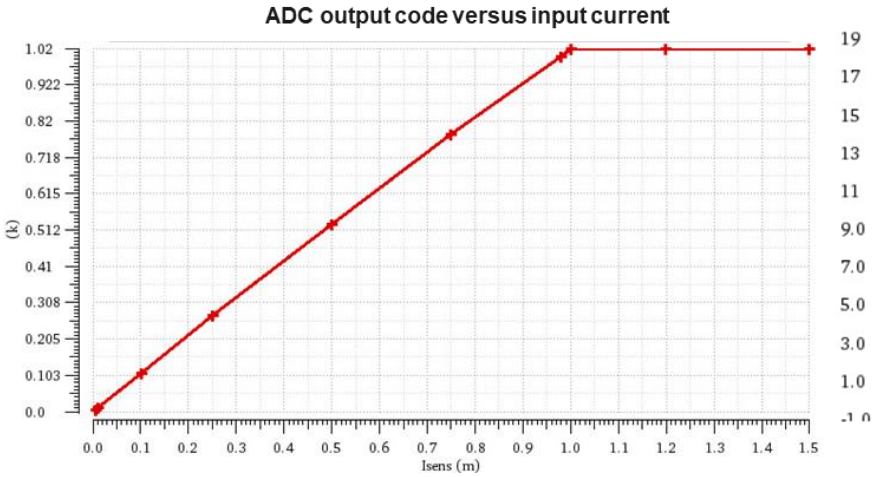


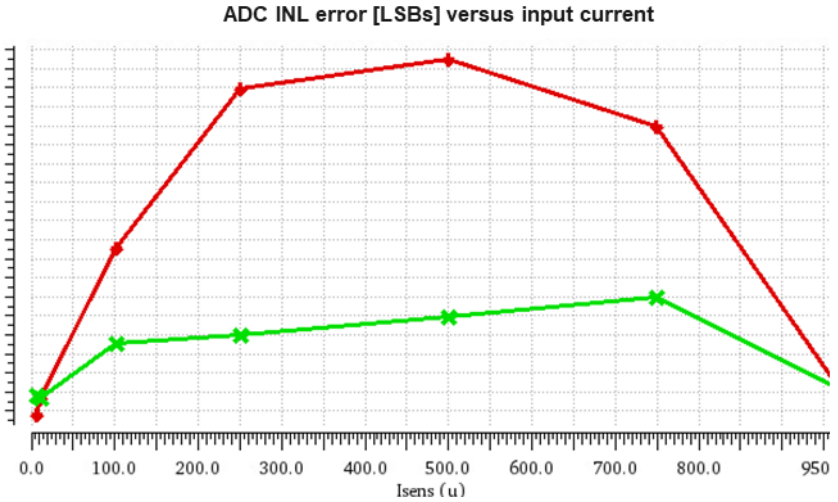


Fck	Imax	Imin
20 MHz	1 mA	0.97 µA
2.5 MHz	125 µA	122 nA
312 kHz	15 µA	15 nA
19.5 kHz	970 nA	954 pA
38 Hz	1.9 nA	1.8 pA

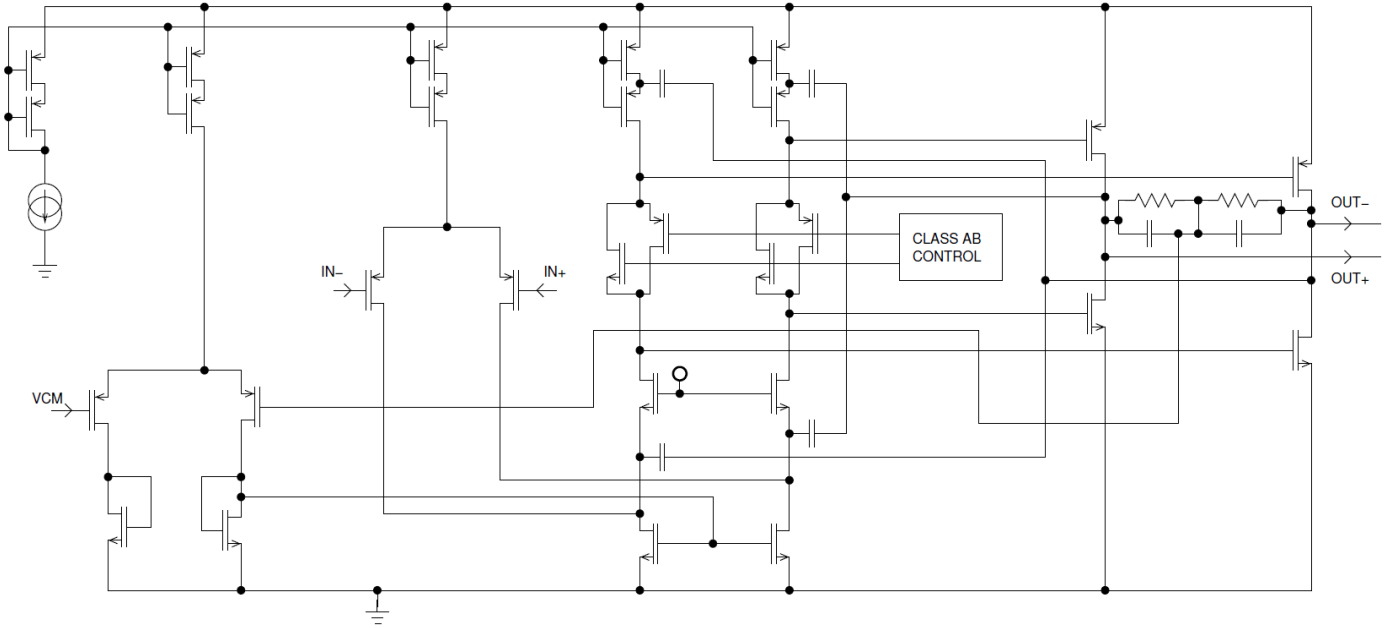
ΔΣ ASIC simulated performance

- Current consumption (per analog channel): 4 mA to 8 mA (signal dependent)
- Monotonic characteristic up to 1 mA input current
- INL (before calibration) in the range 1 mA ~ 1 µA : < 2 %
- RMS noise in the high current range (before filtering): 250 nA





Front end amplifier



Fully-differential two-stages amplifier with cascode Miller compensation and class AB output.

90 dB open loop gain, 200 MHz unity gain frequency.

4 mA static current consumption, 20 pA input leakage, 600 µV RMS output noise in the band 1Hz ~ 1GHz*).

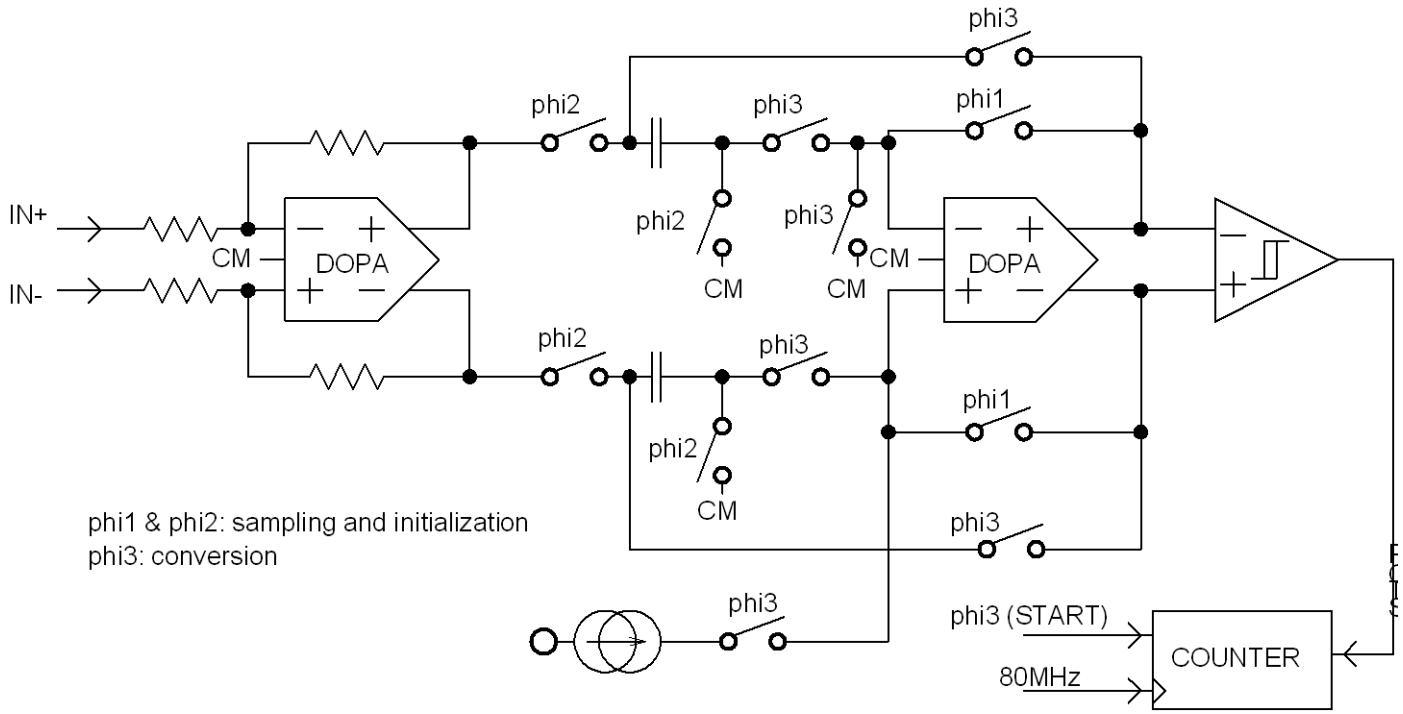
*) For the amplifier in the integrator configuration with 50pF integrating capacitance and 5nF input capacitance.

ASICs development schedule

- Q1 2018: Technology selection and feasibility
- Q2 – Q3 2018: Transistor level design and simulation
- Q4 2018 – Q1 2019: Layout design and simulation
- Q2 2019: Submission of two, full size prototypes
- Q3 – Q4 2019: Testing (evaluation of functionality and radiation tests)
- Q1 2020: Final prototype architecture selection

Thank you

Wilkinson ADC



Wilkinson ADC: differential amplifier and comparator
Amplifier topology the same as for integrator (open loop gain 90dB) but bandwidth limited to 60MHz.