Tracking performance with the HL-LHC ATLAS detector

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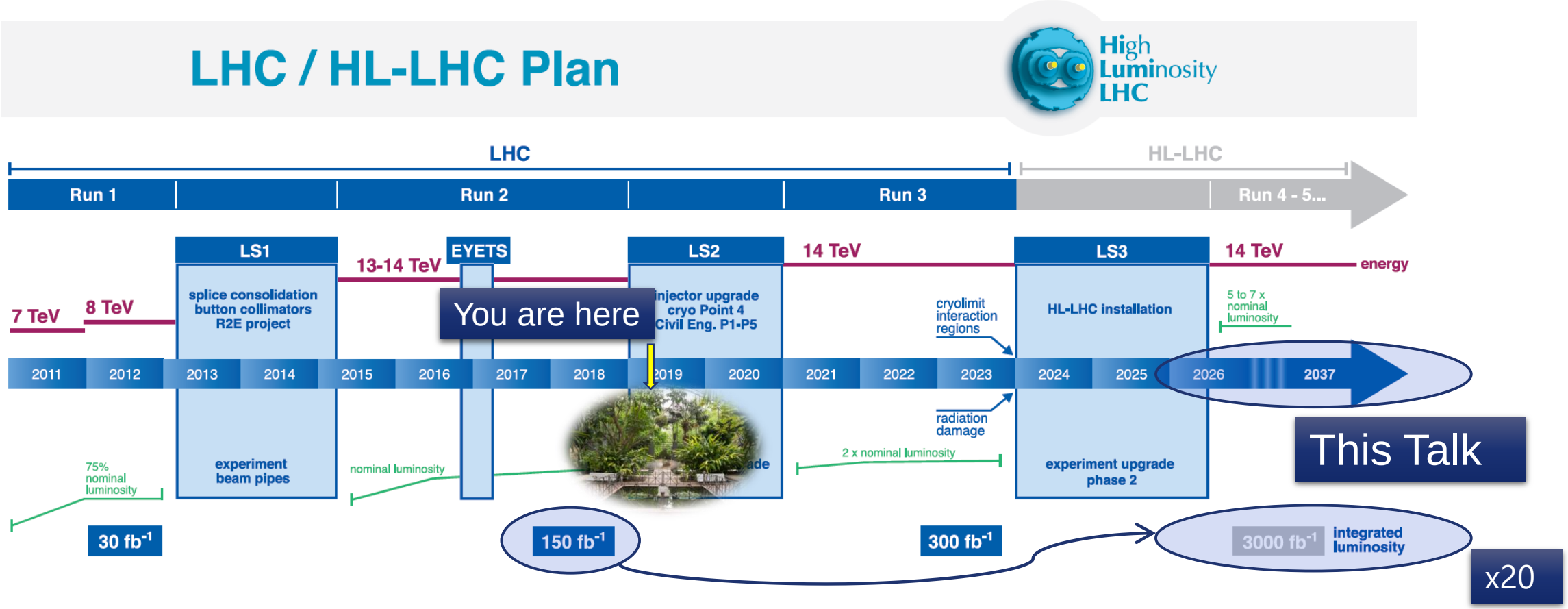
ATLAS EXPERIMENT

Brandeis University

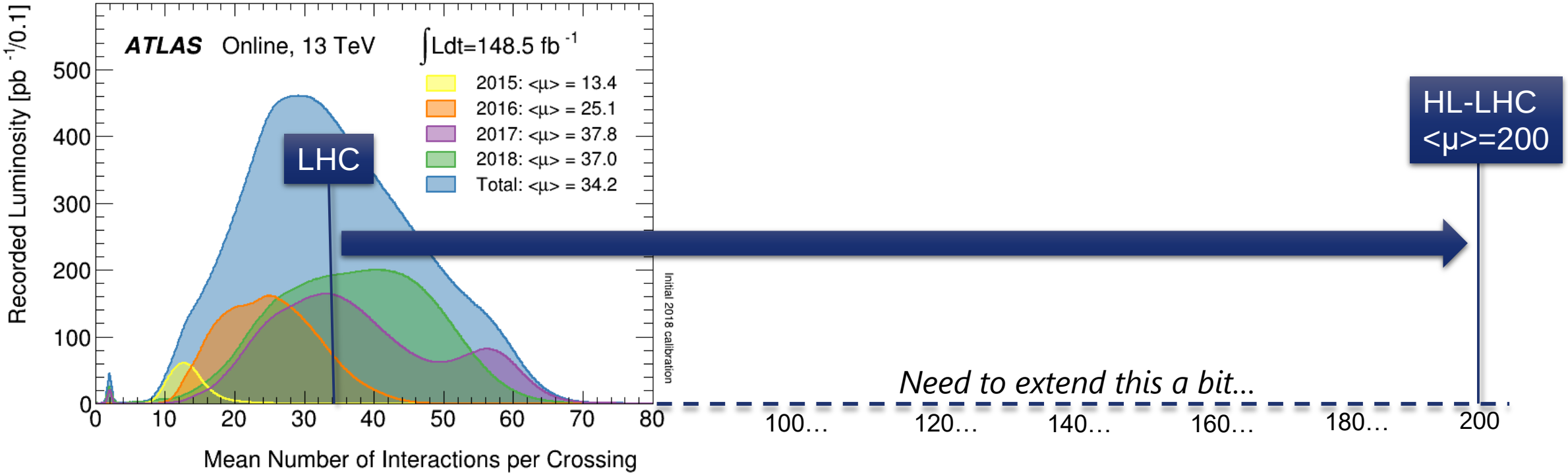
The High-Luminosity LHC Upgrade



- The **High-Luminosity LHC (HL-LHC)** represents a dramatic step in LHC machine performance
- Operation at **up to L=7.5·10^{34} Hz/cm^{2}** (LHC run-2: 2·10^{34}) to collect up to **3000fb^{-1}** of int. luminosity
- Promise vast increase of experimental reach

The High-Luminosity LHC Upgrade

- But the high luminosity also represents a dramatic step in **experimental conditions**
  - Up to **200** p-p collisions per bunch crossing
- Extensive **detector upgrades** enable experiments to operate at HL-LHC
  - Among others: All-new **tracking detectors** for ATLAS and CMS



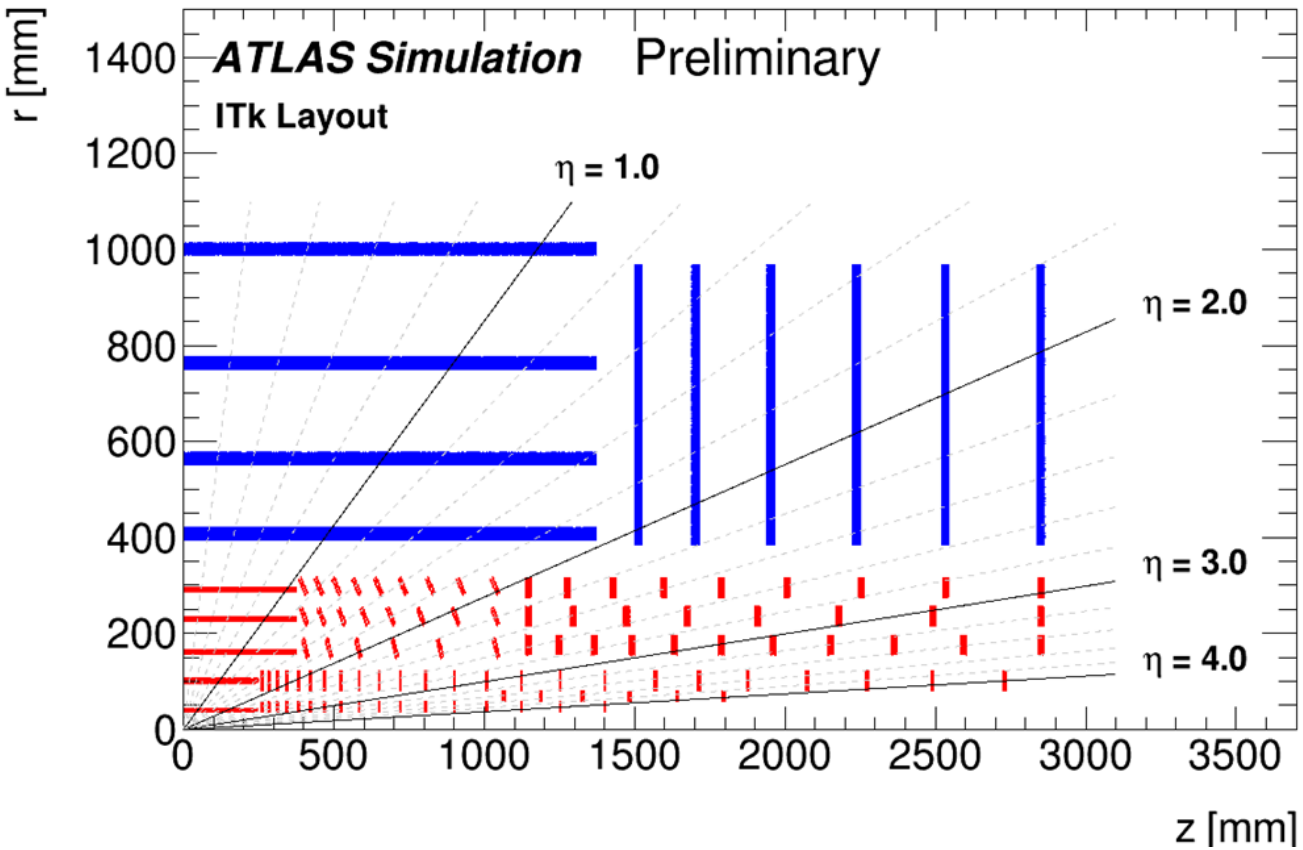
The ATLAS Inner Tracker (ITk)

- **All-silicon** replacement of ATLAS Inner Detector (ID)
- Scheduled for installation during **LS3** (2024-26)

- Designed to **maintain or exceed** current (Run-2) performance at <μ>=200

- Combination of **pixel** and **strip** sensors
  - ➢High number of precision space points for redundancy and suppression of fakes
  - ➢ Innermost two pixel layers designed to be **replacable** during HL-LHC life time

- Increased **acceptance** – |η| < 4
  - Enhance pileup discrimination for forward jets
  - Increase physics acceptance



The ATLAS Inner Tracker (ITk)

Documentation of initial designs in **Technical design reports** released during 2017-18

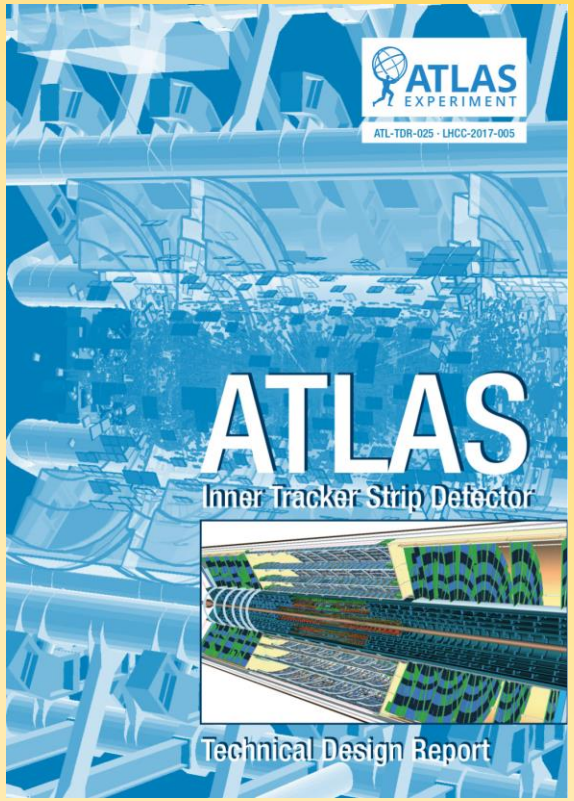
Since then: **Further iteration** on design

- Respond to engineering requirements
- Finalise open design decisions

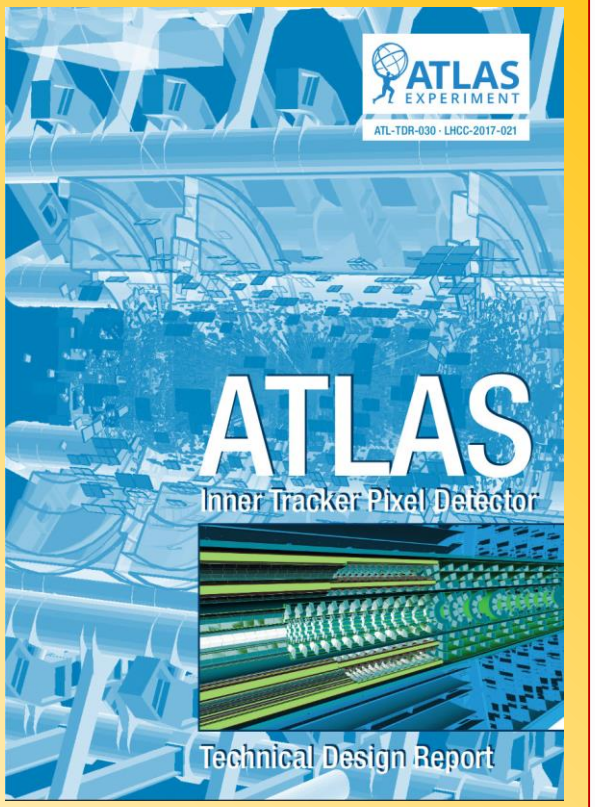
Latest layout (basis of this talk):
ATL-PHYS-PUB-2019-014

Technical Design Reports

Strip subsystem:
CERN-LHCC-2017-005



Pixel subsystem:
CERN-LHCC-2017-021

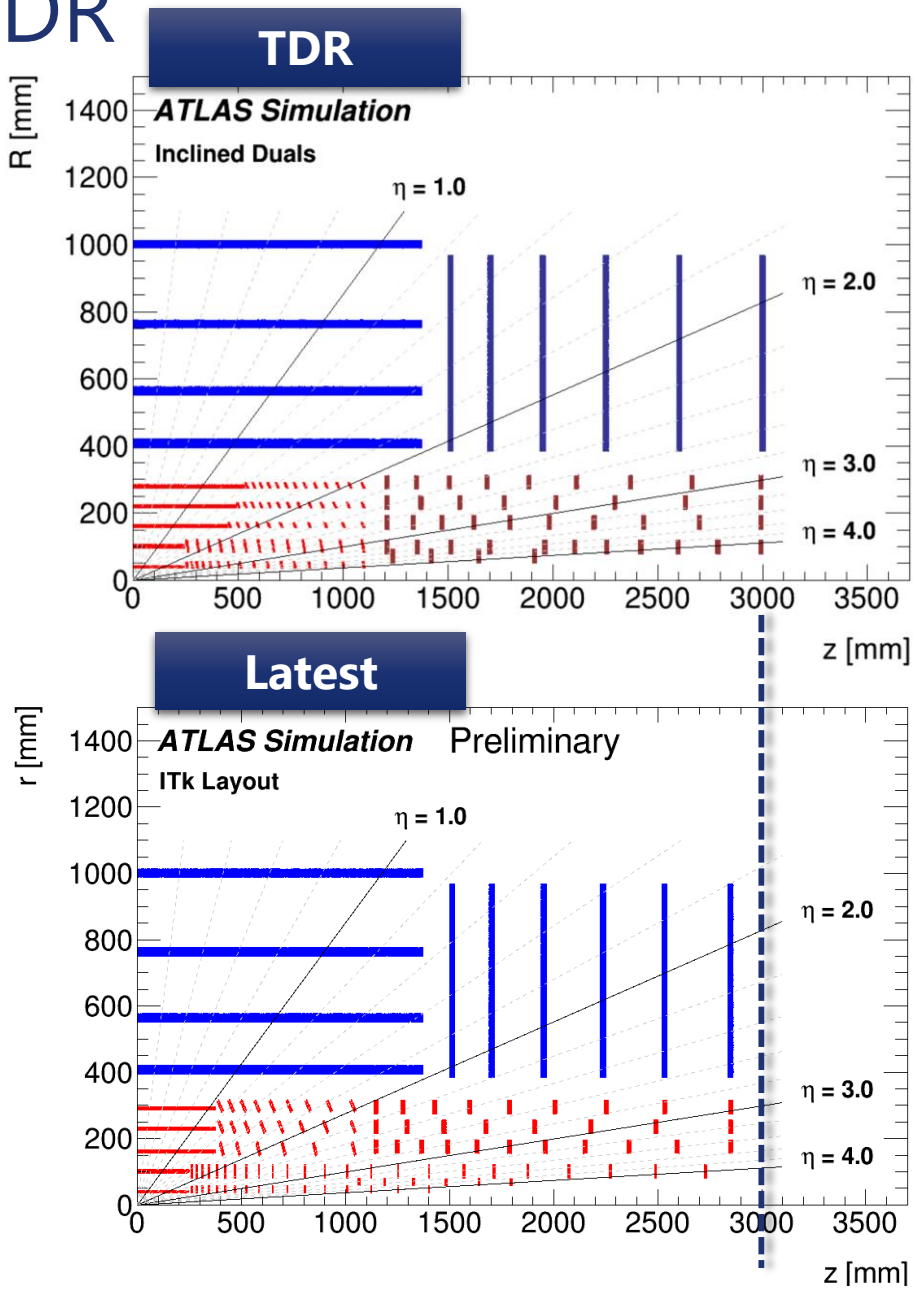


The ITk layout – changes following the TDR

- Reduced length in **z direction** to make space for a **High-granularity timing detector**
  - Enable additional pileup discrimination by adding time information to forward tracks

More on the HGTD:
Technical Proposal & Talk by Lucia – Monday)

➢Saved 15cm in length for both Pixels and Strips
  - Also allows additional space for cabling



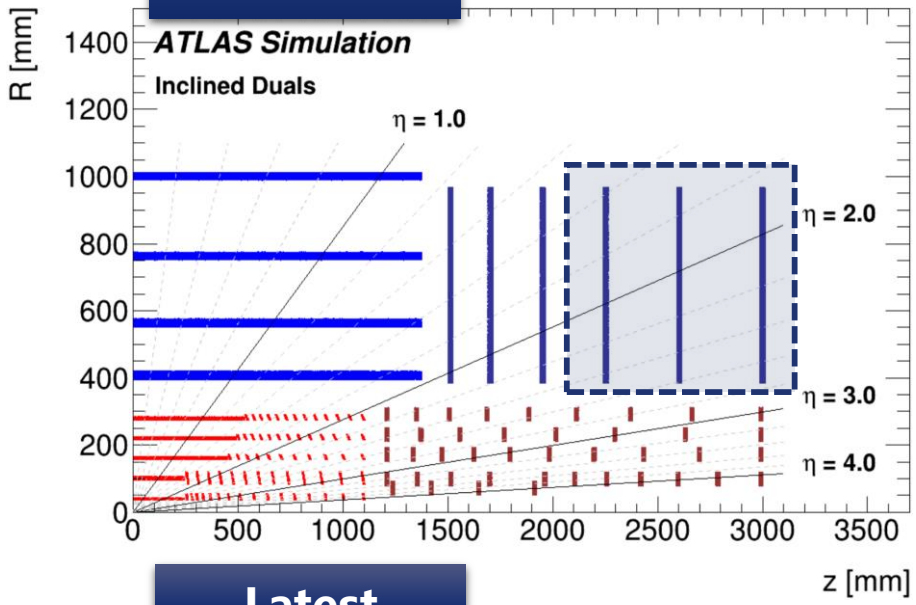
The ITk layout – changes following the TDR

- Saved 15cm in length for both Pixels and Strips
  - Also allows additional space for cabling

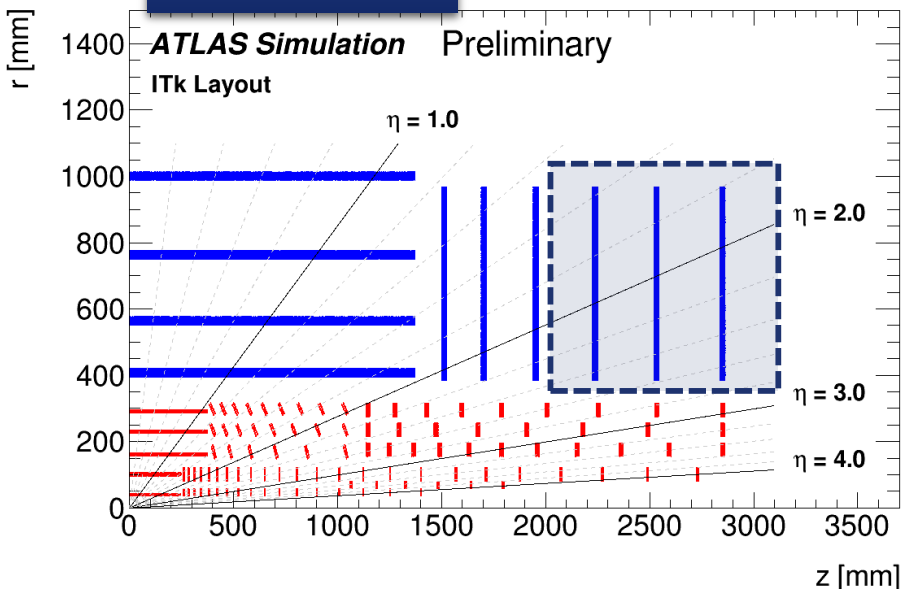
Several **updates to strip subsystem:**

- Reoptimised strip disk locations to new z extent
  - while taking care to ensure sufficient space for installation

TDR



Latest



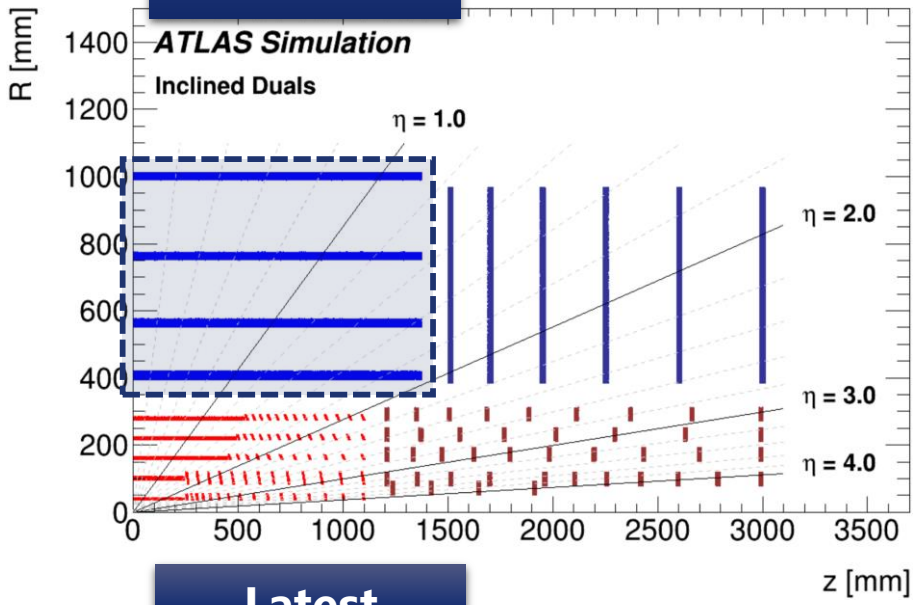
The ITk layout – changes following the TDR

- Saved 15cm in length for both Pixels and Strips
  - Also allows additional space for cabling

Several **updates to strip subsystem:**

- Reoptimised strip disk locations to new z extent
  - while taking care to ensure sufficient space for installation
- Revised tilt angles of barrel strip modules to ensure safe installation

TDR



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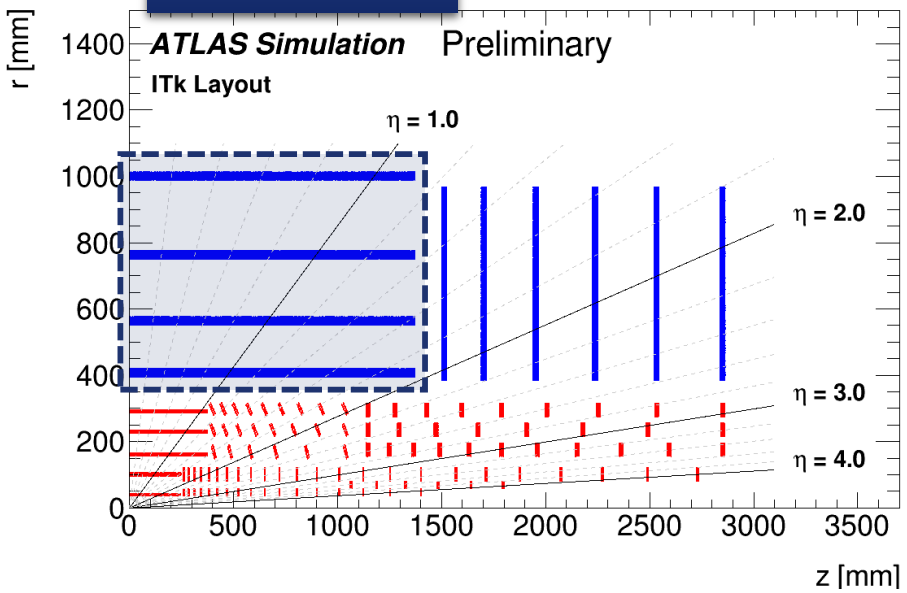
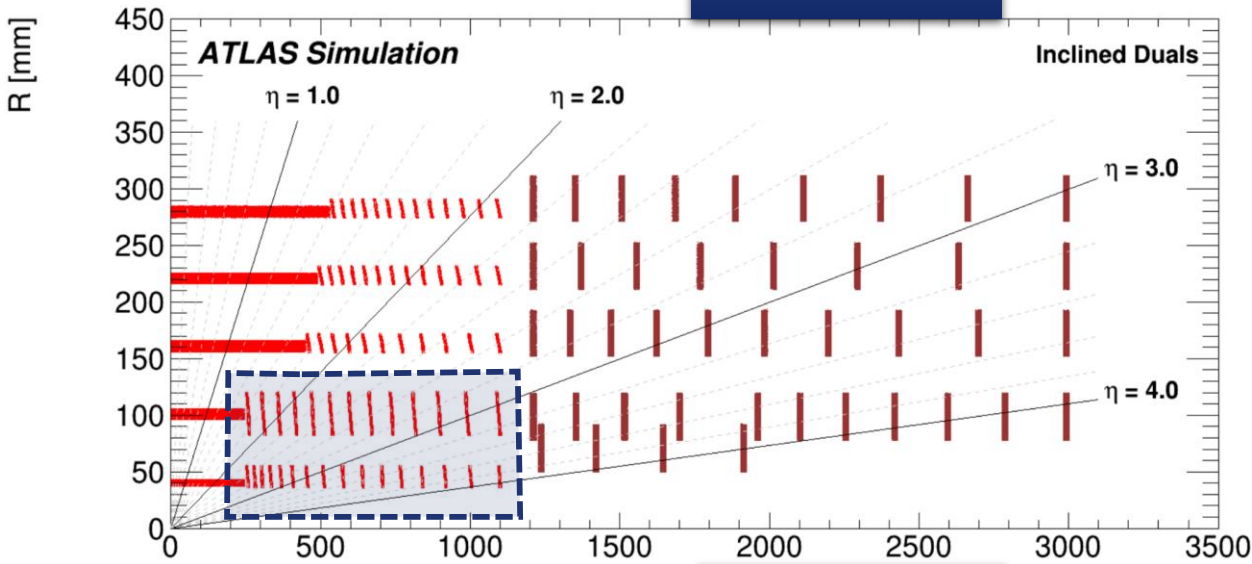


The ITk layout – changes following the TDR

Redesigned **inclined section** of Pixel subsystem:

- First two layers: Move to **coupled rings**

TDR



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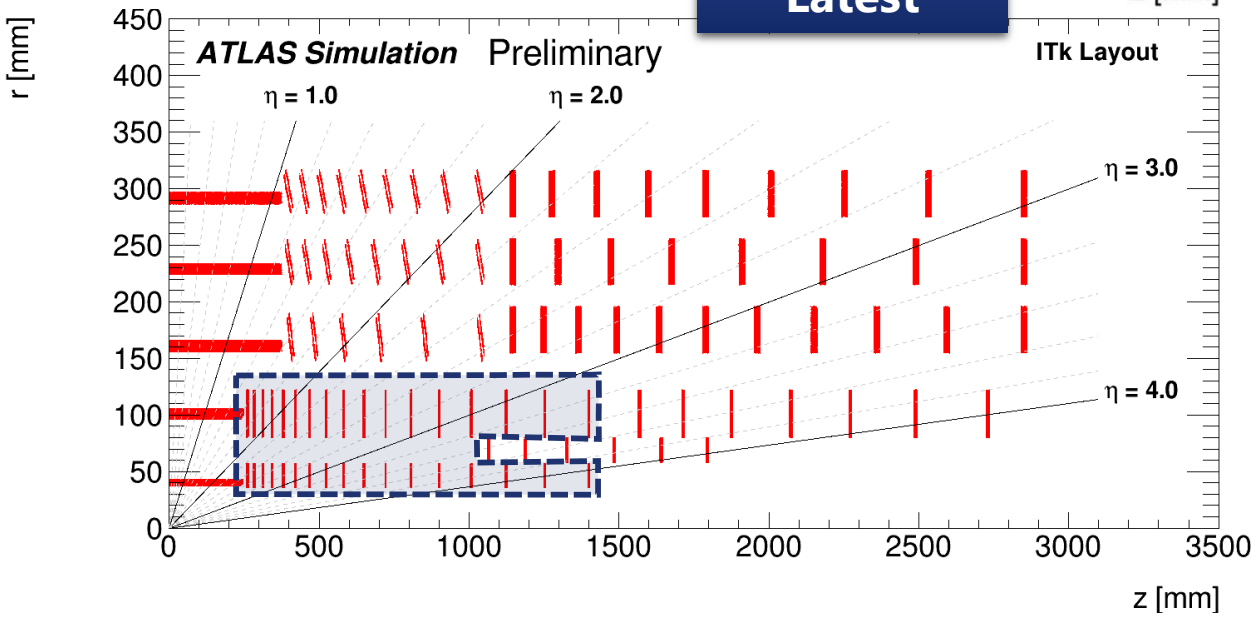
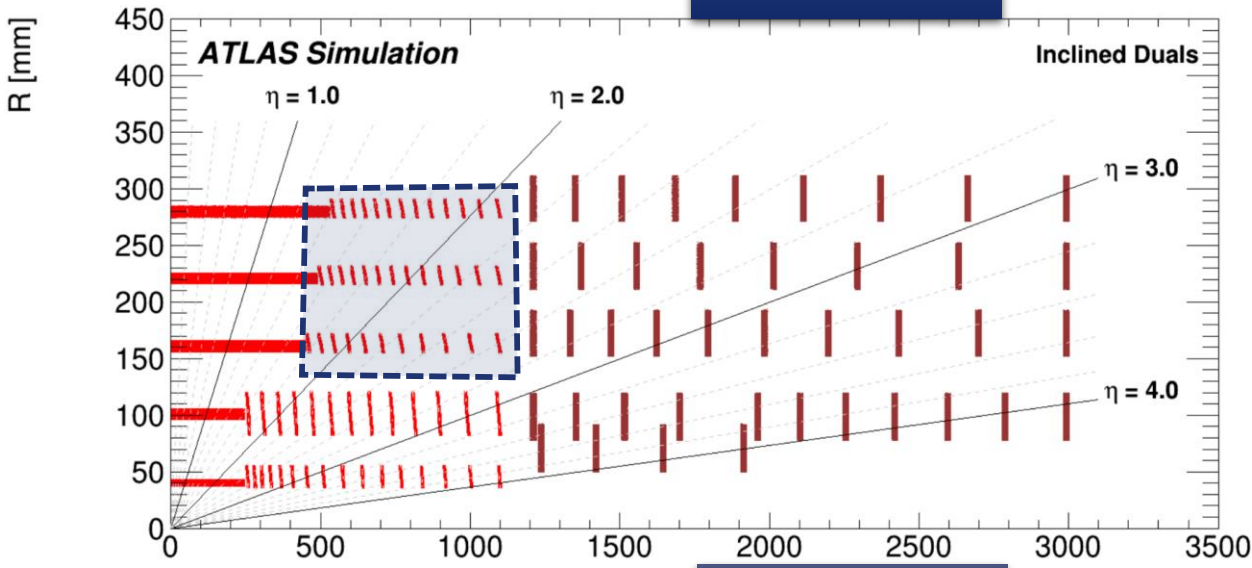


The ITk layout – changes following the TDR

Redesigned **inclined section** of Pixel subsystem:

- First two layers: Move to **coupled rings**
- Outer three layers: move to **quad** modules
  - Includes Shortening of flat barrel

TDR



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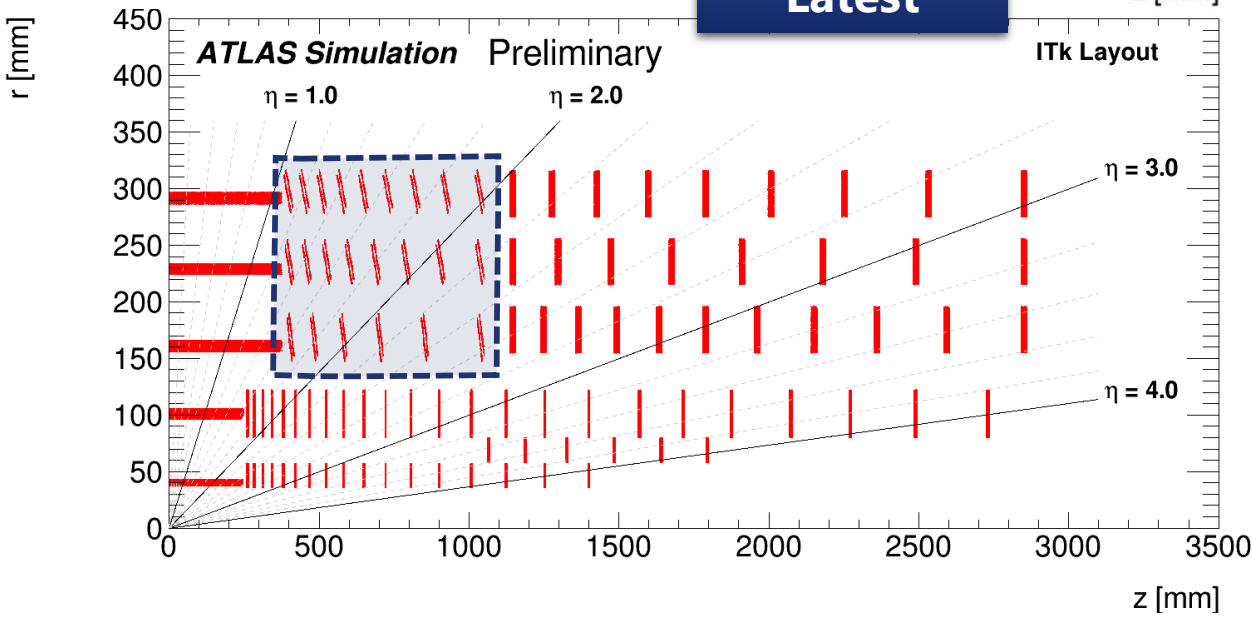
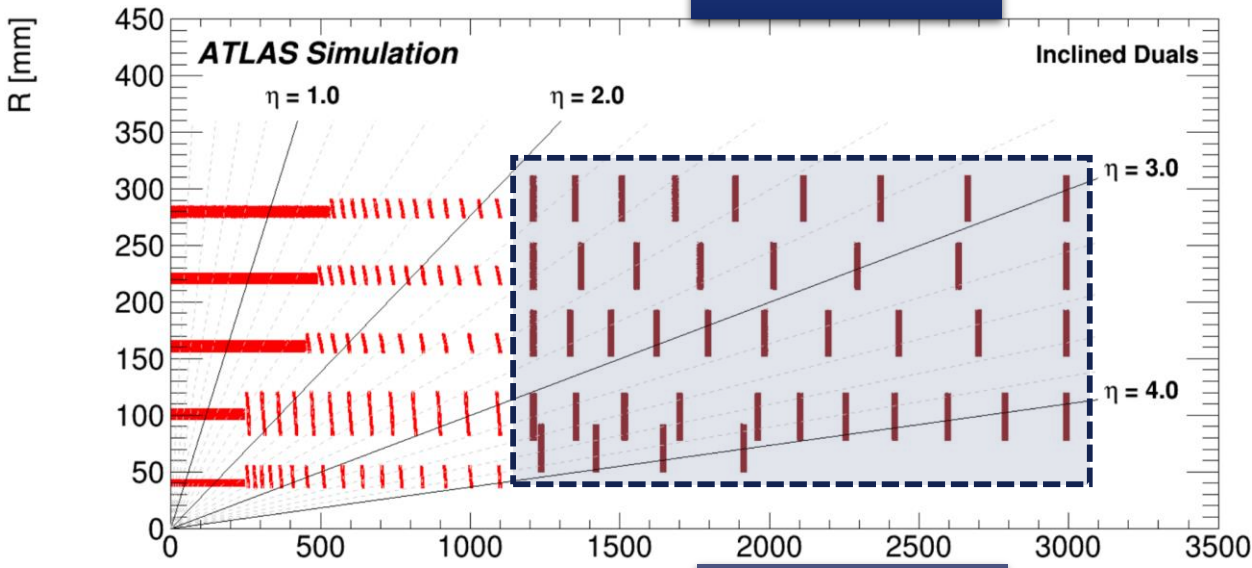


The ITk layout – changes following the TDR

Redesigned **inclined section** of Pixel subsystem:

- First two layers: Move to **coupled rings**
- Outer three layers: move to **quad** modules
  - Includes Shortening of flat barrel
- Update of **Pixel endcaps** to account for reduced z length and modified inclined region

TDR



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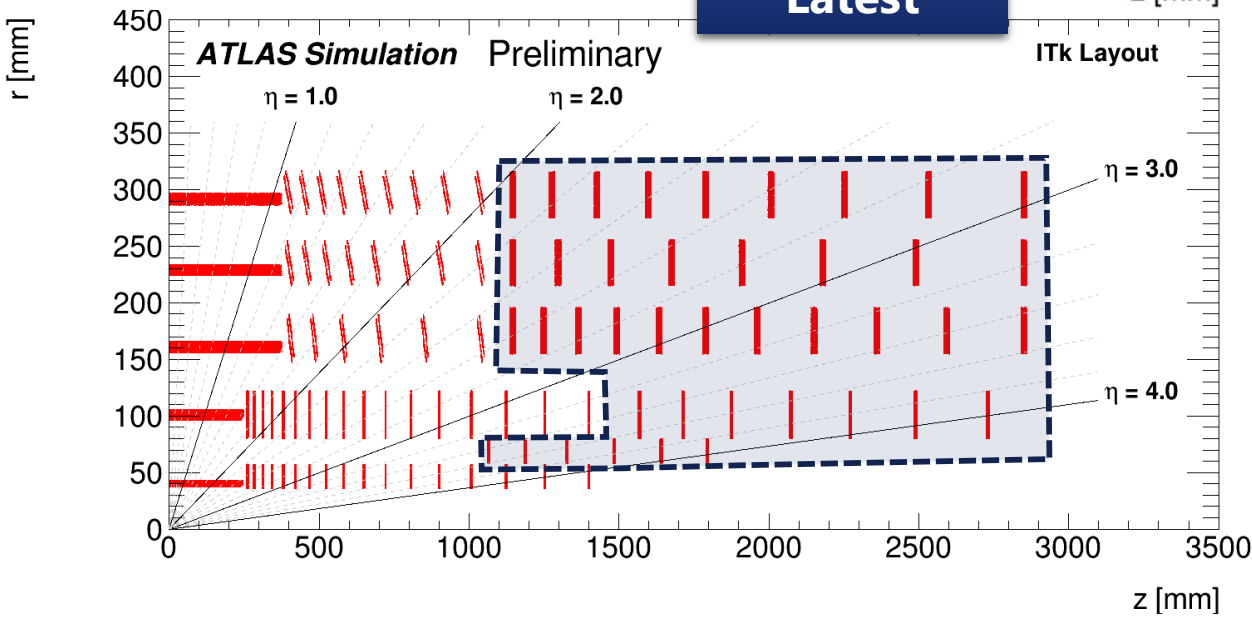


The ITk layout – updated performance estimates

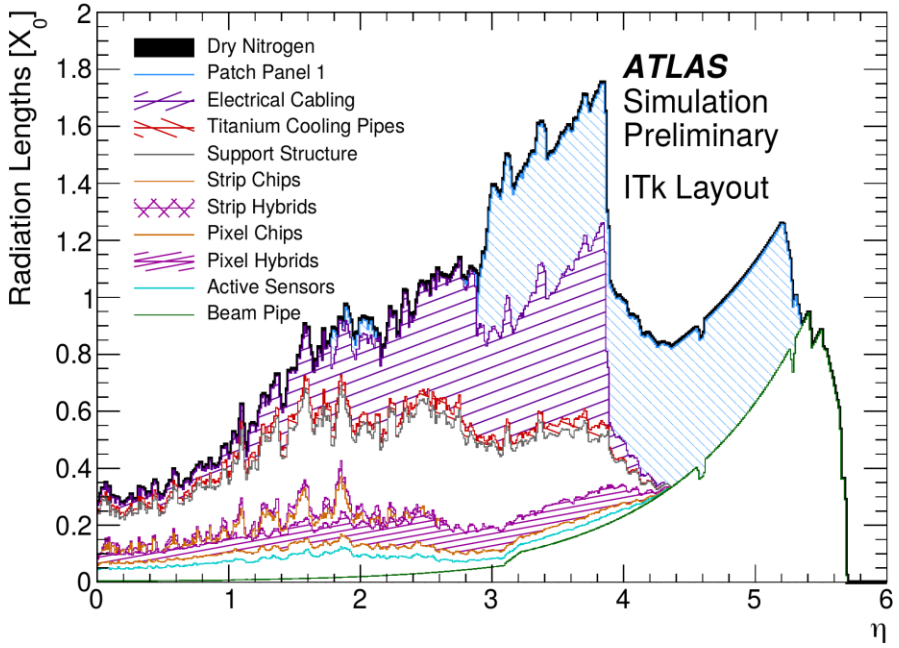
In addition to design changes: Improvements to **simulation model** compared to previous iterations

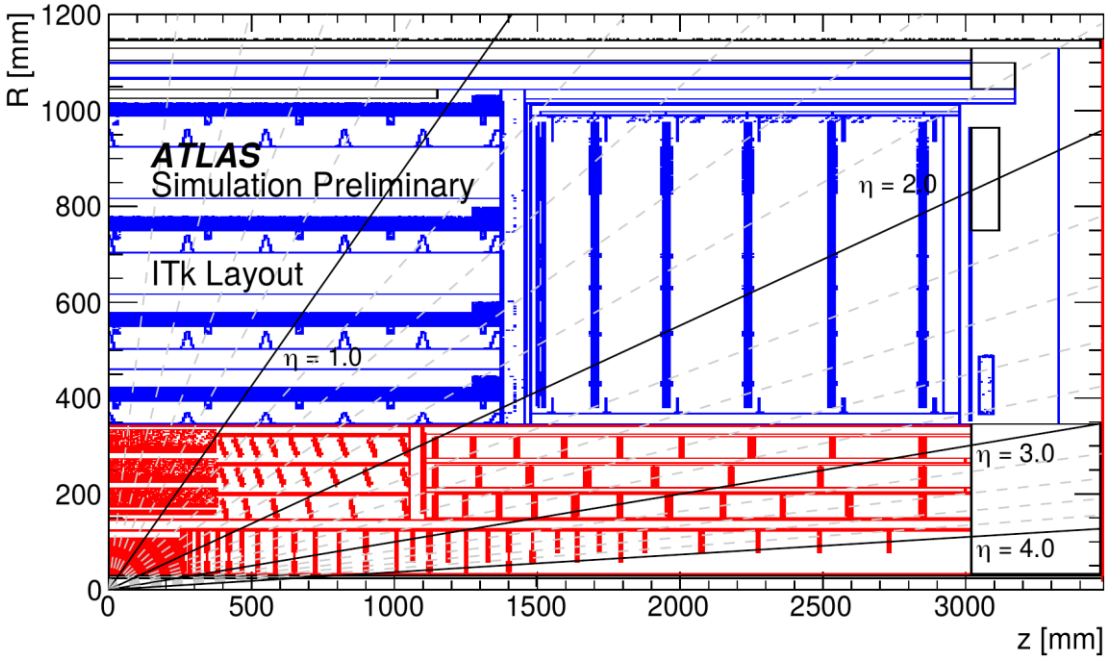
- More detailed geometry description, updated material estimates

➢ Comprehensive set of **performance studies** to evaluate impact of changes to layout and include updates to simulation model

One **open design choice:** Pixel **sensor pitch** – 50x50 μm² or 25x100 μm²

→ Studies compare both where relevant



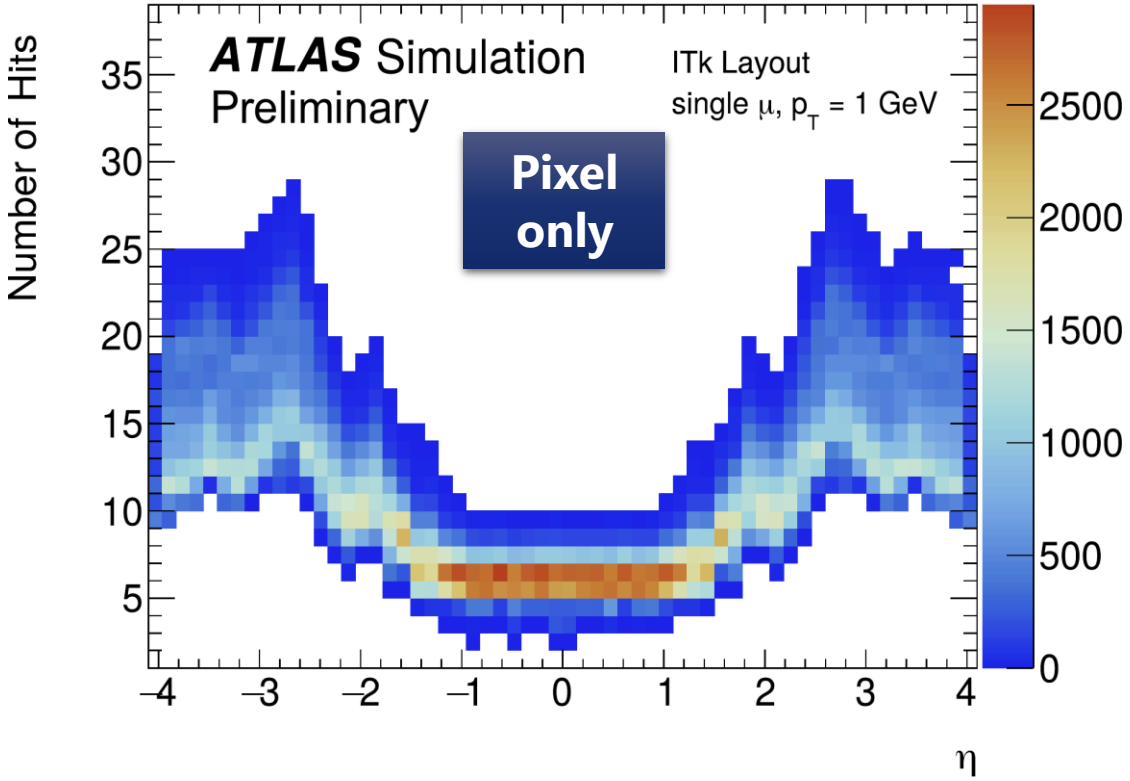


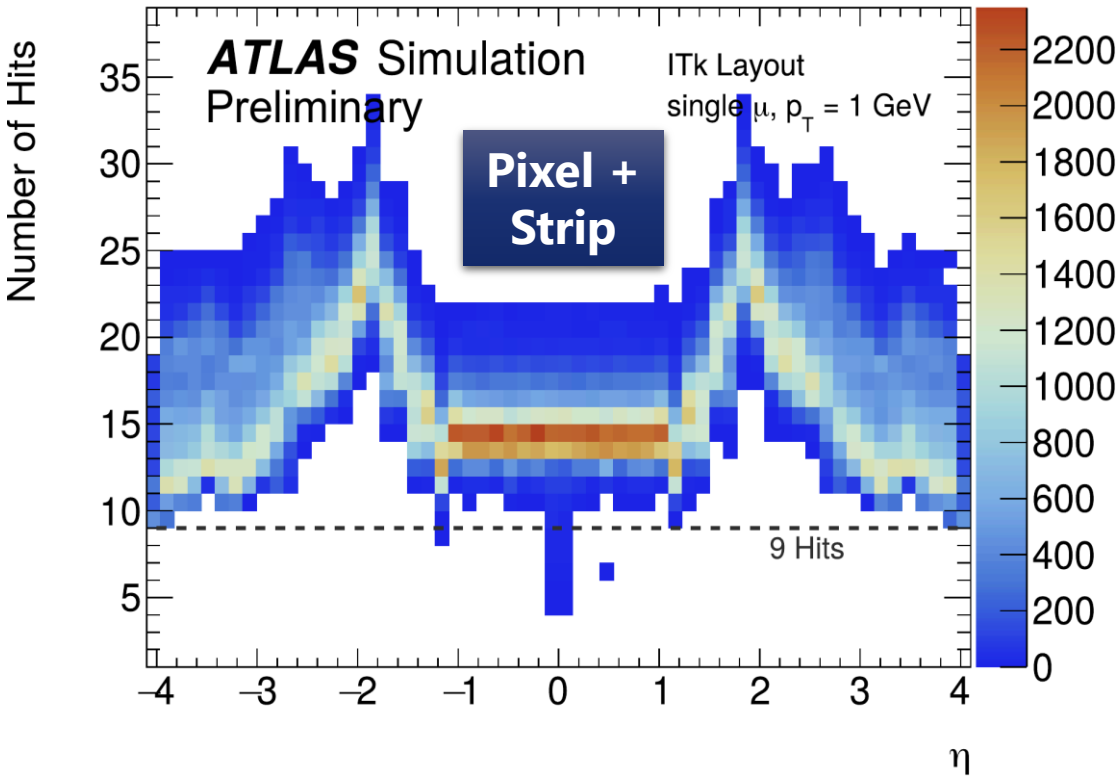
The ITk layout – hermeticity

First observation: Hit hermeticity is preserved

✓ New layout still provides the required **9** space points on track

- for particles in |η| < 4 for |z|<15cm, |r|<2mm
- Rare cases of particles passing through gaps between modules



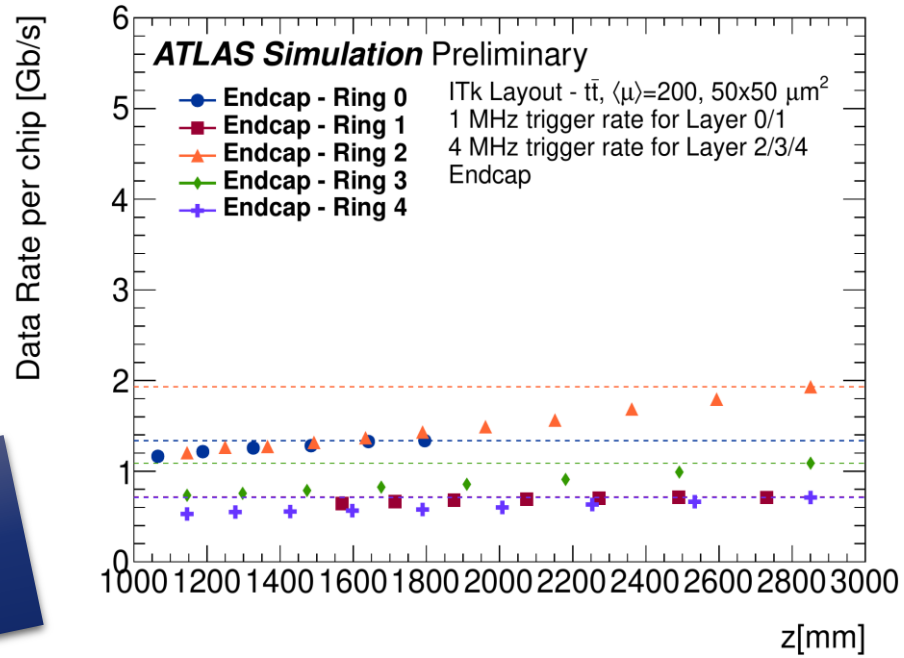


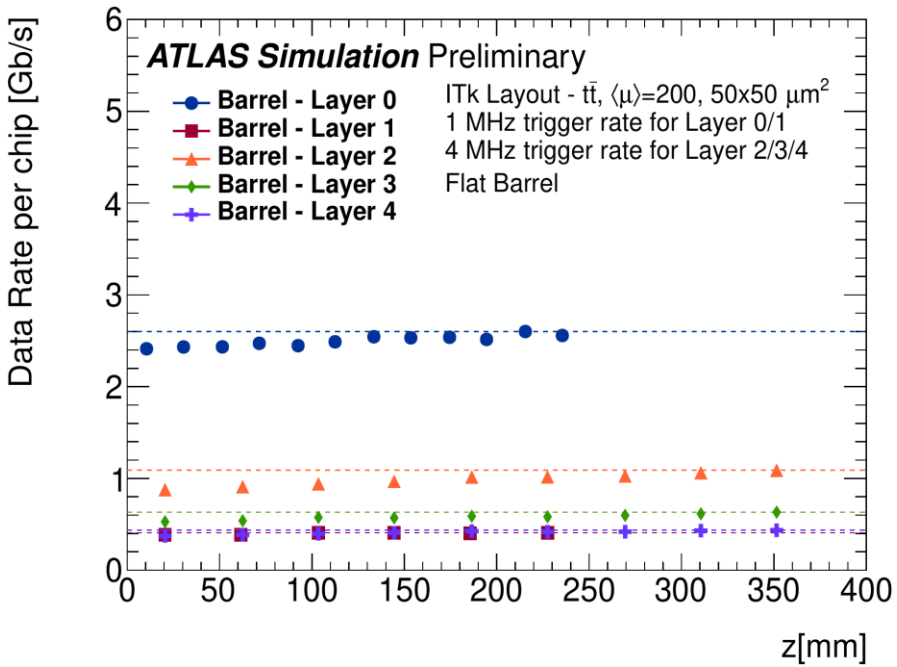
The ITk layout – data rates

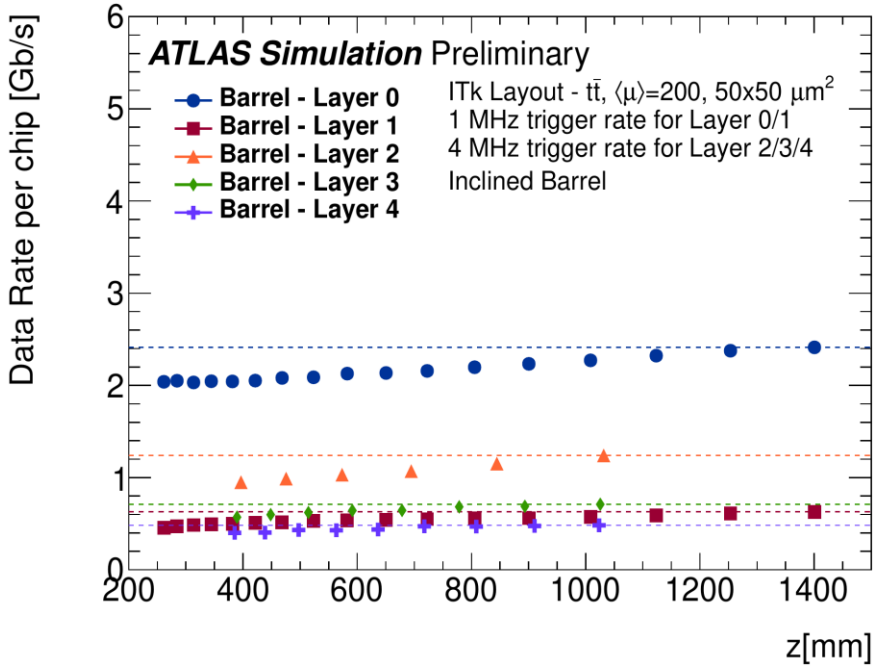
Using hit rates and projected encoding of ITk pixel readout chip: Estimate **data rates** per pixel chip

- For ITk layout, **always within acceptable limit** of data links
- Allow to use only 1 or 2 5Gbit links per quad module for most outer layers
- Regardless of pixel pitch choice

More Detail on RD53B:
Talk by Anders + Poster by Kenneth







The ITk layout – tracking CPU requirements

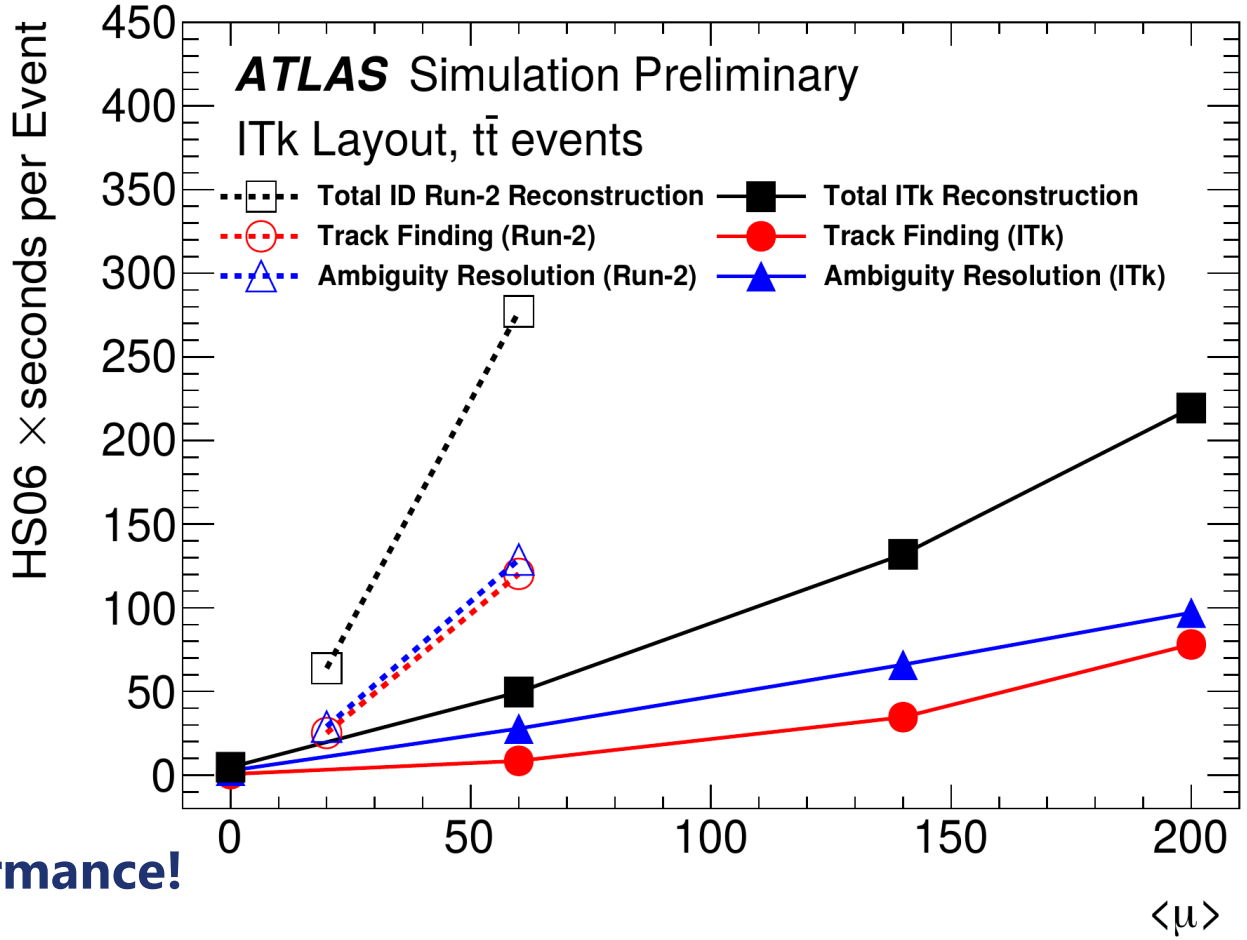
The data rates are ok – is **offline track reconstruction** also within limits imposed by the available resources?

✓ Yes – below <μ>=60 Run-2 reconstruction!

- Tuning to track reconstruction following release of TDR
- Profit from a Si-only detector

→The ITk layout fulfills our technical requirements:

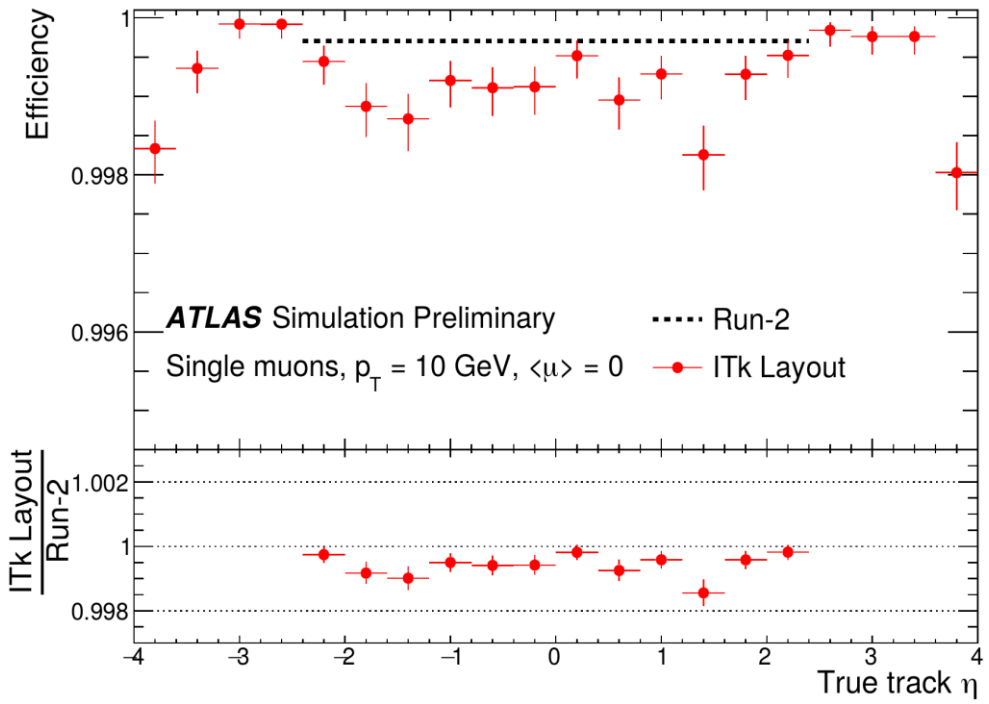
- Hermeticity with sufficient space points across full acceptance
- Acceptable data rates from all chips
- Acceptable CPU consumption in track reconstruction

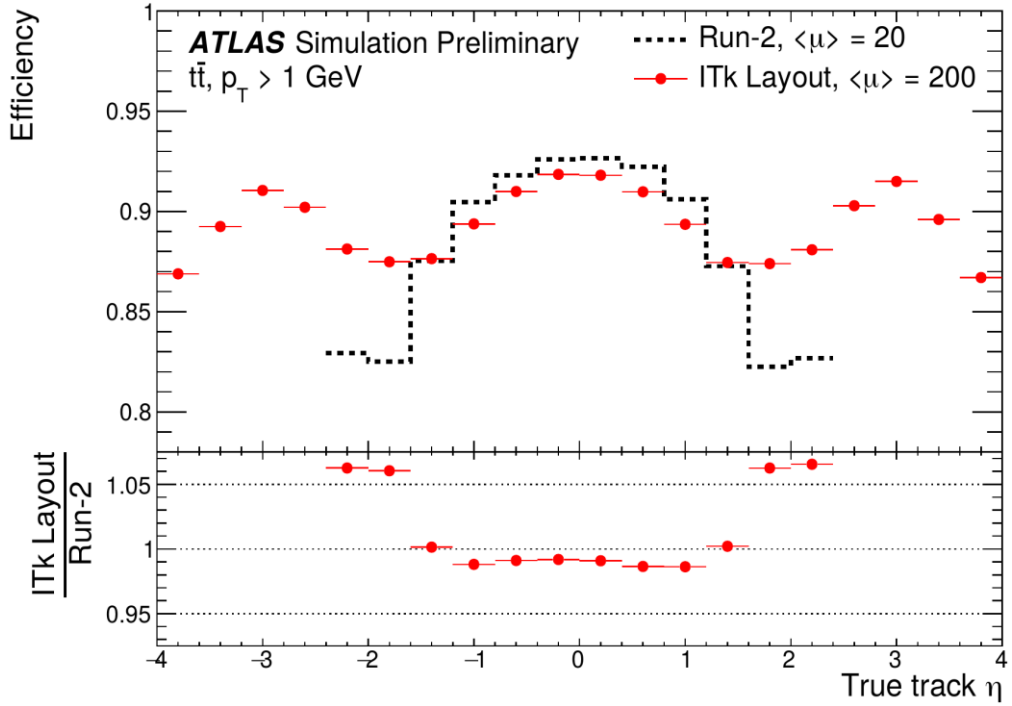


Now, let's take a look at the actual tracking performance!

The ITk layout – reconstruction efficiency

- Key performance aspect: **Tracking efficiency**
  - Fraction of charge particles in acceptance for which we reconstruct a track
- Single muons (~unaffected by material): ~100% efficiency, confirming hermeticity
- tt production in p-p collisions: **Almost match Run-2** in barrel, **superior** performance and increased acceptance in forward direction
  - Inefficiencies compared to muons: Nuclear interactions and p_T spectrum





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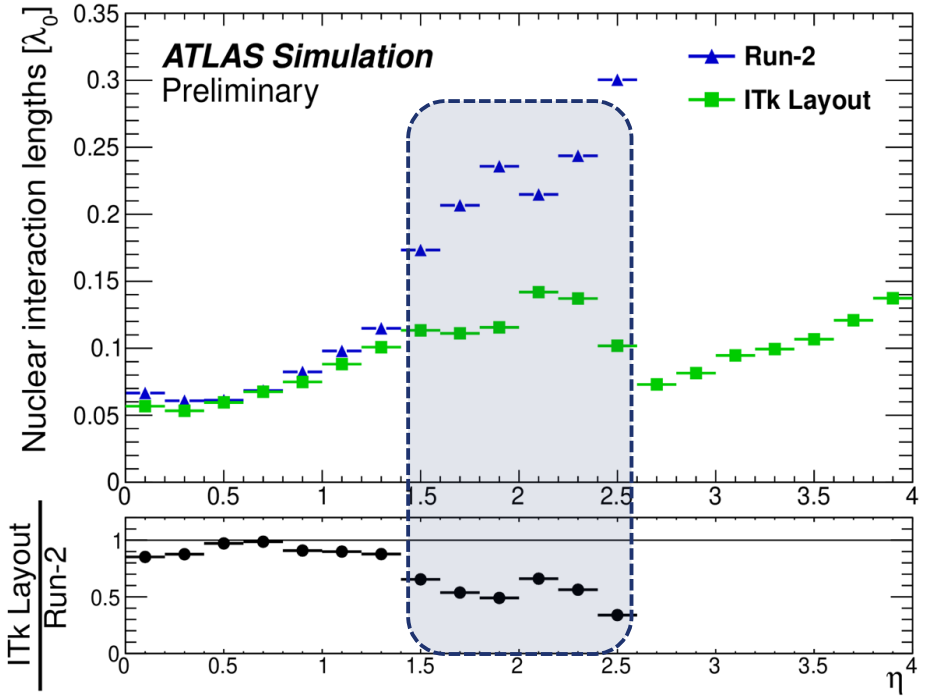
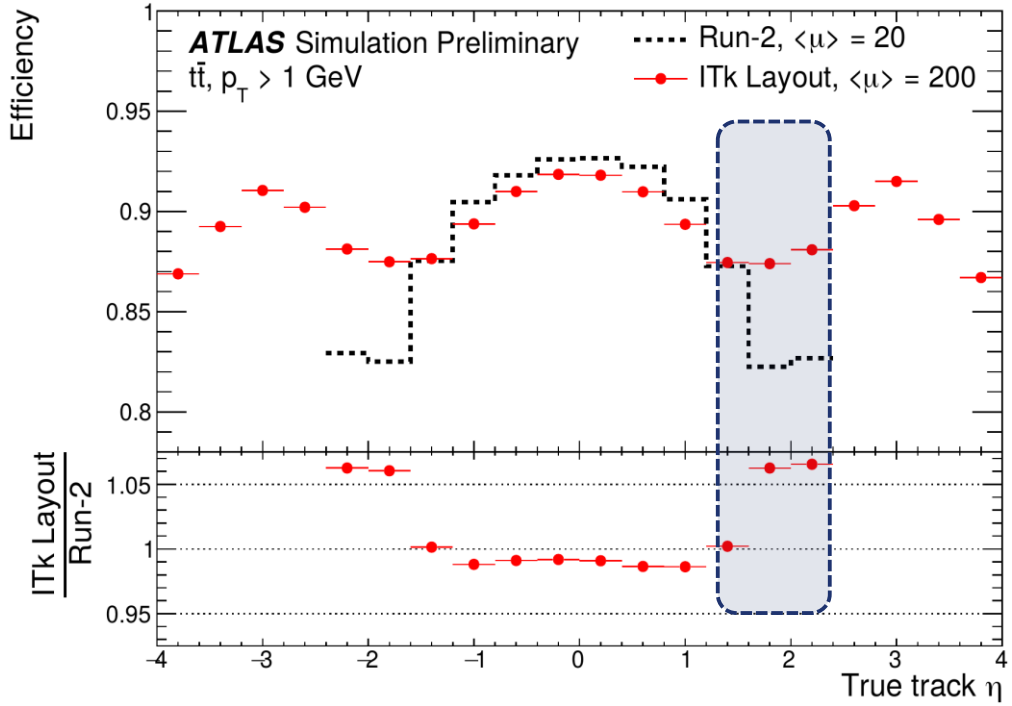
  - Inefficiencies compared to muons: Nuclear interactions and p_T spectrum
- Note: ITk layout features improved material budget in forward region

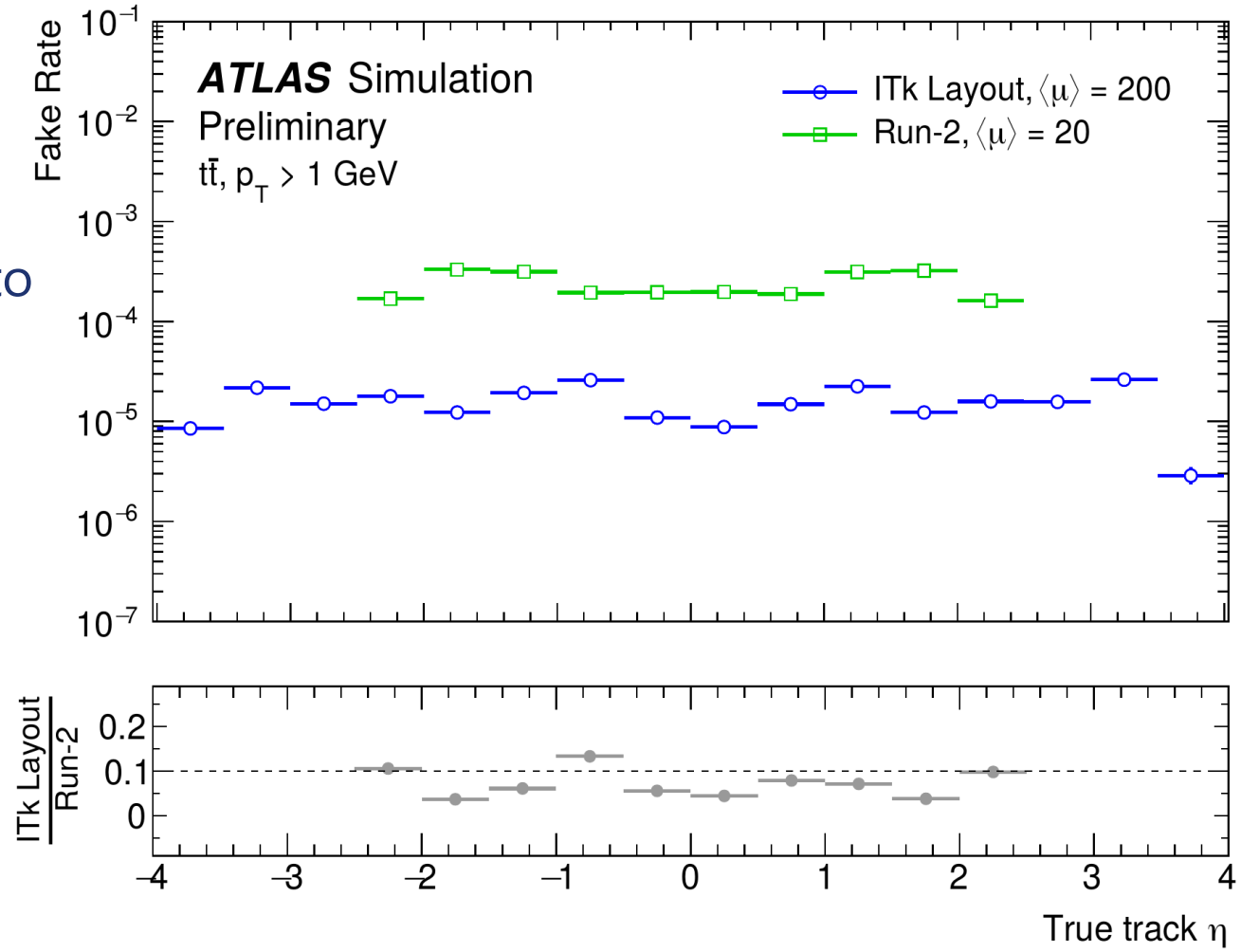




The ITk layout – fake rate

- In addition to efficiencies: Monitor the **fake rate**
- Here, measured as fraction of reconstructed tracks **not** corresponding to a single charged particle

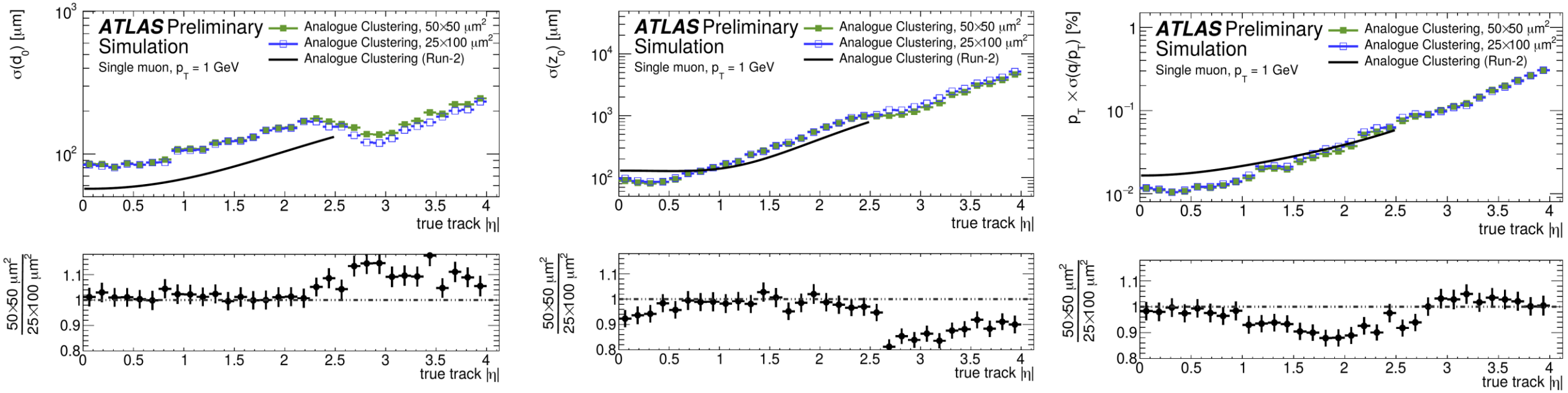
➢ Fake rates **dramatically** reduced compared to the Run-2 detector
  - Use of all-silicon detector
  - Tracking requirements fairly strict for ITk



The ITk layout – track parameter resolutions

Low-p_T: Dominated by **multiple scattering**

- ➢ Choice of the ITk pixel pitch has very small impact
- Resolution in d_0 shows noticeable degradation w.r.t Run-2
  - Due to **radius of innermost layer** – 39mm for ITk vs 33mm for IBL
  - ➢ Studies on potential mitigation in progress
- Resolutions in z_0 and p_T **comparable** to or **slightly below** Run-2



The ITk layout – track parameter resolutions

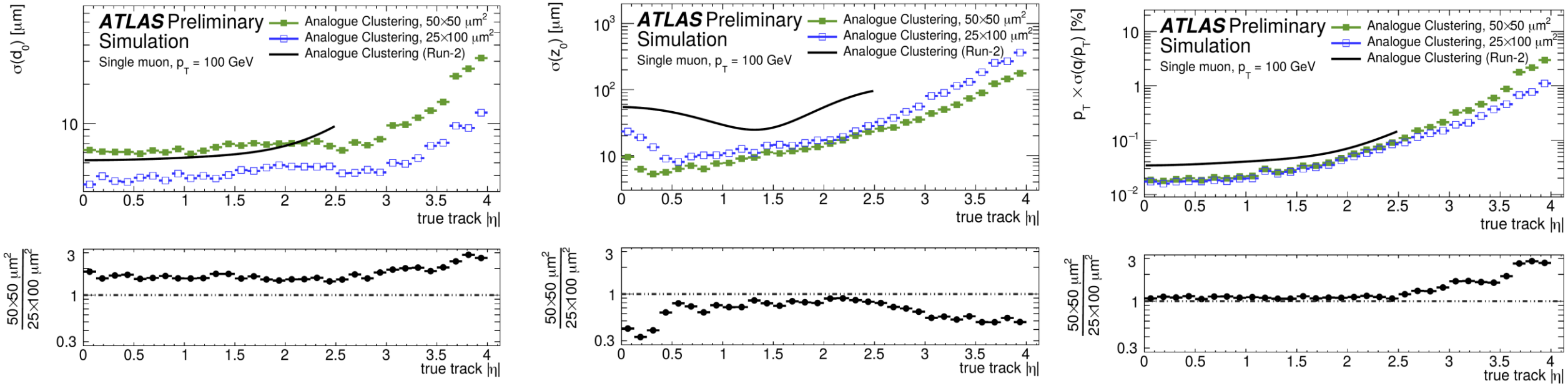
High-p_T: Dominated by **intrinsic resolutions**

➢ Choice of the ITk pixel pitch becomes important

- Resolution in d_0 **comparable** for 50x50 μm² pixels and **superior** for 25x100 μm²

➢In this regime, pixel pitch can compensate radius of layer 0

- Resolutions in z_0 and p_T **superior** to Run-2
  - Longitudinal pixel size smaller than Run-2 IBL (250 μm) for both scenarios
  - Momentum also profits from **strips** up to full ITk radius (replacing TRT)

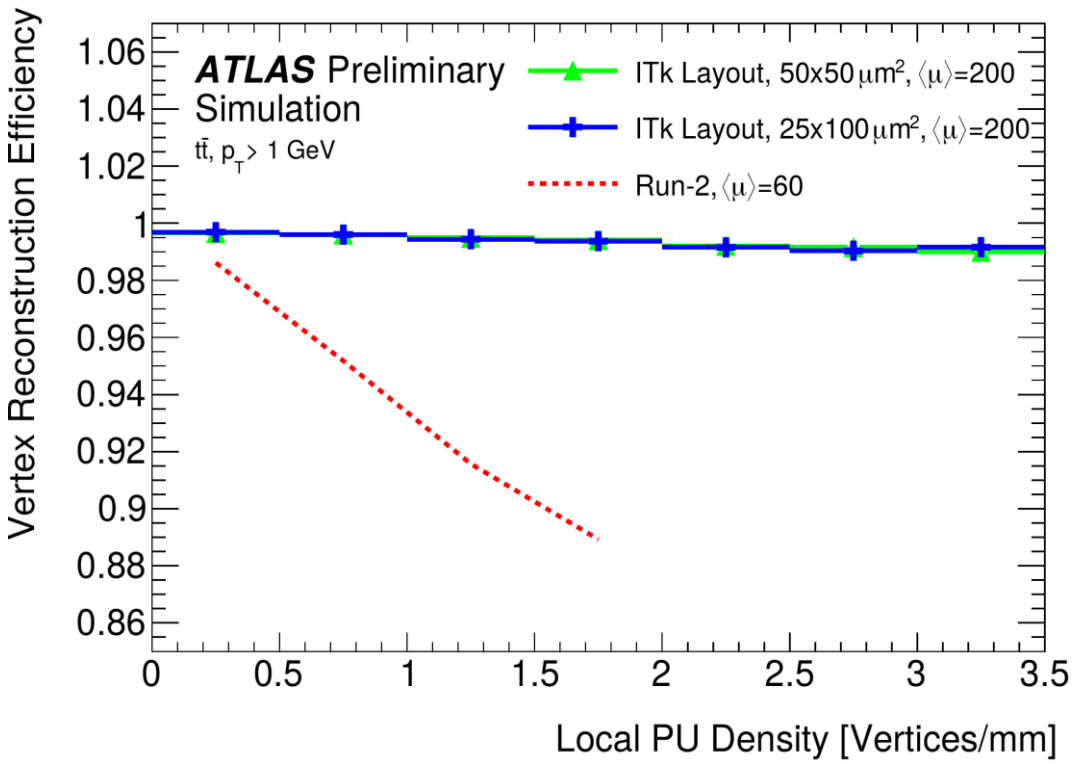


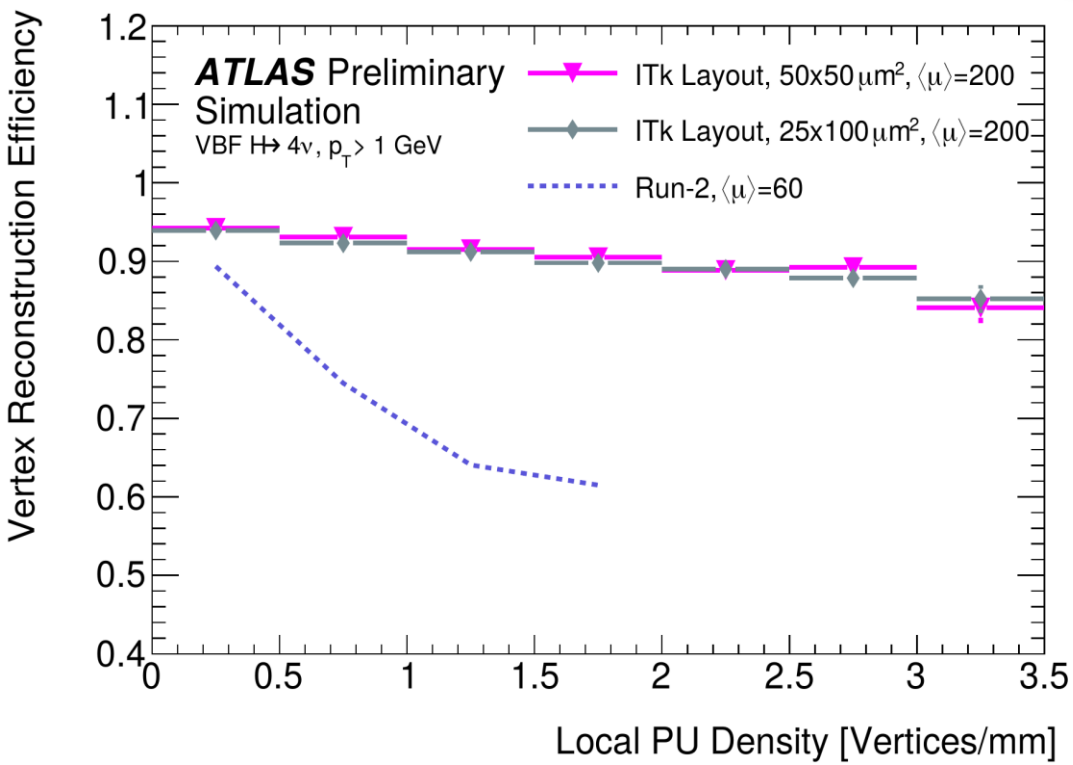
Impact of tracking performance on vertex reconstruction

- Hard-Scatter (HS) vertex reconstruction: Stability against pileup dramatically improved!
  - Profit from pileup robustness of track reconstruction and improved z_0 resolution
  - Also: New vertexing algorithm (adaptive multi-vertex fitter) in use
  - Even for challenging VBF H→invisible topology, HS vertex reliably reconstructed

More Detail: Talk by Izaac tomorrow

$$\rho_{Local} = \frac{N_{VX}(|z - z_{HS}| < \Delta z)}{2\Delta z} \quad \text{(e.g. } \Delta z = 2\text{mm)}$$

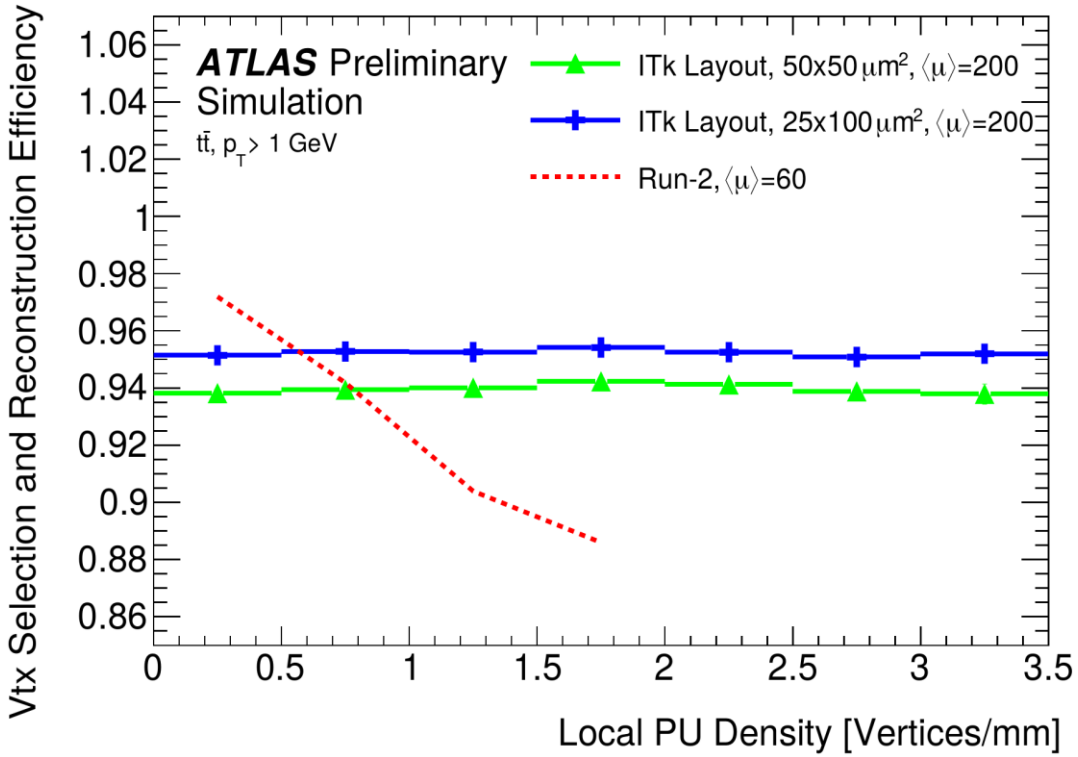


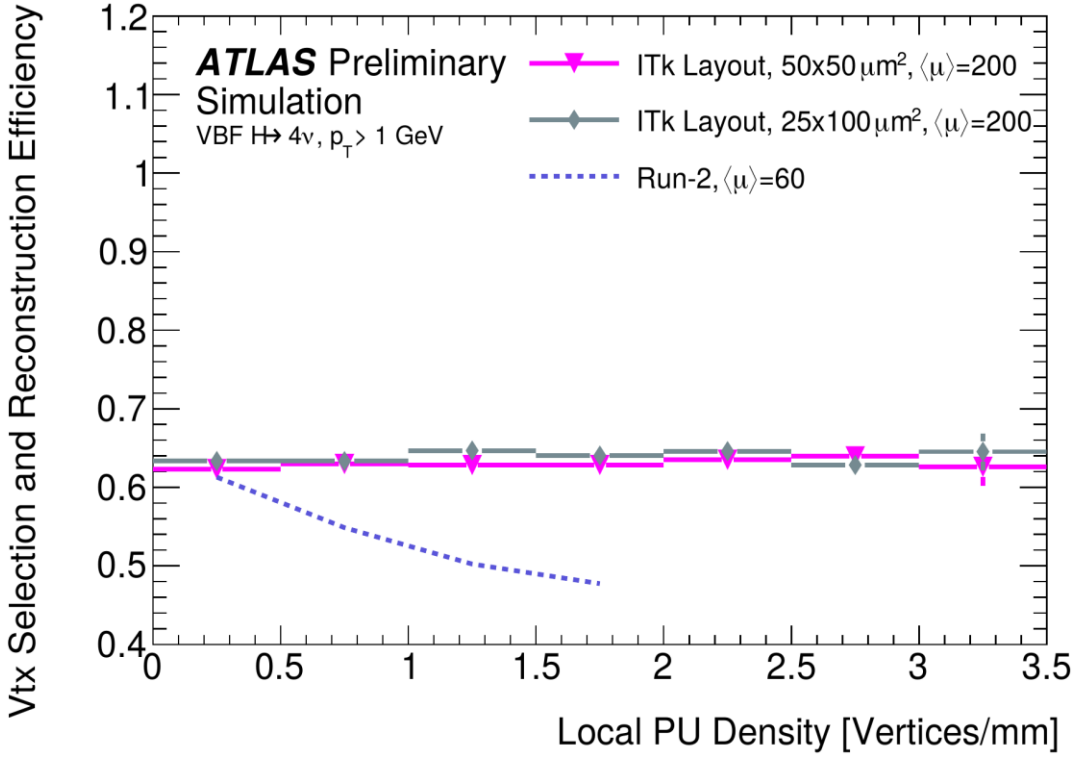


Impact of tracking performance on vertex reconstruction

Now include identification of hard scatter candidate via $\sum p_T^2$ criterion:

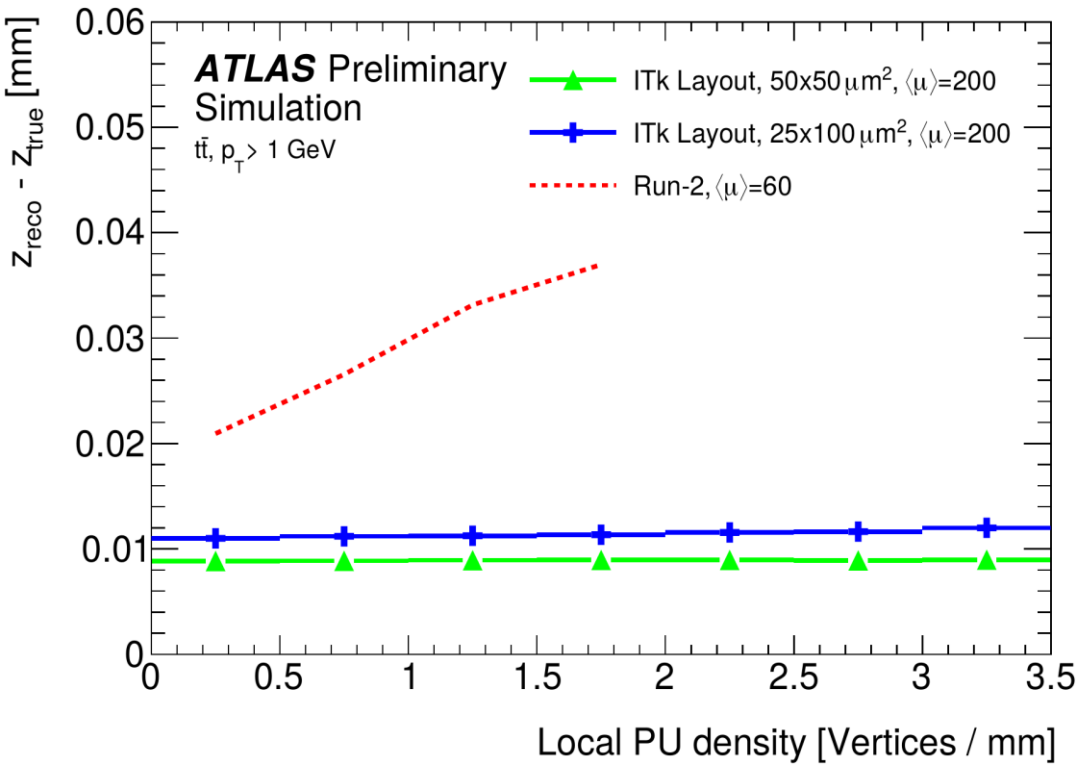
- Efficiency advantage w.r.t Run-2 retained
  - Selection efficiency itself slightly below Run-2
  - Reminder: Comparing <μ>=200 to <μ>=60 – more merged vertices for ITk
  - Can be recovered by use of selection criteria exploiting the event topology

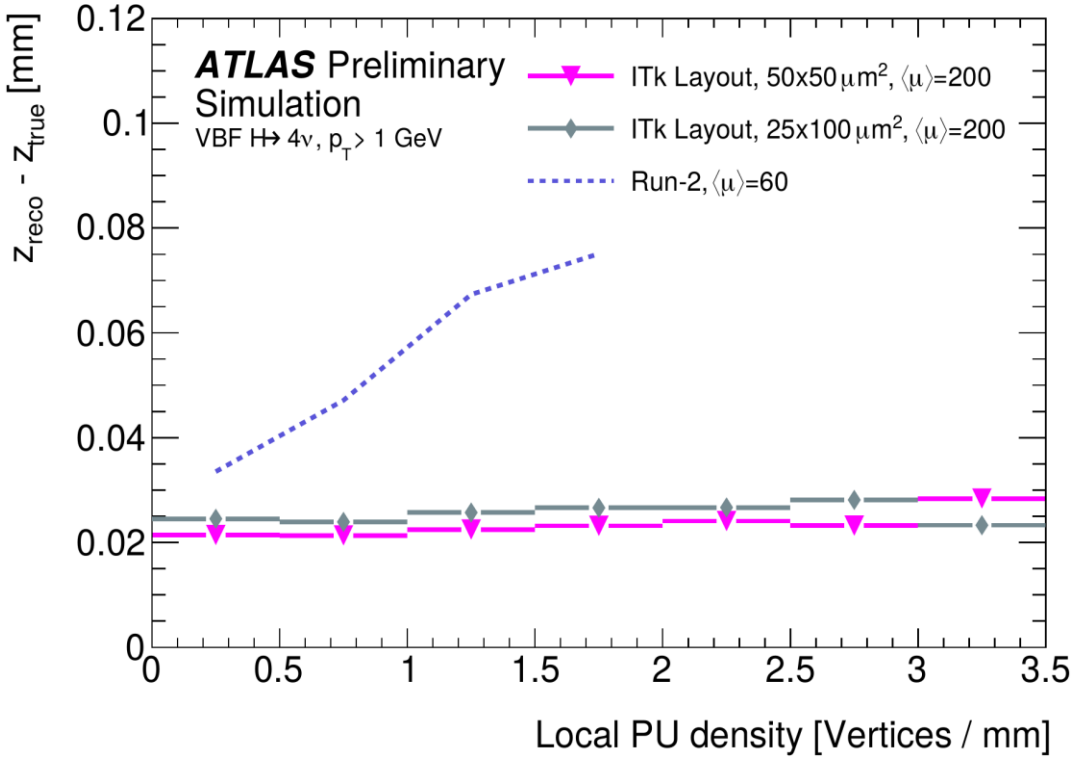




Impact of tracking performance on vertex reconstruction

- And the location of the HS vertex can be precisely measured – independently of pileup
  - Resolution mainly dominated by track multiplicity
- Marginal performance improvement for 50x50 μm² pixels





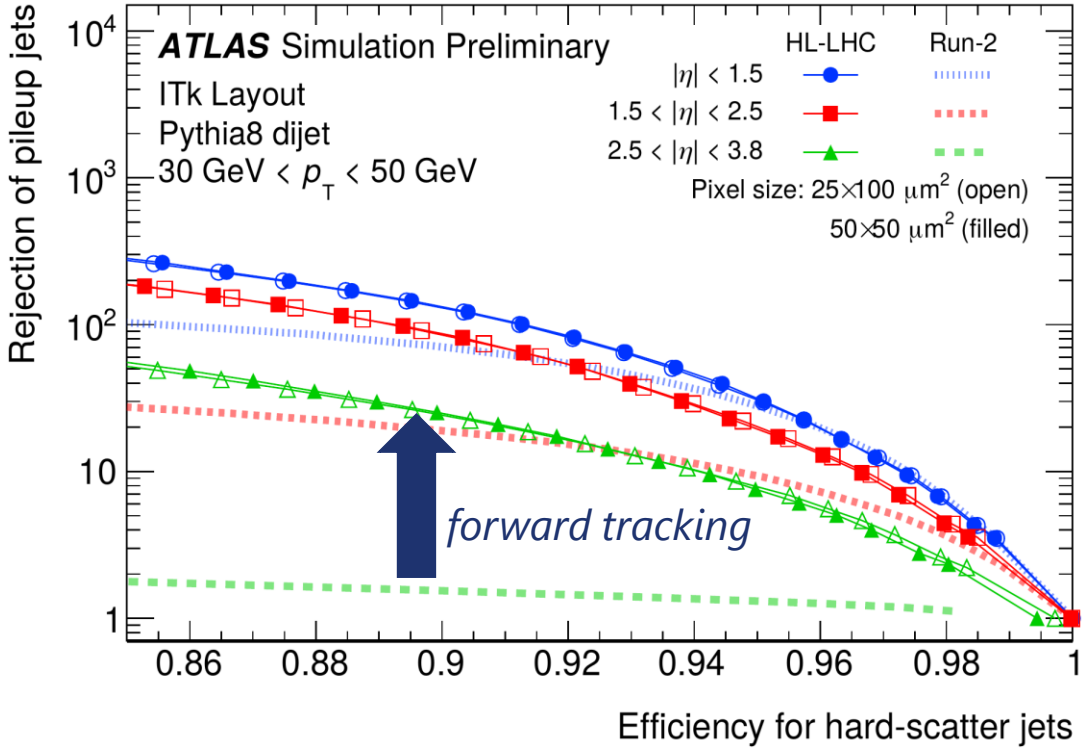
Impact of tracking performance on pileup jet rejection

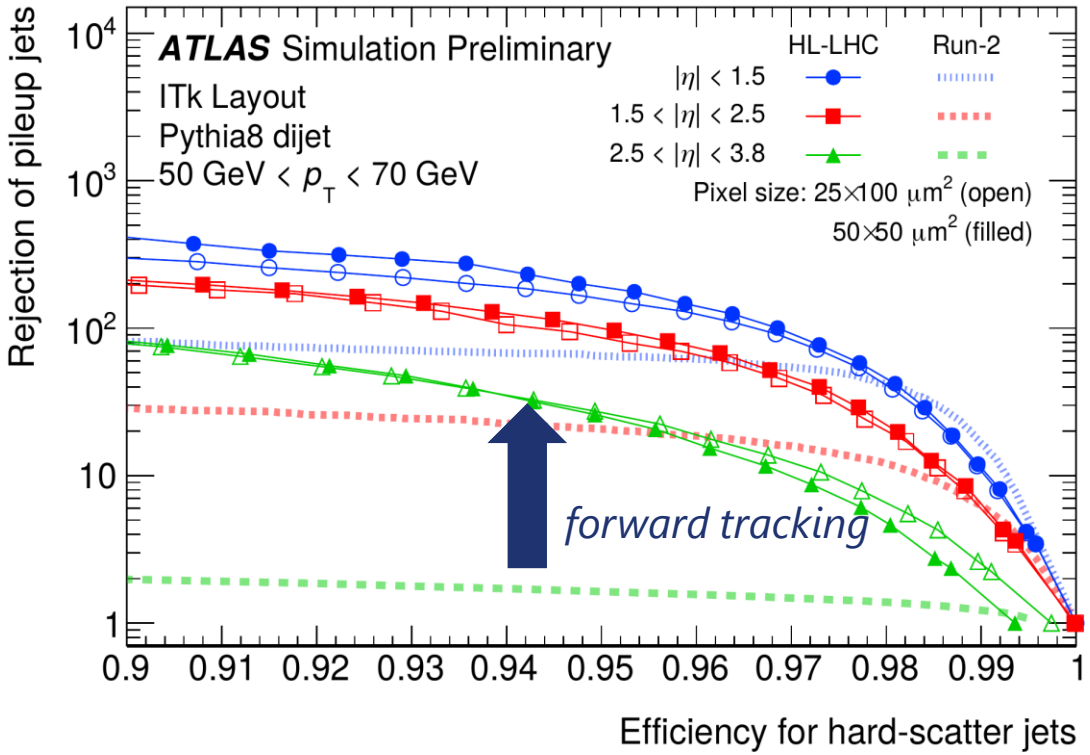
- Tracking information is used to reject **jets** from **pileup interactions**
- The ITk allows to retain Run-2-like separation power in the barrel region…
- … while greatly improving in the forward region (acceptance and efficiency)

$$R_{pT} = \frac{\sum_{\text{Track } k}^{\text{Jet tracks from HS}} p_{\mathrm{T}}^{k}}{p_{\mathrm{T}}^{\mathrm{Jet}}}$$

➢ Crucial capability at <μ>=200 – can further improve through use of timing detector!

➢ Impact of pixel pitch choice fairly small – z_0 resolution well below vertex separation in both cases



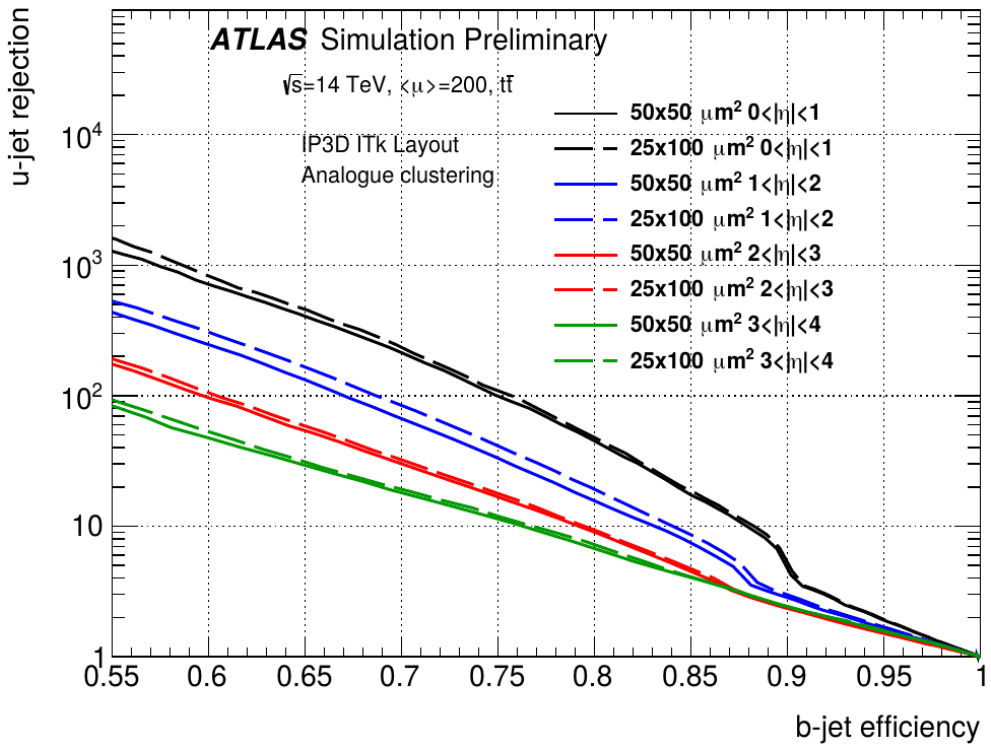


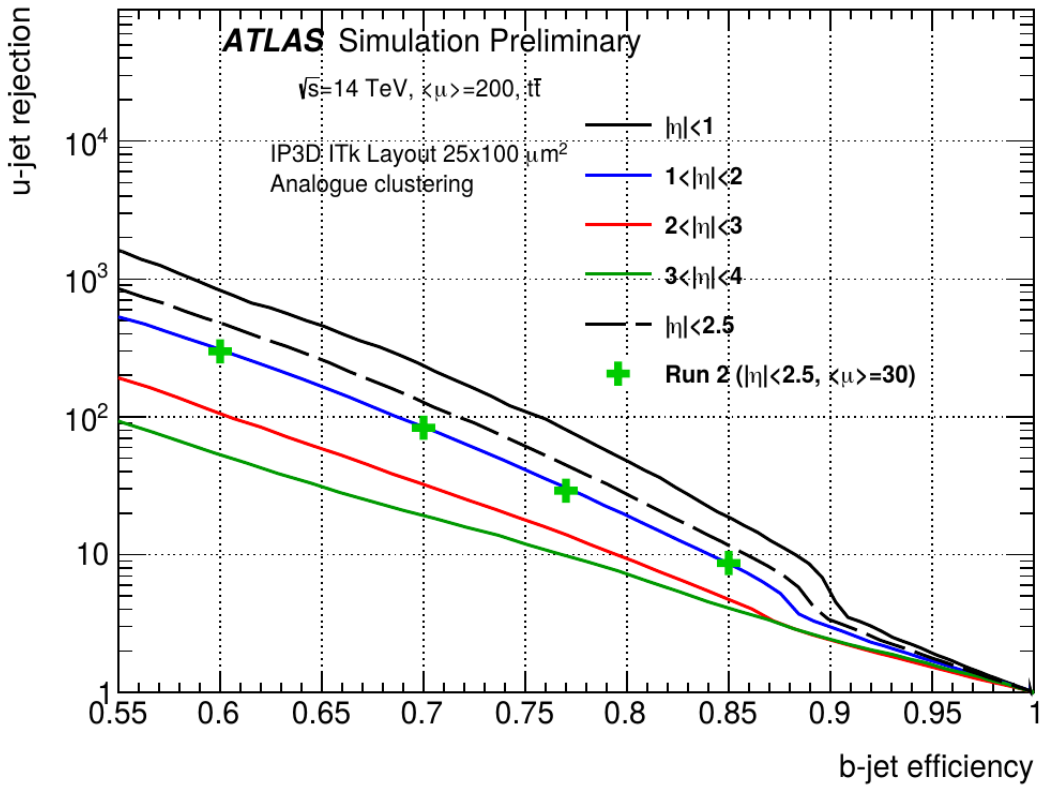
Impact of tracking performance on jet flavor tagging

- Another application of tracking: Jet flavour tagging
- ITk expected to yield stronger separation than Run-2 ID for region with Run-2 acceptance

➢ And open entirely new region of $|\eta|>2.5$ for track-based flavour-tagging!

- Use of 25x100 μm^2 pixels improves performance - due to improved d_0 resolution





Summary and Outlook

- The ATLAS ITk will enable the experiment to take data under HL-LHC pileup conditions
- Design has evolved following the publication of two TDRs
  - implementation of engineering requirements
  - fine-tuning of details
- Design changes and improvements to simulation model: Motivate new round of performance studies
  - Also evaluate impact of pixel pitch choice
- Updated ITk layout matches or exceeds current ATLAS Run-2 tracking performance in nearly all cases
  - one exception: Low-p_T d_0 resolution – limited by layer 0 radius – studies in progress
- Resulting performance of vertexing, pileup jet rejection and jet flavour tagging also compare favourably to Run-2