

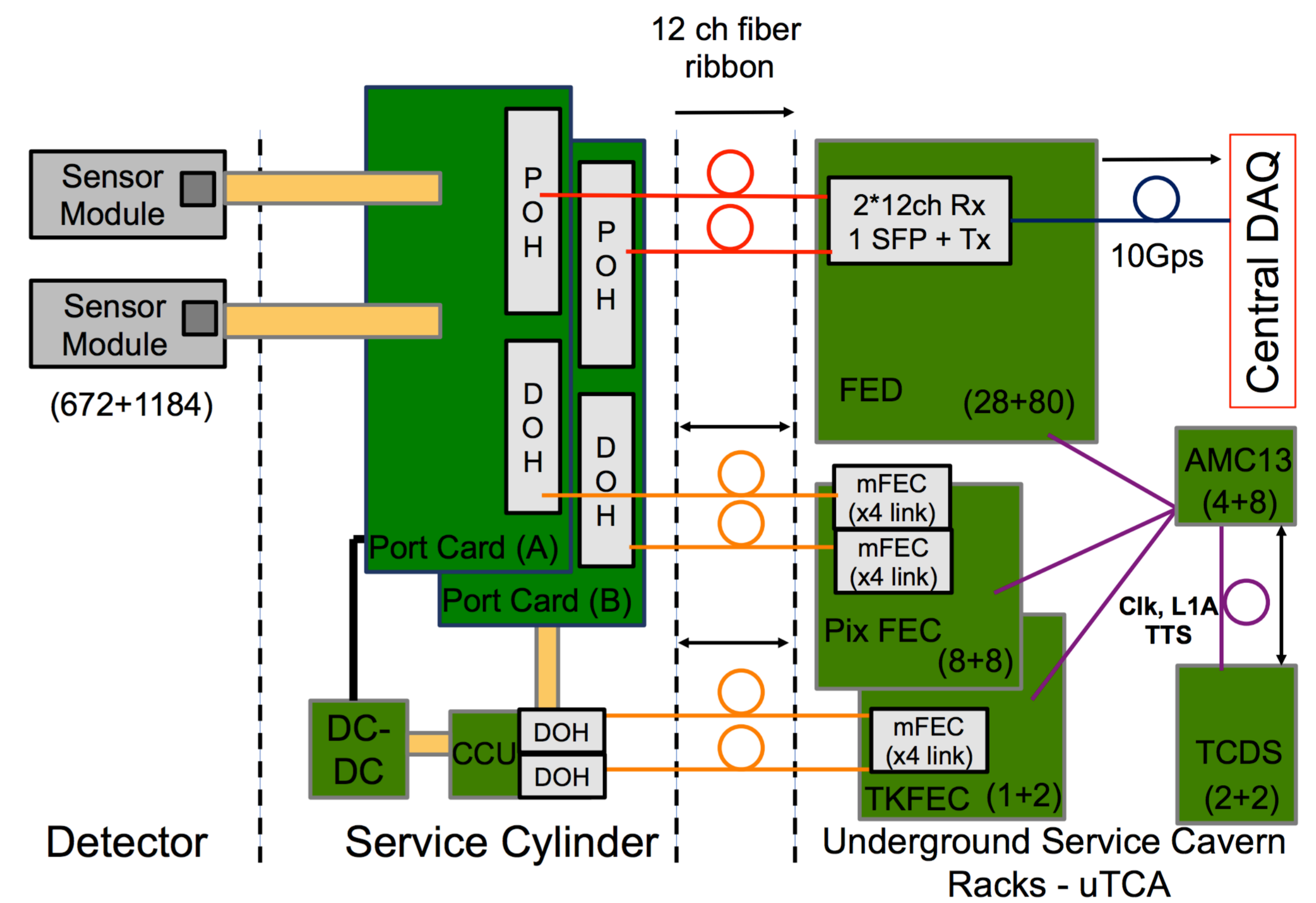
## Introduction: Phase-I Pixel DAQ

- uTCA based backend DAQ
- Two kinds of Front-End Controllers (FEC)
  - *PixelFEC*: Distributes trigger, clock, fast signals, and program modules
  - *TrackerFEC*: Program auxiliary electronics
- Front-End Driver (FED) to read out data

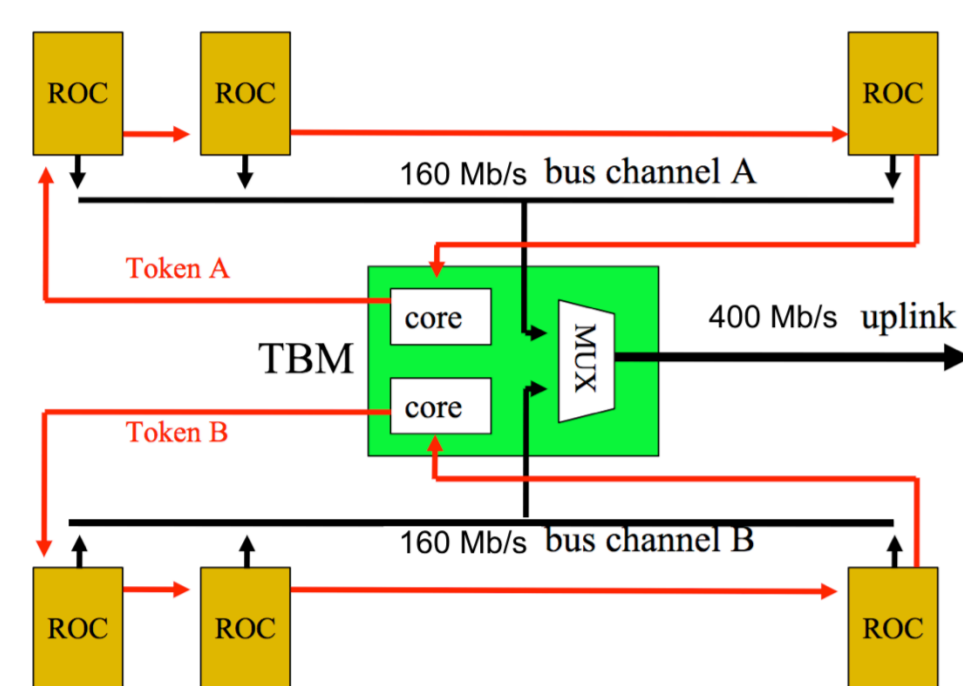
## Motivation of the firmware upgrade

- PixelFEC programs module in a sequential manner for a given crate
  - Longer time needed to configure detector
  - Slower recovery from detected soft errors
- So, make it faster! This will have a direct impact on pixel operation during data taking

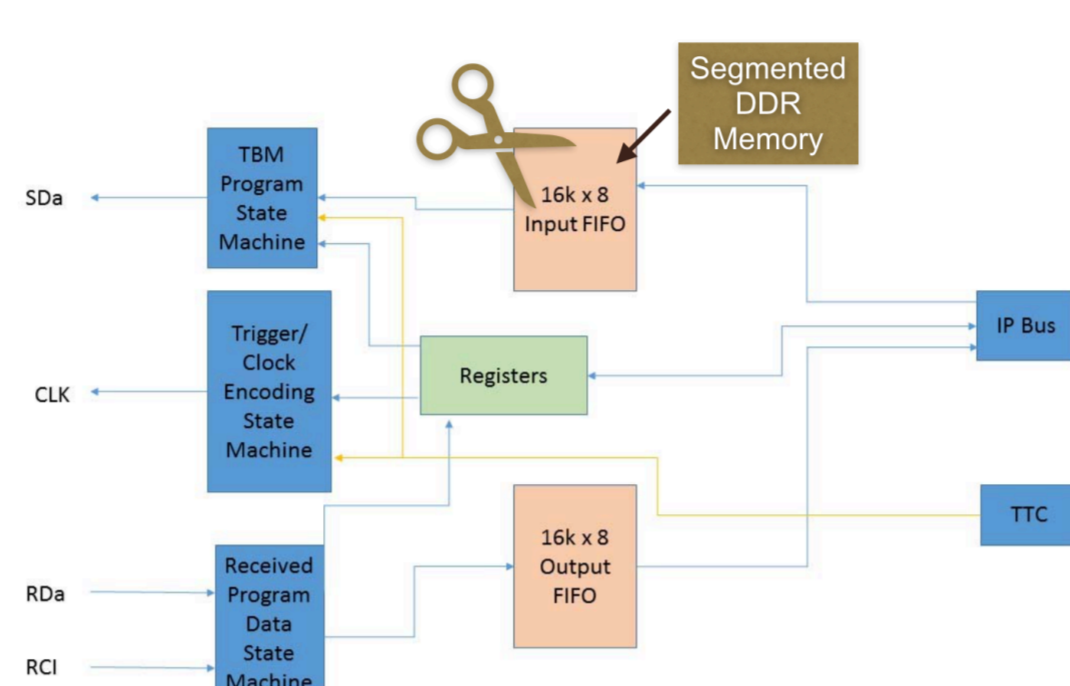
## DAQ Architecture



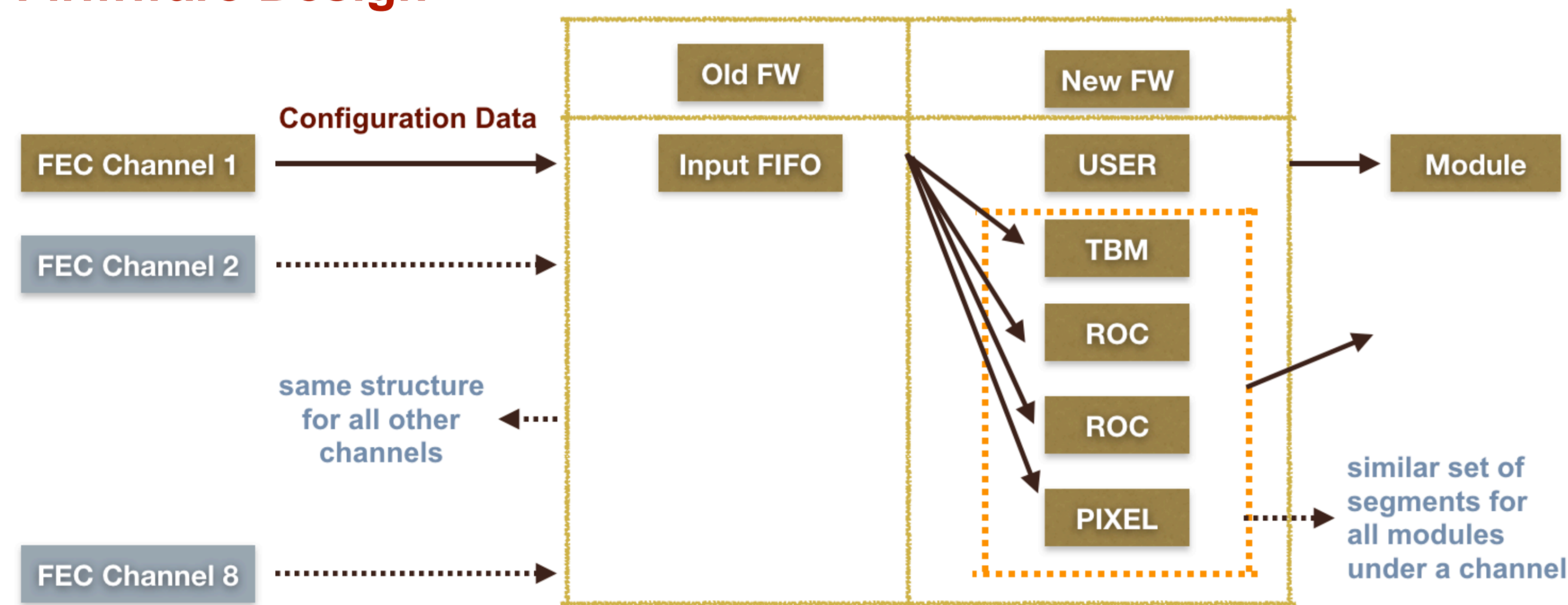
## Schematic of a module



## PixelFEC channel



## Firmware Design



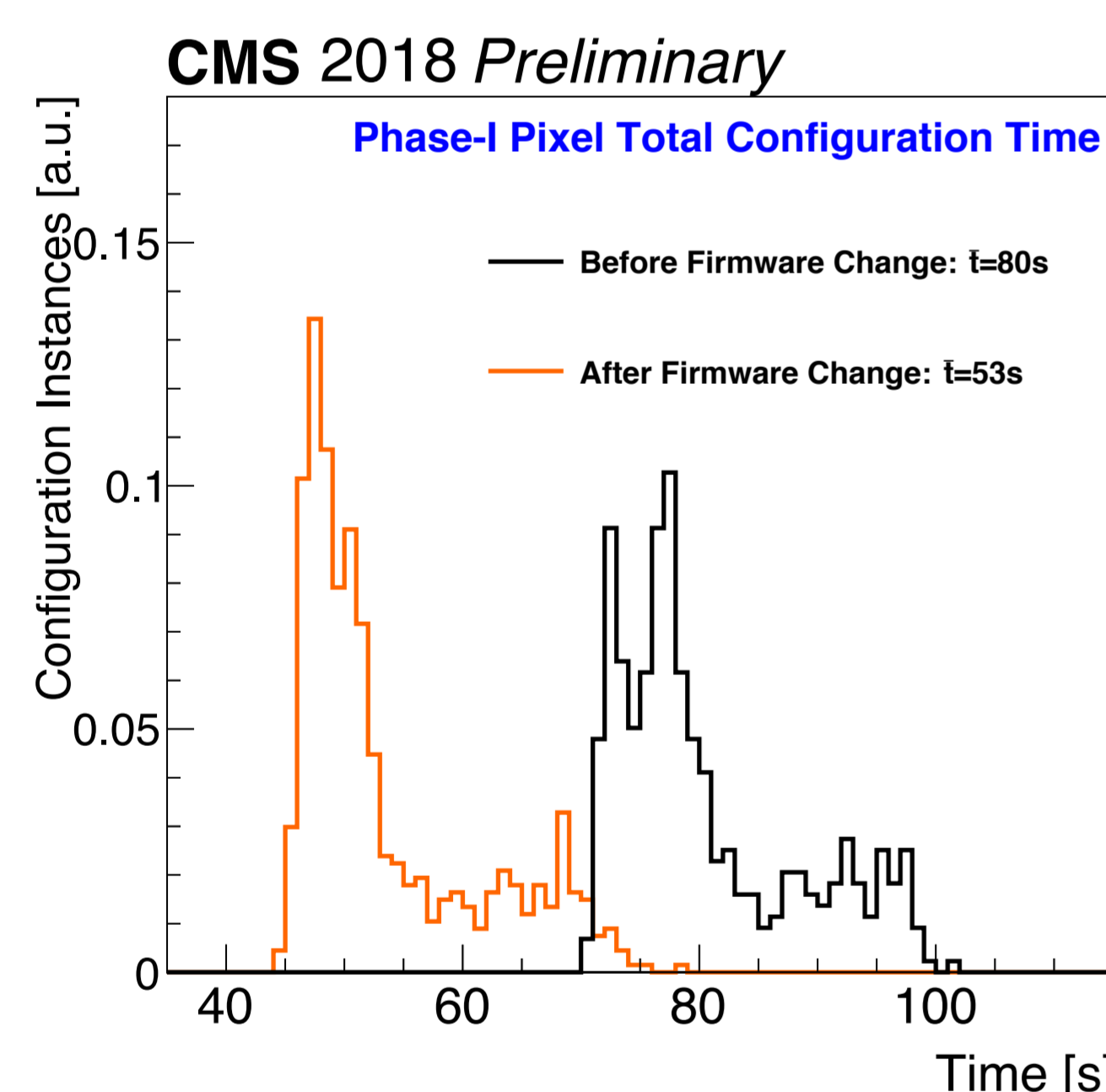
### Old Firmware

1. Program storage in FIFO
2. Load configuration data from remote server and write to FIFO
3. Limited FIFO size, 16kB per PixelFEC channel

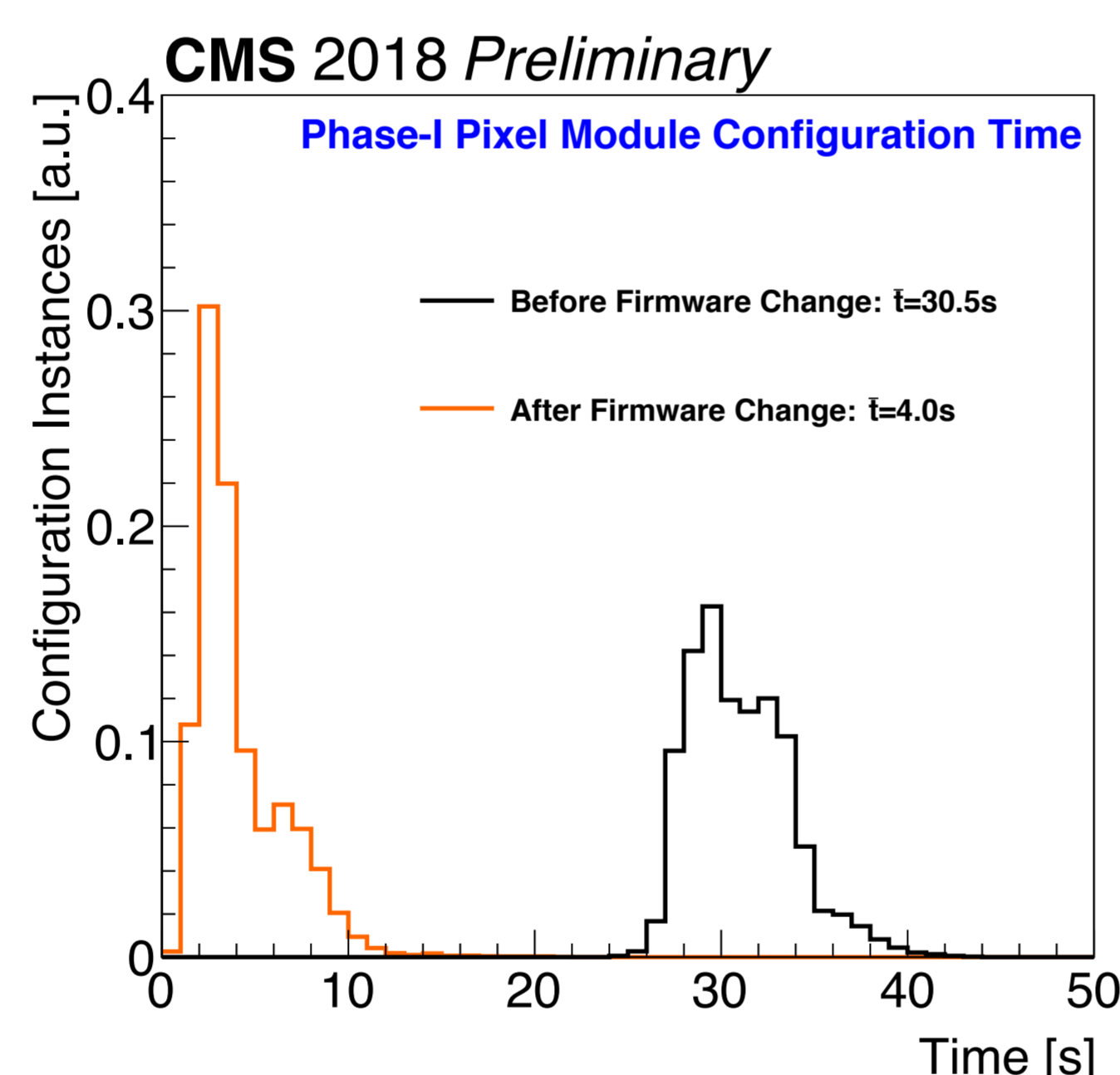
### New Firmware

1. Program storage in DDR3 (on FC7 card)
2. Segmented memory structure
3. Localized configuration data
4. Larger memory, 0.5 MB per segment. Total 113 segments per PixelFEC channel

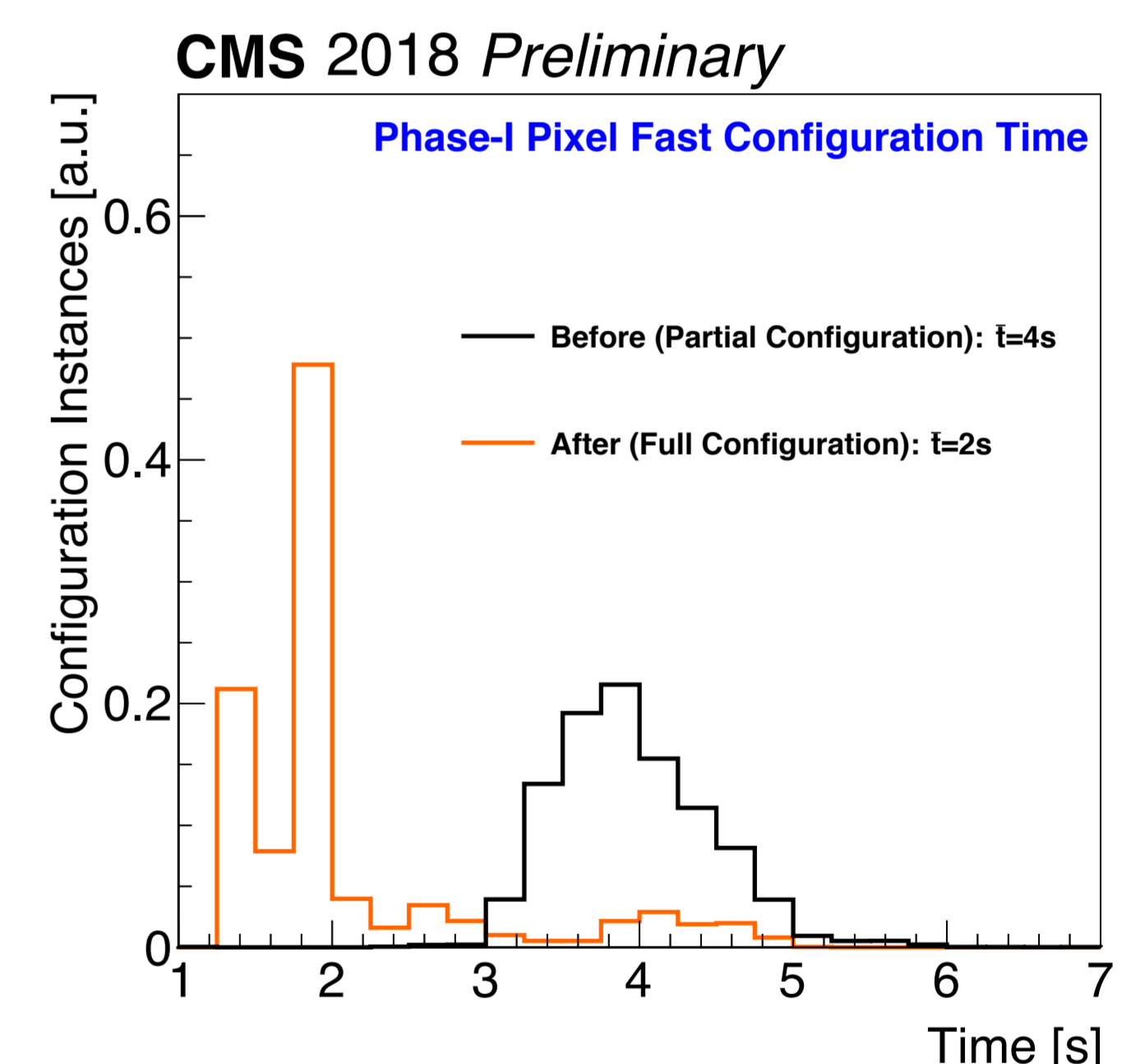
## Performance



Total configuration time of the pixel detector reduced by ~30 sec after the firmware change



- During each state transitions (stop/start, pause/resume, halt/configure) we reprogram the detector
- Partial configuration has only minimal ROC level settings, where as full configuration consists of individual pixel level programming (~25 times more data)
- After the firmware update, we now can reprogram the detector with full configuration during state transitions even quicker than earlier



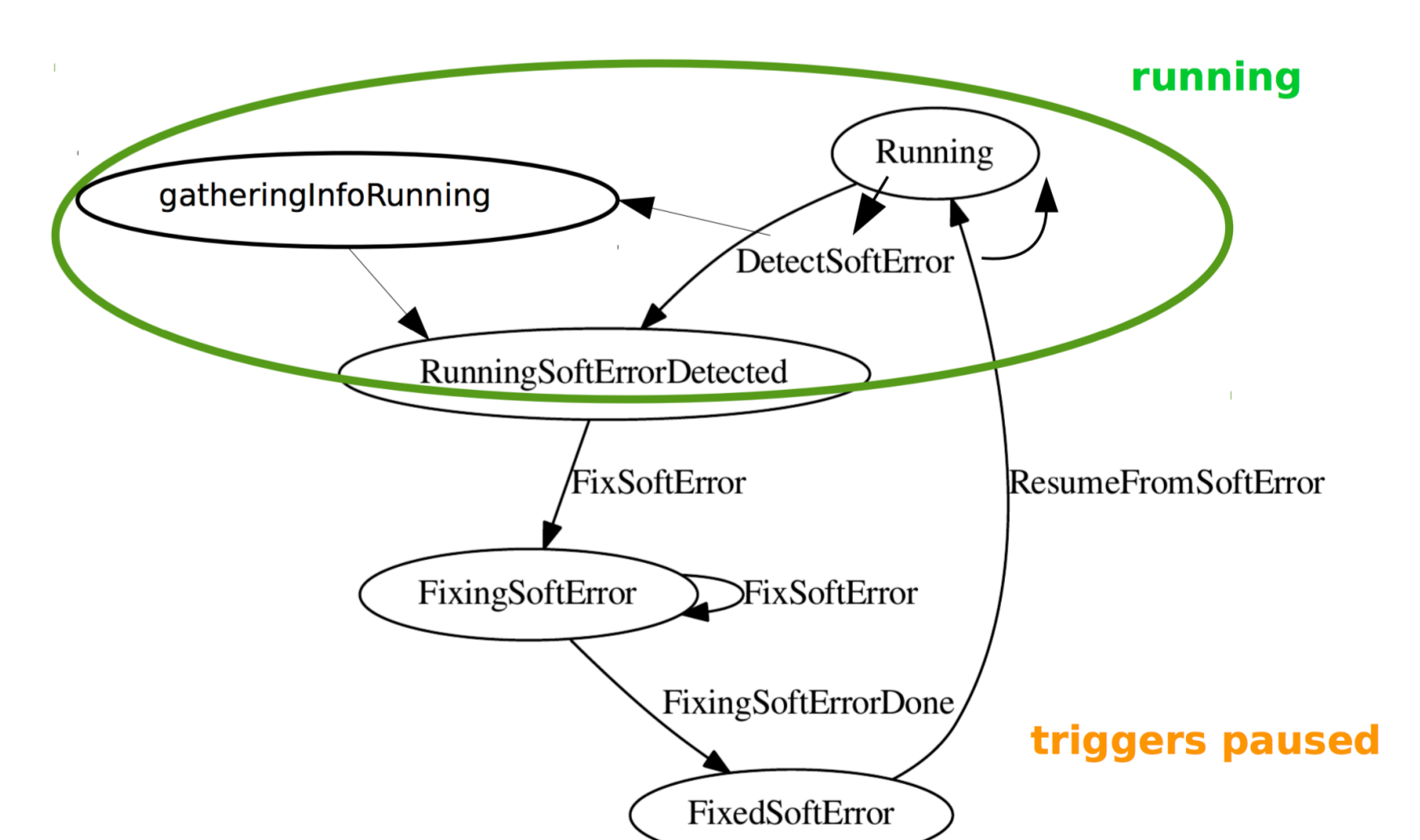
## Single Event Upset (SEU)

- An ionizing particle passing through sensitive part of the front-end electronics can flip a memory bit and may disrupt the normal functioning
- Pixel detector resides very close to the interaction point, and with very high instantaneous luminosity at the LHC, the rate of SEU in front-end electronics is non-negligible

## Auto-Recovery from SEU

- Pixel online software runs a mechanism which can automatically detect any possible SEU during data taking and take action accordingly
- Previously, during this recovery, a complete pixel level programming was not possible since it would have created a lot of down time (data loss)
- Now we have a more complete pixel level reprogramming and quicker recovery from detected soft errors

## Finite State Machine scheme



## Summary

- DDR based firmware was designed, and integrated to pixel online software
- It was successfully commissioned, and deployed for operation of Phase-I Pixel detector in 2018
- Reduced the configuration time of the detector dramatically
- Full pixel level configuration during state transitions, modules are always in a defined state
- More complete and faster recovery of modules affected by SEU during data taking
- Faster calibrations using DDR based firmware

## Future Scope

- Take advantage of the pre-loaded localized configuration data and use a fast-signal based command (BGo) issued by Trigger Control System to refresh part of the front-end in regular interval
- Some of the other calibrations still take really long time to finish and not possible to cover them during normal operation period. Adapt calibration techniques with DDR based firmware to speed up the timing significantly.