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Firmware oriented trigger algorithm for CMS Drift Tubes in HL-LHC

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A full replacement of the muon trigger system in the CMS (Compact Muon Solenoid) detector is envisaged for operating at the maximum instantaneous luminosities expected in HL-LHC (High Luminosity Large Hadron Collider) of about $5 - 7.5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$. Under this scenario, the new on detector electronics that is being designed for the DT (Drift Tubes) detector will forward all the chamber information at its maximum time resolution. A new trigger system based on the highest performing FPGAs is being designed and will be capable of providing precise muon reconstruction and Bunch Crossing identification. An algorithm easily portable to FPGA architecture has been designed to implement the trigger primitive information from the DT detector. This algorithm has to reconstruct muon segments from single wire DT hits which contain a time uncertainty of 400 ns due to the drift time in the cell. This algorithm provides the maximum resolution achievable by the DT chambers, bringing closer to the hardware system the offline performance capabilities. The results of the simulation and of the first implementations in the new electronics test bench will be shown.

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