Atlas ITk pixel read-out simulations

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Experimental Particle Physics

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Overview

The RD53 pixel chip was designed to meet the spatial resolution and datarate demands of the high collision rate and pile-up of the High Luminosity LHC event environment. The high speed data read-out of RD53 chips requires high performance data acquisition (DAq) infrastructure, which must stay within the material budget of the Atlas Inner Tracker (ITk). **This poster shows the results of RD53 chip readout simulation with HL-LHC type events: the expected datarate is within specified limits using an optimised encoding algorithm.**

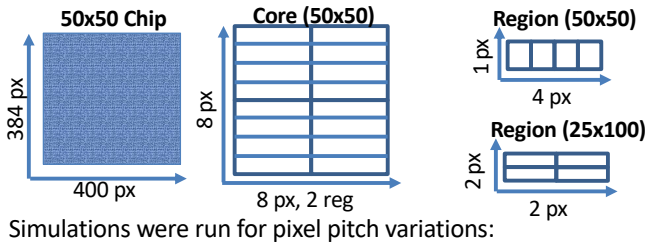
ITk Pixel Data Transmission Specification

A maximum restriction on the data readout rate comes from the cabling in the DAq system. The data must be transported off the chip and out of the ITk environment using electrically robust links with as little mass as possible. Links have a physical limit of 5.12 Gbps, a safety factor of 70% is applied to allow for variance in throughput → **3.58 Gbps average datarate link limit**.

RD53 chip [CERN-RD53-PUB-17-001]

Following a period of R&D the RD53 readout chip was designed for the Atlas ITk. The chip has 400x384 readout channels with pixel area 2500µm² and 4MHz trigger capability.

RD53 readout encoding is based on 4x1 (2x2) **ηxϕ** pixel regions, and 8x8 (4x16) pixel cores for 50x50µm² (25x100µm²) pixels.



Simulations were run for pixel pitch variations:

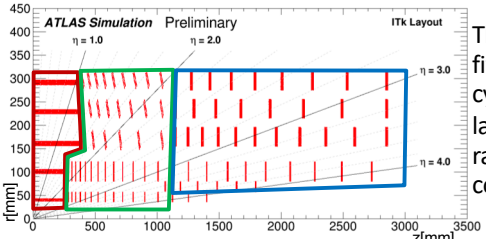
Pixel pitch (ηxϕ)	Sensor Area	rows	cols
50x50 µm²	20x19.2mm²	394	400
25x100 µm²	20x19.2mm²	688	200

Simulation

The simulation used the full Atlas simulation chain for an event sample of ttbar + mu=200 pile-up. Secondary interactions are included. No radiation effects are simulated.

Event Generation → Material Deposition → Digitisation

Track reconstruction then associates clustered hits to a single trajectory. For this analysis digital clusters per chip were used to calculate pixel occupancy.



The barrel region has five concentric cylindrical barrel layers at increasing radii form the collision point (L0-4).

Barrel detector orientation is flat in **centre** and **inclined** at edges to compensate for increased track angles and hence limit cluster size. The **endcap** has five layers at the end of barrel with increasing z position (R0-4).

The L0 trigger acceptance is 4MHz (1MHz) for layers 2-4 (0-1).

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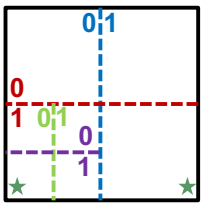
RD53B Encoding [CERN-RD53-PUB-19-001]

RD53B optimise datarates using compressed hit information (ToT + Addressing) packaged into streams of data frames.

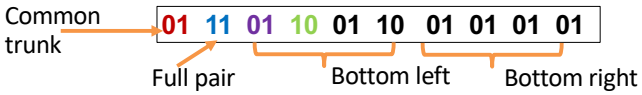
ToT: Time-over-Threshold information provides 4 bits per pixel → 16 bits per region, ordered structure retains pixel identity. Further compression possible (not implemented here).

Core Addressing: Cores addressed: 12/13 bits
X(Y) position: 6(6/7) bits per position → 64 > 400/8 (64 > 384/8). Neighbouring core address suppression possible

In-core Addressing: bit-tree
Core occupancy is encoded by iterative procedure until all hit pixels mapped:
- Split array and assign bit pair
  bit: hit=1, empty=0
- For each hit section:
  Split array and assign bit pair…



One bit pair per iteration→ 6 pairs for single pixel in 64 array

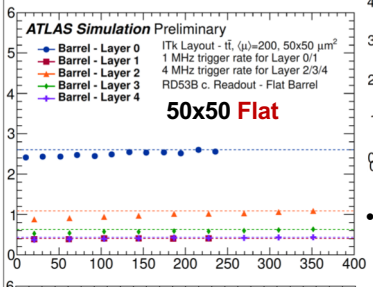


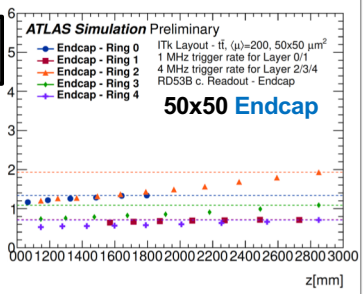
Framing: region data is grouped into frames of 64 bits, with 2 bits as "Aurora frame header" (64/66bit encoding). Additional Aurora overhead for "register frames" of 4%.

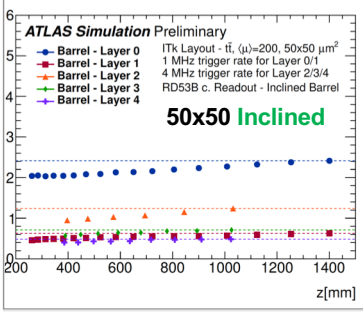
Streaming: multiple/part events
First frame bit for new stream flag, 8 bit event tag, 11 bit tag.
Stream ends when remaining bits in frame < (N_{hc} * E-step) bits.
- N_{hc} = number of hit cores, E-step = step size (1 bit min.)

RD53B Average Datarate Prediction [ATL-PHYS-PUB-2019-014]

Result: Encoded datarate within 3.58 Gbps specified link limit







- Low occupancy events combine information to single stream → minimize unused bits
- High occupancy events are split → standardise unused bits
- Stream length tuned using E-step → unused bits per stream

Max datarate per region:

Pixel type	Flat	Inc.	End.
50x50 [Gbps]	2.6	2.41	1.93
25x100 [Gbps]	2.22	2.37	1.94

Summary & Future

Expected RD53 encoded datarate lies within 3.58 Gbps specified link limit

- Fully simulated HL-HLC event environment and ITk layout
- RD53B encoding: addressing, framing, streaming
- RD53B data encoding implemented in ATLAS simulation

Further possible optimisation
- ToT compression: maximal 4 bits per pixel considered here
- E-step optimisation: control stream size per region