Overview of CMOS sensors for future tracking detectors

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on behalf of the CERN RD50 HV-CMOS collaboration (U. Liverpool, IFAE, U. Barcelona, U. Seville, IFCA, CPPM, JSI, FBK, HEPHY, U. Lancaster and IFIC)

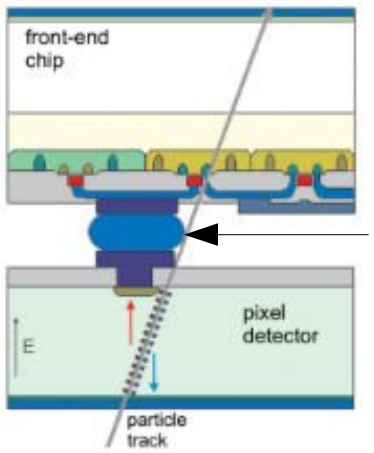
Outline

- Introduction to depleted CMOS sensors.
- Large vs. small collection electrode structure.
- Current challenges for depleted CMOS sensors.
- CMOS foundries available.
- Summary of CERN RD50 collaboration CMOS activities.
- CMOS development project within CERN RD50 collaboration.
- Conclusion.

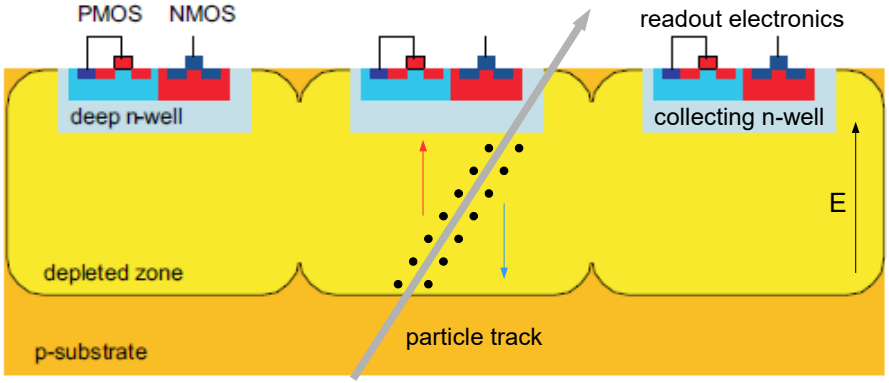
Introduction to depleted CMOS sensors

- Current large pixel detectors in HEP mostly follow a hydrid approach.
  - Independent development of sensor and readout electronics technologies: high radiation tolerance ($2x10^{16}$ 1 MeV n_{eq}/cm^2) and particle rates (1000 MHz/cm^2).
  - Bump-bonding is an expensive and complex process with limited output pace.
  - Several layers with significant material thickness (~300 μm) restrict accuracy of particle trajectory measurement.
- Depleted Monolithic Active Pixel Sensors (DMAPS).
  - Integrate the sensing diode and the readout electronics in the same CMOS wafer.
  - Charge collected mainly in depleted area (from few to hundreds of μm) created by applying reverse bias.
  - Pixel electronics placed inside an isolated well.
  - Possibility of noise reduction and higher signal sensitivity.
  - Commercial CMOS fabrication process and integration leads to an easier production, a large cost reduction and faster fabrication.
  - Material budget saving: reduced thickness (~50 μm).
- There is still sufficient room for improvement in several aspects of depleted CMOS sensors.
  - Radiation tolerance: 10^{15} 1 MeV n_{eq}/cm^2 → > $7 \cdot 10^{17}$ 1 MeV n_{eq}/cm^2.
  - Timing resolution: 10 ns → < 5 ns.
  - Fast readout: particle rate 100 MHz/cm^2 → > 1000 MHz/cm^2.

Ref: T. Hemperek, PoS (Vertex 2017) 034



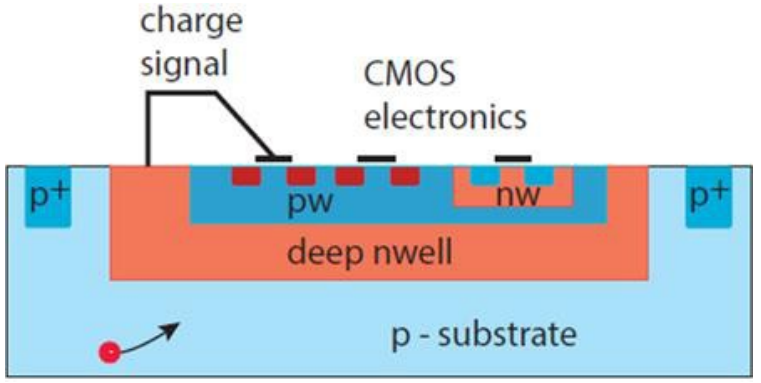
Hybrid pixel detector



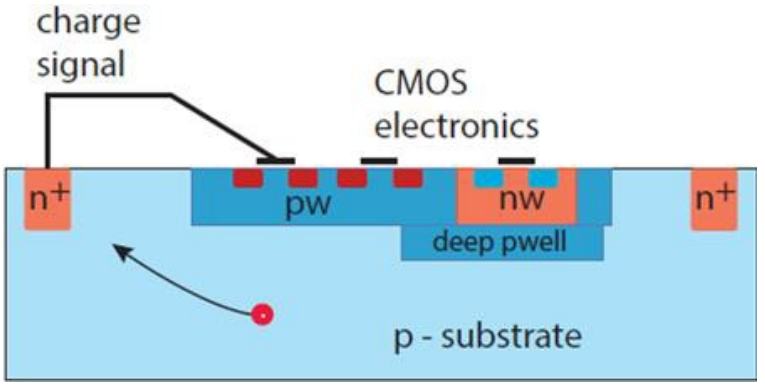
Depleted CMOS monolithic active pixel sensor

Large vs. small collection electrode

- Two main n-on-p CMOS sensor design concepts depending on collection electrode size (fill factor).
- Large fill-factor structure.
  - Sensing diode made up of p-substrate and deep nwell: electronics inside charge collection well.
  - High resistivity substrates available (up to 3 kΩ·cm).
  - High voltage can be applied to the substrate (> 100 V).
  - Shorter drift distances: higher radiation tolerance (10^{15} 1 MeV n_{eq}/cm^2).
  - Larger sensor capacitance (~100 fF): larger noise. Lower speed and higher power electronics.
  - Prone to cross talk from digital electronics into sensor.
- Small fill-factor structure.
  - Sensing diode and electronics are separated by p-substrate.
  - Higher resistivity substrates available (up to 8 kΩ·cm).
  - Only low voltage can be applied to the substrate (< 10 V).
  - Longer drift distances: lower radiation tolerance (10^{14} 1 MeV n_{eq}/cm^2).
  - Small sensor capacitance (~5 fF): lower noise. Higher speed and lower power electronics.



Large fill-factor CMOS structure



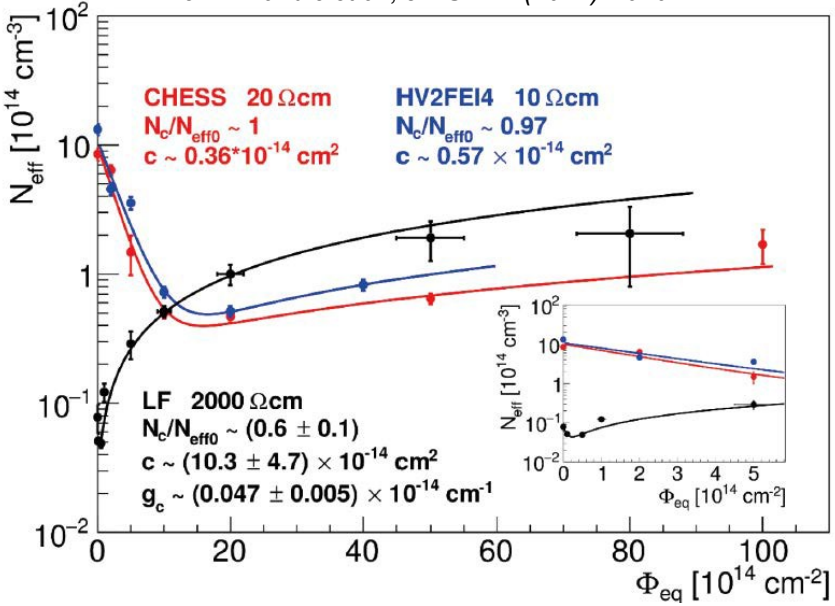
Small fill-factor CMOS structure

Ref: N. Wermes, 32nd RD50 Workshop.

Depleted CMOS sensors challenges

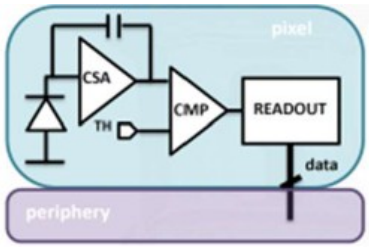
- Higher radiation tolerance (10^{15} 1 MeV n_{eq}/cm^2): > $7 \cdot 10^{17}$ 1 MeV n_{eq}/cm^2.
  - Increase the allowed substrate biasing ($W \propto \sqrt{\rho \cdot V_{bias}}$)
  - Access to high resistivity substrates: need of considering doping concentration dependence with irradiation.
  - Backside processing (back bias contact and thinning): improved charge collection efficiency.
  - Multiple nested wells for increasing isolation between low voltage CMOS electronics and bias applied to the substrate.
  - Use of CMOS technologies with smaller feature sizes.
- Timing resolution (10 ns): < 5 ns.
  - Sources of time uncertainty are the charge collection time, delay in readout electronics and time-walk.
  - Reduction of charge collection time constrained by sensor structure, geometry and bias.
  - Delay improvement in readout electronics limited by power consumption.
  - Design methods to improve time-walk in readout electronics (two-threshold method, ramp method, etc.).
- Fast readout (particle rate 100 MHz/cm^2): > 1000 MHz/cm^2.
  - Full readout architecture to be implemented on-chip to cope with detector demands in HEP (fast readout, time stamping, triggering, etc.).
  - Different readout architectures being tested: column drain architecture, parallel pixel to buffer or asynchronous.
  - Optimization of integration level, cross-talk and speed.

Ref: I. Mandic et al., JINST 12 (2017) P02021.

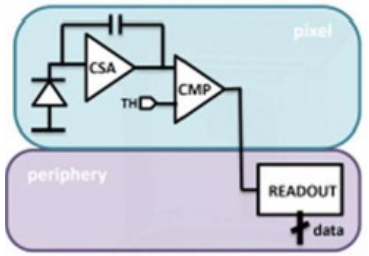


Effective doping concentration vs. neutron fluence.

Ref: T. Hemperek, FEE 2018



In-pixel readout: column drain architecture



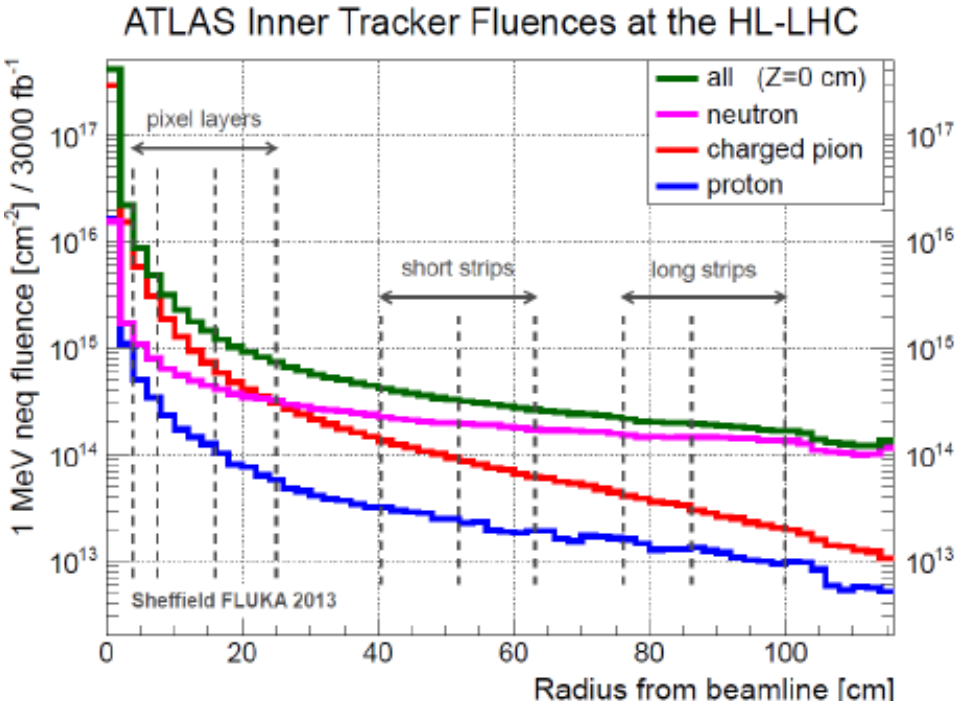
Periphery readout: parallel pixel to buffer architecture

Commercial CMOS foundries

- There is a number of commercial foundries available.
- Valuable experience with some of these vendors from several depleted CMOS developments carried out.
- Large fill-factor structures produced in LFoundry, ams and TSI.
  - H35Demo (ams 350 nm). ATLAS experiment.
  - LF-Monopix01 (LFoundry 150 nm). ATLAS experiment.
  - ATLASPix01 (ams 180 nm). ATLAS experiment.
  - MuPix7 (TSI 180 nm). Mu3e experiment.
- Small fill-factor structures produced in TowerJazz.
  - EPBC01 (ESPROS 150 nm).
  - Investigator (TowerJazz 180 nm epitaxial). ATLAS experiment.
  - MALTA (TowerJazz 180 nm epitaxial). ATLAS experiment.
  - TJ-Monopix (TowerJazz 180 nm epitaxial). ATLAS experiment.
- HV-SOI technology available in XFAB (180 nm).
- Current technologies offer feature sizes ≥ 130 nm: room for radiation tolerance and logic density improvement with smaller sizes (≤ 65 nm).

CERN RD50 collaboration CMOS activities

- International collaboration with more than 300 members.
- Aimed at developing and characterizing radiation-hard semiconductor devices for high luminosity colliders.
- Semiconductor sensors will be exposed to hadron fluences not withstood by current LHC detectors.
  - HL-LHC: > 10^{16} 1 MeV n_{eq}/cm^2.
  - FCC: > $7 \cdot 10^{17}$ 1 MeV n_{eq}/cm^2.
- R&D carried out in new structures.
  - n in p sensors.
  - 3D sensors.
  - LGAD.
  - Depleted CMOS.
- Depleted CMOS devices is a RD50 priority.
  - Extensive depletion depth measurements (E-TCT) and charge collection measurements.
  - Before and after irradiation.
  - Thined and unthinned devices.
- New effort to develop different matrices of pixels and test structures in depleted CMOS processes (coordinated by E. Vilella/U. Liverpool).
- For more information about CERN RD50 activities: see specific talk of M. Mandurrino on Tuesday.

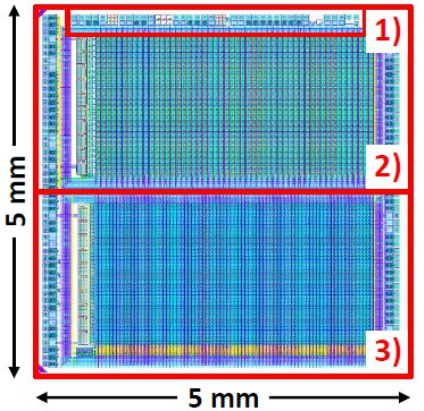


Ref: I. Dawson, P. S. Miyagawa, ATL-UPGRADEPUB-2014-003, 2014

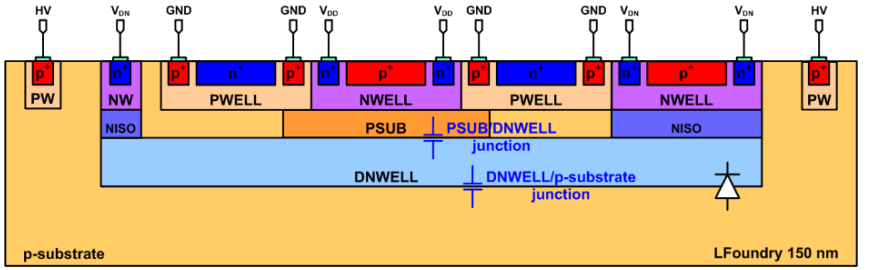
CERN RD50 depleted CMOS development project (I)

- Participating institutions: U. Liverpool, IFAE, U. Barcelona, U. Seville,IFCA, CPPM, JSI, FBK, HEPHY, U. Lancaster and IFIC. U. Bonn and IRFU collaborate with support.
- RD50-MPW1: test technology aspects of the process and novel designs.
  - 150 nm HV-CMOS LFoundry MPW. HR wafers (500 and 1.9 kΩ·cm). 280 µm detector thickness.
  - Design effort by IFAE and U. Liverpool.
  - Test structures for TCT/E-TCT.
  - 26x52 depleted CMOS pixels matrix with 16-bit embedded counter.
  - 40x78 depleted CMOS pixels (50 µm x 50 µm) matrix with FE-I3 style embedded readout (column drain).
  - Large collection electrode structure.
  - DAQ development and device characterization activities still ongoing.
  - Sensors are fully functional but measured leakage current in test structures higher than expected.
- RD50-MPW2: minimize leakage current and improve speed..
  - 150 nm HV-CMOS LFoundry MPW. Different resistivities wafers (10, 100, 1.9k and 3 kΩ·cm). 280 µm detector thickness.
  - Design effort by IFAE, CPPM, FBK and U. Liverpool.
  - Test structures for TCT/E-TCT.
  - 8x8 matrix depleted CMOS pixels (60 µm x 60 µm) with analogue embedded readout.
  - Single Event Upset (SEU) tolerant memory array.

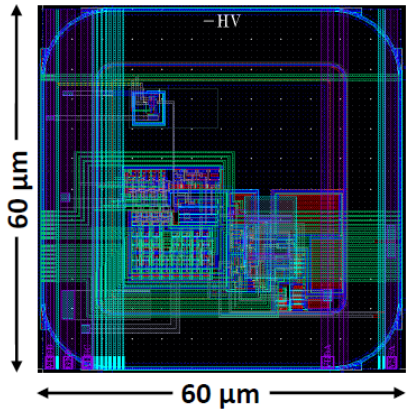
Ref: E. Vilella et al., 33rd RD50 Workshop



RD50-MPW1 sensor floor plan



RD50-MPW1 sensor cross-section

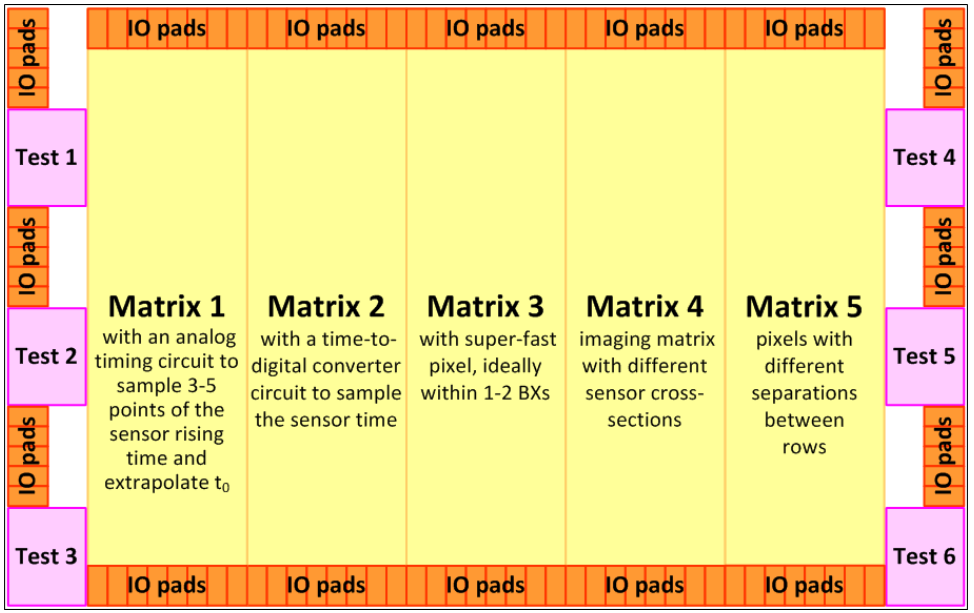


RD50-MPW2 pixel floor plan

CERN RD50 depleted CMOS development project (II)

- RD50-ENGRUN1 goals.
  - Improvement of current time resolution with dedicated readout circuits.
  - Implementation of new sensor cross-sections.
  - Assessment of pre-stitching options to increase device area (beyond reticle size limitation).
  - Increase of radiation tolerance by sensor design and backside processing.
- Technology.
  - 150 nm HV-CMOS from LFoundry.
  - Large area submission.
- Design effort.
  - FBK-Trento.
  - IFAE-Barcelona.
  - U. Barcelona.
  - U Liverpool (also project coordination).
  - U. Sevilla.
  - IFIC-Valencia.
  - U. Bonn/CPPM/IRFU collaborate with support.
- DAQ development and TCAD simulations carried out in parallel with device design.

Ref: E. Vilella et al., VERTEX 2018 Workshop



RD50-ENGRUN1 sensor floor plan block diagram

Conclusion

- Depleted CMOS sensor technology is very promising for future silicon tracking detectors due to several factors.
  - Lower costs and easier detector assembly.
  - Fast fabrication turn-around of CMOS commercial technology.
  - Material budget saving due to reduced thickness.
- However, some challenges must still be faced to cope with future tracking detectors requirements.
  - Radiation hardness.
  - Timing resolution.
  - Fast data readout.
- This sensor technology is a priority for the CERN RD50 collaboration, which has been involved in the radiation tolerance study of depleted CMOS sensors.
- Within CERN RD50 a project to develop depleted CMOS sensors has been started.
  - RD50-MPW1 designed and fabricated. Currently under test.
  - RD50-MPW2 designed and submitted with new design approaches to minimize leakage current and increase electronics speed.
  - Larger RD50-ENGRUN1 being designed with several matrices of pixels with the main goal of improving the timing resolution.

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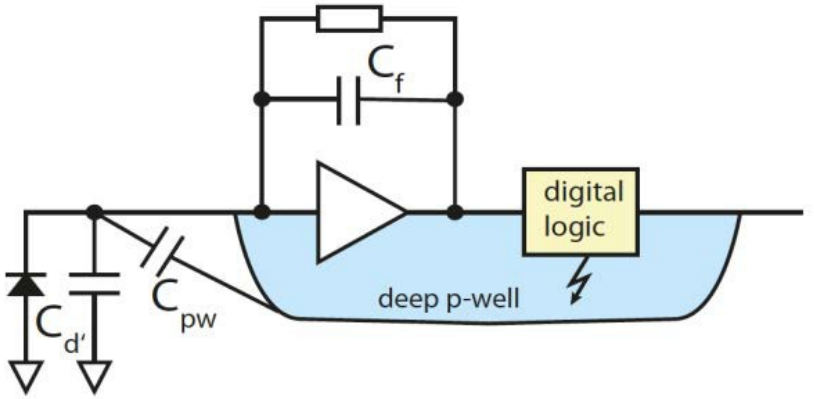
Back-up slides

Additional inter-well capacitance

- Total detector capacitance: $C_d = C_{d'} + C_{pw}$
- Noise and timing proportional to detector capacitance (C_d).
- There is a need to increase the amplificer transconductance (g_m) to compensate for noise and timing: power increased (g_m proportional to transistor drain current).
- Large fill factor more prone to cross talk into sensor if digital logic is implemented inside the collecting node.
  - Digital noise can couple to the sensor through the parasitic capacitance between the deep p-well (digital logic ground) and the deep n-well (input).
  - Circuit design must consider this fact.

Ref: N. Wermes, 32nd RD50 Workshop.



Typical silicon pixel readout scheme with digital logic in the collecting node.

$$ENC^2_{thermal} \propto \frac{4}{3}\frac{kT}{g_m}\frac{\mathbf{C_d^2}}{\tau}$$

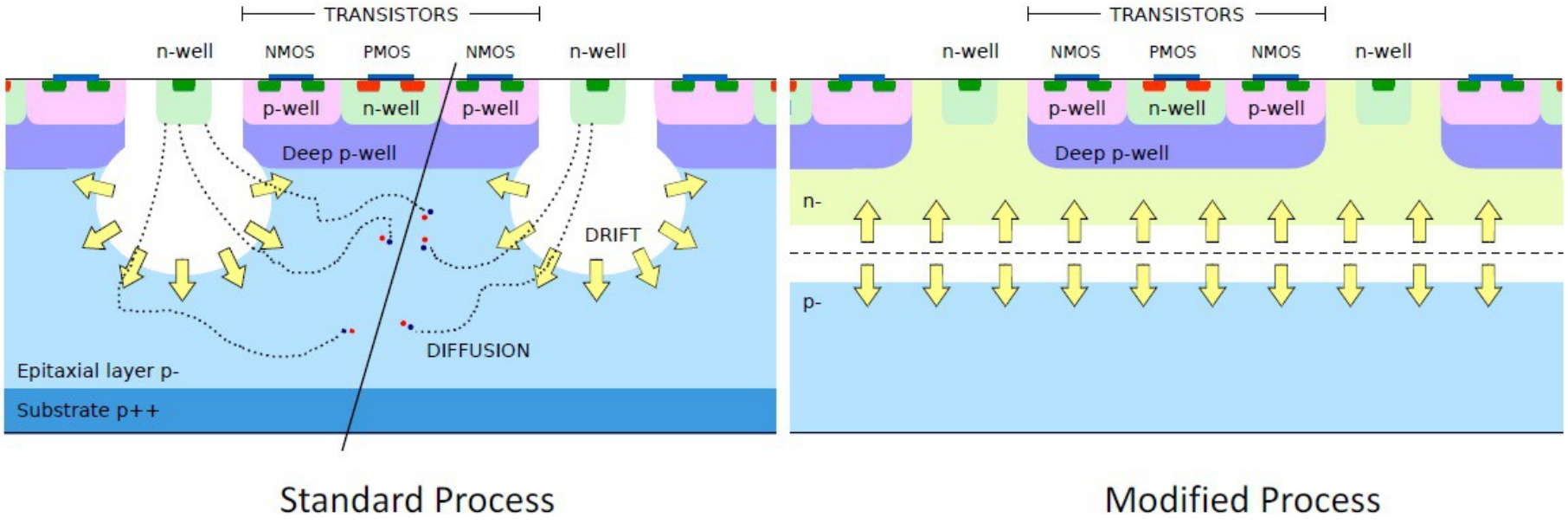
Charge amplifier thermal equivalent noise

$$\tau_{CSA} \propto \frac{1}{g_m}\frac{\mathbf{C_d}}{C_f}$$

Charge amplifier rise time

TowerJazz 180 nm modified process

- A uniform n-implant is added in the epi layer: ensures full lateral depletion.

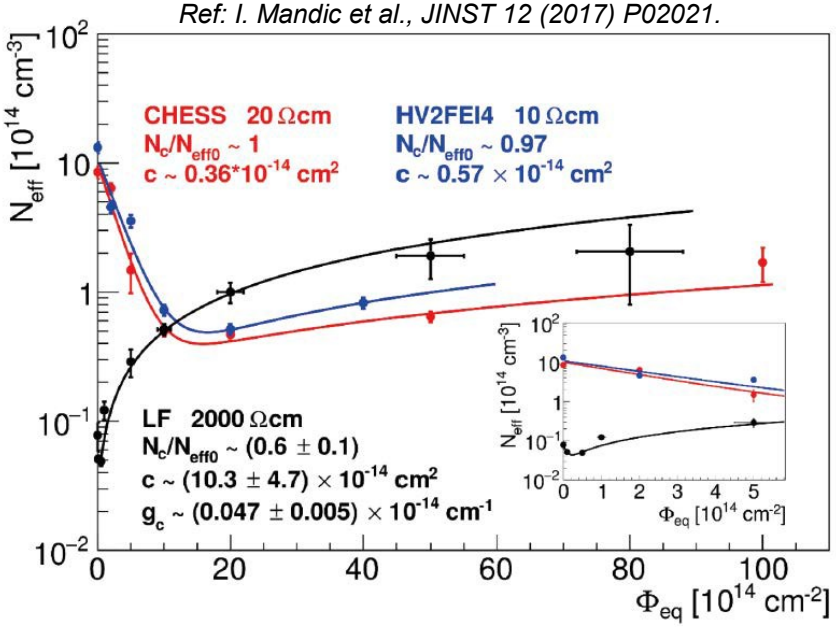


Ref: A. Sharma, Vertex 2018

Effective doping concentration vs. fluence

- Effective doping concentration dependence on neutron fluence for three different CMOS detectors with p-substrates of different resistivities.
- Acceptor removal effect visible for lower substrate resistivities: increase of the depletion depth after irradiation (up to $2 \cdot 10^{15}$ 1 MeV n_{eq}/cm^2).
- Due to the low initial dopant concentration for higher resistivities: creation of stable acceptors dominates and the depletion depth decreases after irradiation.

Ref: I. Mandic et al., JINST 12 (2017) P02021.



Effective doping concentration vs. neutron fluence.

Depletion depth

$$W = w_0 + \sqrt{\frac{2\varepsilon_0\varepsilon_r}{e_0 N_{eff}} V_{bias}}$$

Effective doping concentration vs. neutron fluence

$$N_{eff} = N_{eff0} - N_c \cdot \left(1 - \exp(-c \cdot \Phi_{eq})\right) + g \cdot \Phi_{eq}$$

Acceptor removal

Radiation introduced deep acceptors