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Overview of CMOS sensors for future tracking detectors

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ABSTRACT

The depleted CMOS sensors are emerging as one of the main candidate technologies for future tracking detectors in high luminosity colliders. Its capability of integrating the sensing diode into the CMOS wafer hosting the front-end electronics allows for reduced noise and higher signal sensitivity. They are suitable for high radiation environments due to the possibility of applying high depletion voltage and the availability of relatively high resistivity substrates. The use of a CMOS commercial fabrication process leads to their cost reduction and allows faster construction of large area detectors. A general perspective of the state of the art of these devices will be given in this contribution as well as a summary of the main developments carried out with regard to these devices in the framework of the CERN RD50 collaboration.

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1 Introduction

Current large pixel detectors in High Energy Physics, such as the ones which will be part of the ATLAS Tracker Detector [1] or the CMS Tracker Detector [2] upgrades for the High Luminosity Large Hadron Collider (HL-LHC), mostly follow a hybrid approach. In a hybrid pixel detector the sensor and the readout electronics are independent devices connected by means of bump-bonding, as it can be seen in Figure 1. This fact allows for independent development of the sensor and readout electronics technologies to cope with high radiation environments and particle rates. However, bump-bonding is a complex and expensive assembly process with a limited output rate. Moreover, the overall material budget of several layers restricts the accuracy of the particle trajectory measurement in hybrid pixel detectors.

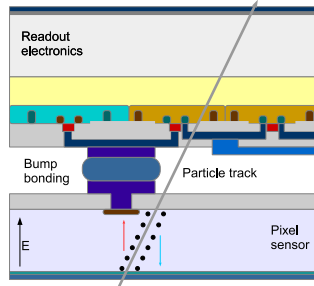


Figure 1: Diagram of a hybrid pixel detector.

A promising alternative to the current hybrid approach is the so-called depleted monolithic active pixel sensors (MAPS). These kind of sensors integrate the sensing diode and the readout electronics in the same CMOS wafer, as it is shown in Figure 2. The charge is mainly collected in the depleted area created by applying reverse bias. The pixel electronics is placed inside an isolated n-well. This sensor technology offers the possibility of noise reduction and higher signal sensitivity. An important advantage is that its commercial CMOS fabrication process and its integration leads to an easier production, a large cost reduction and a faster fabrication. Furthermore, this technology can save material budget due to its reduced thickness.

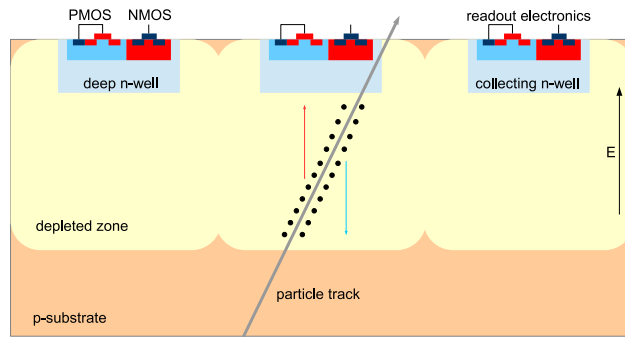


Figure 2: Diagram of a depleted CMOS MAPS sensor.

Unfortunately, although the depleted CMOS sensor technology offers several clear advantages, there are several aspects of this technology which still have to be improved, as the radiation tolerance, the timing resolution and a fast readout capability to cope with high particle rates.

2 Large versus small fill-factor structures

The two main n-on-p CMOS sensor design concepts according to their collection electrode size, known as the fill factor, are depicted in Figures 3(a-b). In the large-fill factor structure (Figure 3a), the sensing diode is

made up of the p-substrate and the deep n-well while the electronics are placed inside the charge collection well. High resistivity substrates, up to $3 \text{ k}\Omega\cdot\text{cm}$ [3], are currently available for this structure. Since a high bias voltage can be applied to the device, there will be on average shorter drift distances and, as a consequence, a higher radiation tolerance capability. However, the sensor capacitance is larger in this structure, up to hundreds of fF [4] depending on the pixel size, so the noise will be also larger. The electronics will also have lower speed and will need more power to counterbalance this fact. Furthermore, this structure is more prone to cross talk from digital electronics into sensor.

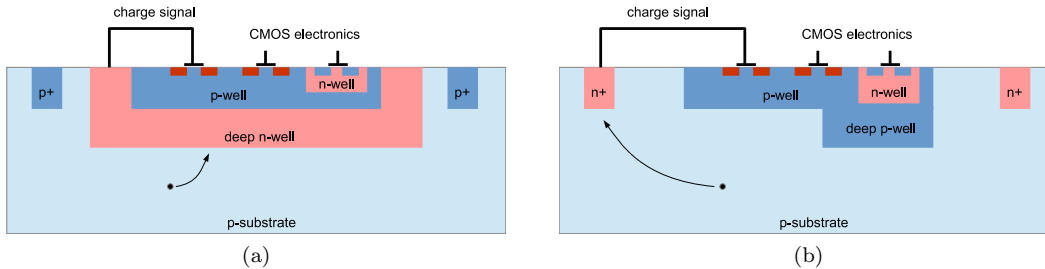


Figure 3: Large fill-factor structure (a) and small fill-factor structure (b).

On the other hand, the small fill-factor structure (Figure 3b) is characterized by the fact that the sensor diode and the readout electronics are separated by the p-substrate. Higher resistivity substrates, up to $8 \text{ k}\Omega\cdot\text{cm}$ [3], can be used with this structure but only low bias voltage can be applied to the substrate. Therefore, longer drift distances are required on average and consequently, this structure tends to a lower radiation tolerance. Nevertheless, the sensor capacitance is very small, a few fF [4], having a lower noise compared to the large fill-factor structure. Thus, the electronics implemented in the small fill-factor structure can be faster and less power-consuming.

3 Challenges of the depleted CMOS sensors

As it has been aforementioned, there are three important challenges that the depleted CMOS sensor technology has to face: the radiation hardness, the timing resolution and a fast data readout.

3.1 Radiation tolerance

The first challenge is to increase the radiation hardness of this sensor technology, currently about $10^{15} \text{ 1 MeV } n_{eq}/\text{cm}^2$ [5], to reach the equivalent fluences required, for instance, for the Future Circular Collider, which will be larger than $7 \cdot 10^{17} \text{ 1 MeV } n_{eq}/\text{cm}^2$ [6]. In order to meet this requirement, the CMOS sensors will need to increase the allowed substrate biasing as well as to access to high resistivity substrates, since the depleted depth is proportional to the product of these two parameters. In that sense, the effective doping concentration of the p-substrate varies with irradiation in a different way for high and low resistivities [7], there is an increase of the depletion depth after irradiation for lower resistivities (up to equivalent fluences of about $2 \cdot 10^{15} \text{ 1 MeV } n_{eq}/\text{cm}^2$) whereas the depletion depth decreases after irradiation for higher resistivities. This fact has to be considered in the sensor design process. The backside processing of CMOS sensors is also an important factor to increase their radiation tolerance since having back bias contact or thinned devices will improve their charge collection efficiency. Another relevant aspect for a better radiation hardness would be the possibility of implementing multiple nested wells in order to increase the isolation between the CMOS electronics and the substrate so that higher bias voltages could be applied to the devices. Finally, the use of CMOS technologies with smaller feature sizes would also increase the radiation tolerance of the depleted CMOS sensors.

3.2 Timing resolution

The second challenge is to improve the timing resolution of this kind of devices from the current one, lower than 10 ns [8][9], to a even better resolution, lower than 5 ns. There are different sources of time uncertainty such as the charge collection time, the delay in the readout electronics and the time-walk in the comparator. The reduction of the charge collection time is constrained by the sensor geometry and bias whereas the electronics delay improvement is limited by the readout electronics power consumption. Therefore, there is more room for improvement in the reduction of the time-walk by applying new design methods for the discrimination of the analogue signals like using a time-walk compensated comparator [5], the two-threshold method or the ramp method [8].

3.3 Fast readout

The third challenge for this technology is to be able to get a fast readout of the data to deal with high particle rates in future high luminosity colliders. For instance, a particle rate higher than 1000 MHz/cm² is foreseen in the inner pixels layers of the ATLAS tracker detector in the HL-LHC [1]. One of the advantages of the depleted CMOS sensor technology is the implementation of the full readout architecture in the same device to cope with detector demands, not only in terms of particle rates but also for triggering or time stamping. There are different readout architectures such as the column drain architecture implemented in the LF-Monopix device [10] or the parallel pixel to buffer architecture implemented in the ATLASPix M2 device [11]. In the former architecture, the address and time stamp is read out in each pixel and then the data are moved selectively to the chip periphery whereas in the latter architecture the binary data of each pixel are moved immediately to the device periphery and processed there upon a trigger arrival. Another type of asynchronous readout architecture has been also implemented in the TJ-Malta device [12]. These readout architectures are being tested to optimize the integration, cross-talk and speed of the device.

4 Commercial CMOS foundries

There is a number of commercial foundries available for the fabrication of depleted CMOS sensors. The CMOS sensors community has already a valuable experience with some of these vendors from several developments carried out. Large fill-factor structures have been produced in LFoundry Srl, ams AG and TSI Semiconductors Corp, in the framework of the ATLAS upgrade and the Mu3e experiments, like the H35Demo device [13], implemented in the ams 350 nm process, the LF-Monopix device [10], implemented in the LFoundry 150 nm process, or the MuPix7 and MuPix8 devices [8], implemented in the ams and TSI 180 nm processes, to mention a few ones. Regarding the small fill factor structures, some devices of this type have been also produced in TowerJazz Ltd. following the TJ 180 nm process as the TJ-Monopix device [10] or the TJ-Malta device [12]. A special type of CMOS technology, the High Voltage Silicon On Insulator, is also available at X-FAB Semiconductor Foundries AG, several devices have been implemented in the XFAB 180 nm process, like the XTB01 device [14]. Finally, it must be emphasized that the current technologies available for CMOS sensors offer feature sizes larger than 130 nm, therefore the radiation tolerance and logic density of these devices can be further improved with smaller sizes in the future.

5 Summary of CMOS activities in the framework of the CERN RD50 collaboration

The CERN RD50 is an international collaboration with more than 300 members aimed at developing and characterizing radiation-hard semiconductor devices for high luminosity colliders. As it has been mentioned, semiconductor sensors will be exposed in the HL-LHC or FCC to hadron fluences not withstood by current LHC sensors. Among other research interests, the collaboration has a research line in new detector structures, such as n-on-p sensors, 3D sensors, low gain avalanche photodiodes and depleted CMOS sensors. The latter are a priority for RD50. In fact, several depletion depth and charge collection measurements have been

already carried out with different CMOS devices [15][16]. Moreover, there is a new effort within the RD50 collaboration to develop different matrices of pixels and test structures in depleted CMOS processes.

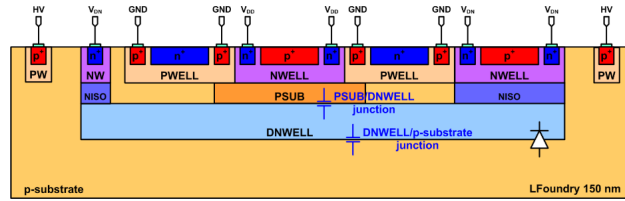


Figure 4: Diagram of the RD50-MPW1 depleted CMOS sensor cross-section.

A small depleted CMOS sensor prototype, the RD50-MPW1 [17] device of 5 mm by 5 mm, has been already developed using the 150 nm LFoundry process in two different resistivities, $500 \Omega \cdot \text{cm}$ and $1.9 \text{ k}\Omega \cdot \text{cm}$. The device has a total thickness of 280 m. The main goals of this design are to test the technology used and verify the validity of novel designs. Figure 4 shows a diagram of the RD50-MPW1 device cross-section, where it can be seen that the device has a large fill factor structure. The RD50-MPW1 device has test structures for Edge-Transient Current Technique (E-TCT) measurements and two independent CMOS pixels matrices. One is a photon counting matrix with 28 by 52 pixels with embedded readout electronics, charge amplifier and discriminator, and a 16-bit counter. The other matrix has 40 by 78 pixels, with a size of $50 \mu\text{m}$ by $50 \mu\text{m}$, with embedded readout electronics following a column drain readout architecture similar to the FEI3 readout chip [18]. The DAQ development and the device characterization activities related to the RD50-MPW1 device are still ongoing. The sensors are fully functional but the measured leakage current is higher than expected.

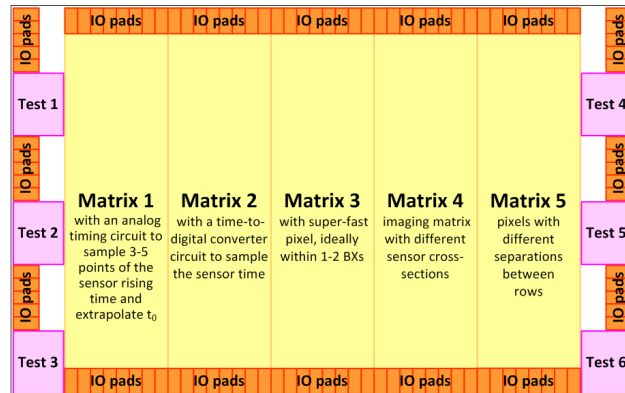


Figure 5: Diagram of the RD50-ENGRUN1 device main blocks.

Finally, the so-called RD50-ENGRUN1 device, a large area demonstrator, is also being designed within the CERN RD50 collaboration using the 150 nm process of Lfoundry. A diagram of the main blocks of the RD50-ENGRUN1 device can be seen in Figure 5. This device has several independent depleted CMOS pixel matrices and test structures. The pixel matrices have different purposes and the main goals pursued in this design are the improvement of the current time resolution with dedicated readout circuits, the implementation of new sensor cross-sections, the assesment of pre-stitching options to increase the device size beyond the reticle size limitation and the increase of radiation tolerance by sensor design and backside processing. The design effort is being carried out by several of the institutions already involved in the RD50 CMOS project. The DAQ development and TCAD simulations are also running in parallel with the device design.

6 Conclusions

It has been pointed out that the depleted CMOS sensor technology is very promising for future silicon tracking detectors due to its lower cost, easier and faster detector assembly, faster fabrication turn-around and larger material budget saving. However, some challenges must still be faced to cope with future tracking detectors requirements in terms of radiation hardness, timing resolution and fast data readout. This sensor technology is a priority for the CERN RD50 collaboration, which has been involved in the radiation tolerance study of depleted CMOS sensors. Within the CERN RD50 collaboration, a project to develop depleted CMOS sensors has been started. The RD50-MPW1 chip has been designed and fabricated and is currently under test. The RD50-MPW2 has been designed and already submitted aimed at reducing the leakage current and improving the readout electronics speed. A larger RRD50-ENGRUN1 device is being designed with several matrices of pixels with the main goal of improving the timing resolution.

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