

Introduction

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Meet the team

TCAD simulations

- Matt Franks Uni. Liverpool/FBK
- Patrick Freeman Uni. Birmingham
- Laura Gonella Uni. Birmingham

ASIC design

- Oscar Alonso + 1 student Uni. Barcelona
- Raimon Casanova IFAE
- Nicola Massari FBK
- Fernando Muñoz Uni. Seville
- Rogelio Palomo Uni. Seville
- Eva Vilella Uni. Liverpool
- Chenfan Zhang Uni. Liverpool/FBK
- New designers Uni. Bonn, CPPM and IRFU

DAQ development

- Thomas Bergauer HEPHY
- Christian Irmler HEPHY
- Ricardo Marco-Hernández IFIC
- Salvador Martí IFIC
- Helmut Steininger HEPHY

RD50-ENGRUN1

Aims

- Improve the time resolution and speed of HV-CMOS sensors (matrices 1-3)
- Study different sensor cross-sections (matrix 4)
- Study options to increase the detector area beyond the reticule size limitation (matrix 5)
- Increase the radiation tolerance (all)

Prototyping

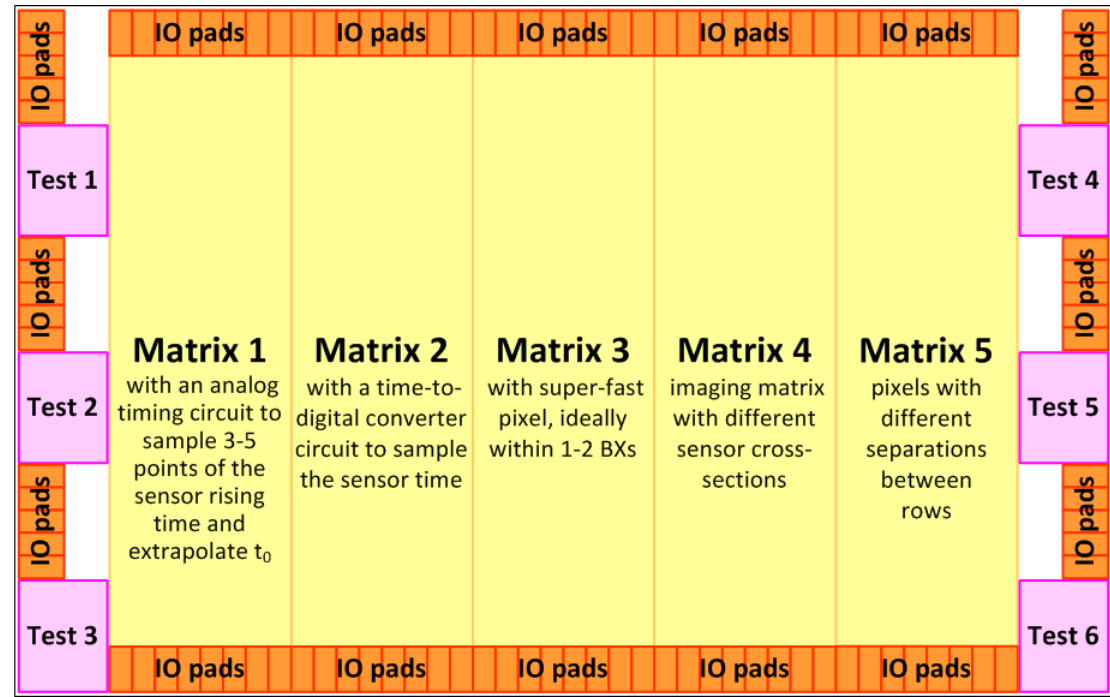
- 150 nm HV-CMOS from LFoundry
- Large area submission (MLM)
- Maximum design area is ~ 2.5 cm x 0.9 cm
- Backside biasing at the foundry

Costs

- ~ 90 k€ (need to double check with foundry)
- Half of the costs come from the RD50 common funds

Timeline

- Ideally, to be submitted towards the end of 2018 or beginning of 2019, but there's no real deadline



Test structure 1

Test structure 2

Test structure 3

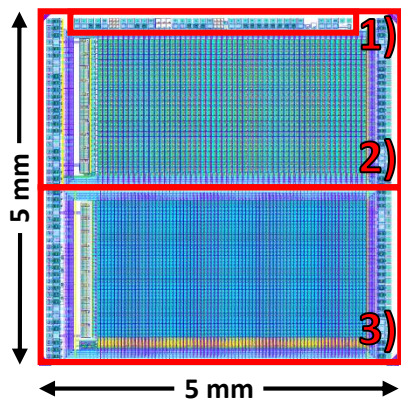
Test structure 4

Test structure 5

Test structure 6

Simple CMOS capacitors to study oxide thickness
 10 x 10 matrix of very small pixels with passive RO
 10 x 10 matrix of very small pixels with 3T-like RO
 Small matrix of pixels for TCT, e-TCT and TPA-TCT
 Single pixels for sensor capacitance measurements
 ...

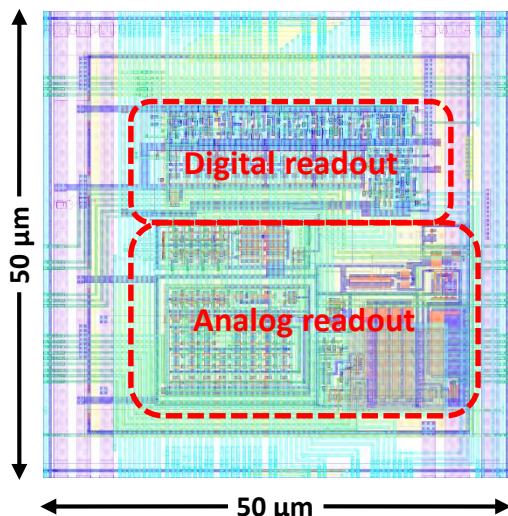
RD50-MPW1



Technical details:

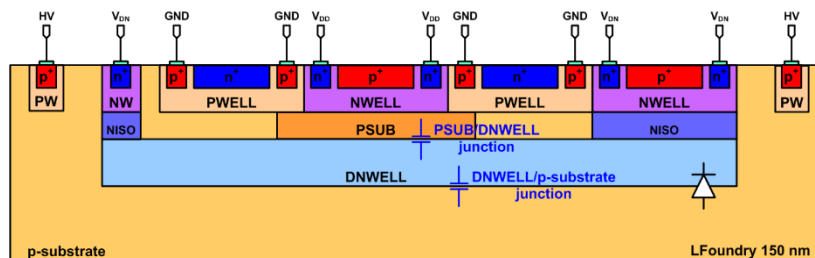
- MPW in 150 nm HV-CMOS from LFoundry
- Manufactured on wafers with different substrate resistivities:
 - 500 Ω·cm (40 samples) and 1.9k Ω·cm (80 samples)
- Fab-in in November 2017, fab-out in April 2018 (measurements just started)
- Contents:
 - 1) Test structures for TCT/e-TCT
 - 2) Matrix of 26 x 52 HV-MAPS pixels with 16-bits counter
 - 3) Matrix of 40 x 78 HV-MAPS pixels with FE-I3 style readout
 - pixel area is 50 μm x 50 μm
 - analog and digital readout electronics are embedded inside the pixel area

FE-I3 pixel:



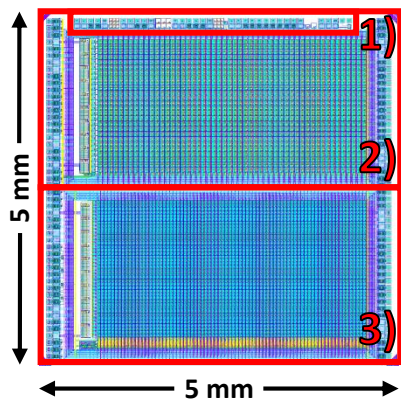
- **Analog readout** → biasing circuit, amplifier, low-pass/high-pass filters and comparator with 4-bit DAC to compensate for offset variations
- **Digital readout** → two 8-bit DRAMs that continuously store leading/trailing edge time stamps (ToT = TE – LE) + one 8-bit ROM to store pixel address (FE-I3 style)

Sensor cross-section



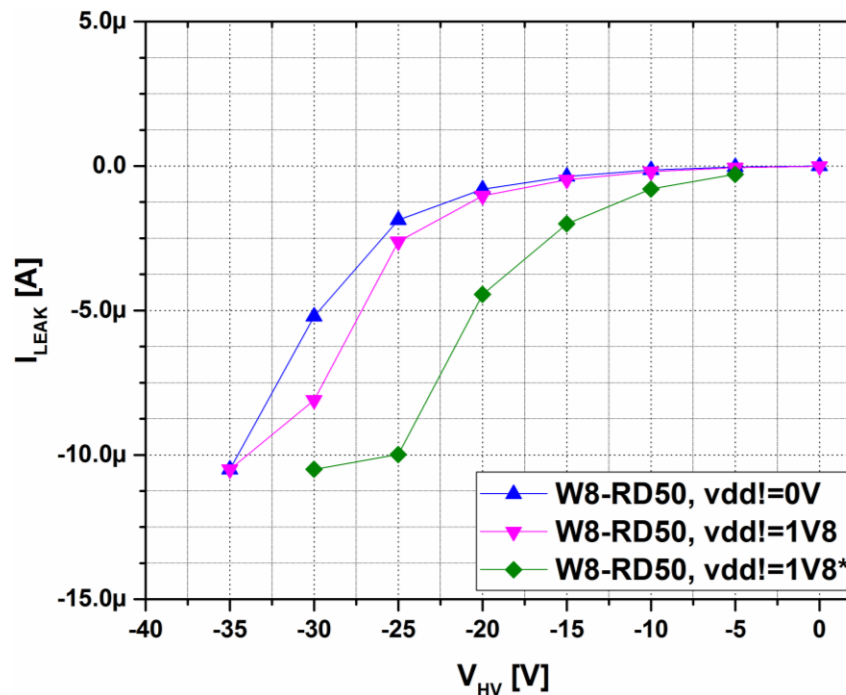
- 50 μm x 50 μm
- $C_{PIX} \approx 200$ fF
- PDK V1.2.0
(proper verification)

RD50-MPW1



Preliminary measurements:

- Despite the very careful design, measurements show an unexpected I-V with too low breakdown voltage and too large leakage current.
- This effect is under investigation at the moment.



- To test the electronic functionality of the matrices, there is a dedicated DAQ in place at IFAE and a new generic DAQ is being developed by HEPHY/IFIC.
- Preliminary measurements show what seems to be an issue with the substrate (being investigated at the moment at IFAE).