Design of matrix 1 for RD50-ENGRUN1 - Analog sampling

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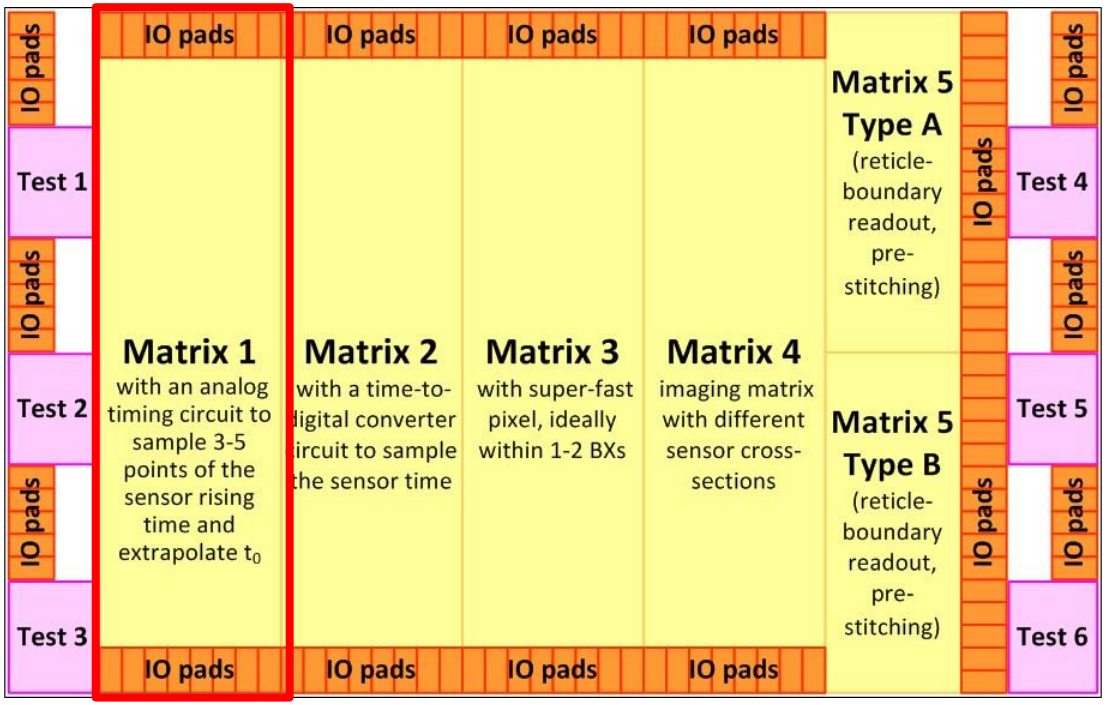
ENGRUN1: Design



Test structure 1	Simple CMOS capacitors to study oxide thickness
Test structure 2	10 x 10 matrix of very small pixels with passive readout
Test structure 3	10 x 10 matrix of very small pixels with 3T-like readout
Test structure 4	Small matrix of pixels for TCT, e-TCT and TPA-TCT measurements
Test structure 5	Single pixels for sensor capacitance measurements
Test structure 6	…

CERN/RD50 collaboration:

- International project to develop radiation hard semiconductor devices for very high luminosity colliders

Target of this submission:

- Improve the timing resolution of HV-CMOS sensors with different solutions implemented at the readout circuit level
- Study new sensor cross-sections
- Study pre-stitching options (increase the device area beyond the reticle size limitation)

Technology:

- 150 nm HV-CMOS from LFoundry

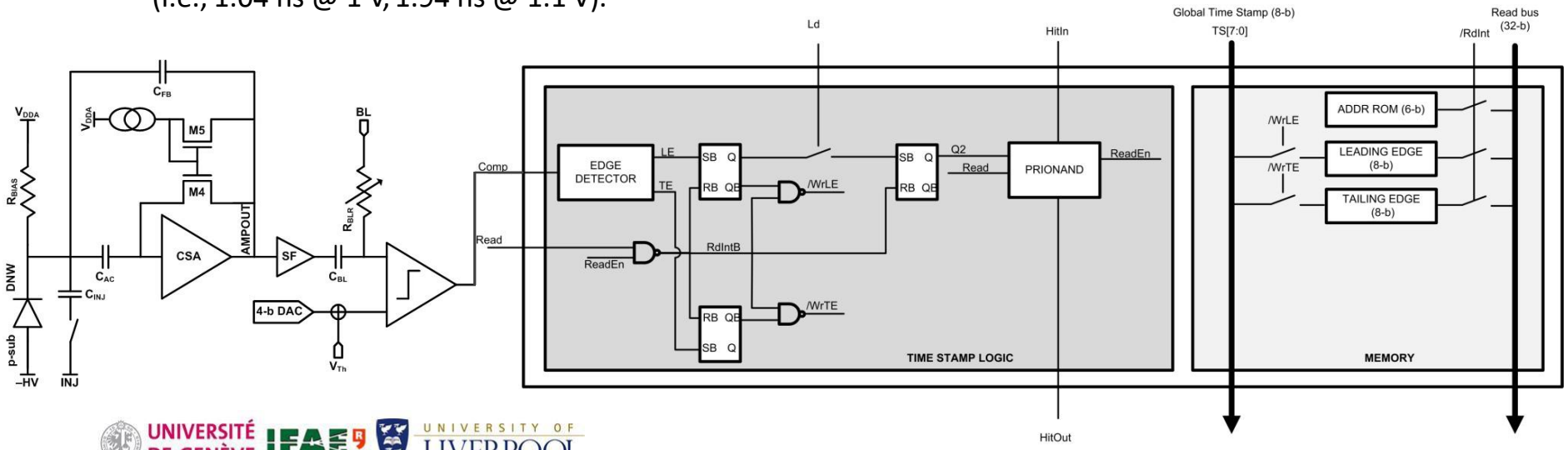
Design effort:

- IFAE (R. Casanova)
- Uni. Barcelona (O. Alonso)
- Uni. Liverpool (S. Powell, E. Vilella and C. Zhang)
- FBK (N. Massari and M. Perenzoni)

ENGRUN1: Design

The pixel in Matrix 1 includes:

- **Sensor** → 50 µm x 50 µm (~200 fF parasitic capacitance)
- **Analog readout electronics** → CSA, shaper, filter and comparator.
- **Digital readout electronics** → Electronics that sense the leading edge of the comparator and store the corresponding time-stamp in an 8-bit memory. The electronics also store the pixel address in another 8-bit memory (this info is not needed for the analysis presented in these slides).
- **Sampling electronics** → Chain of delay elements and sample & holds to store 5 analog voltages. The sample & holds sample the output voltage of the shaper. The delay elements put the sample & hold in hold mode when there is an event in the pixel. We can tune the delay with an external voltage (i.e., 1.04 ns @ 1 V, 1.94 ns @ 1.1 V).



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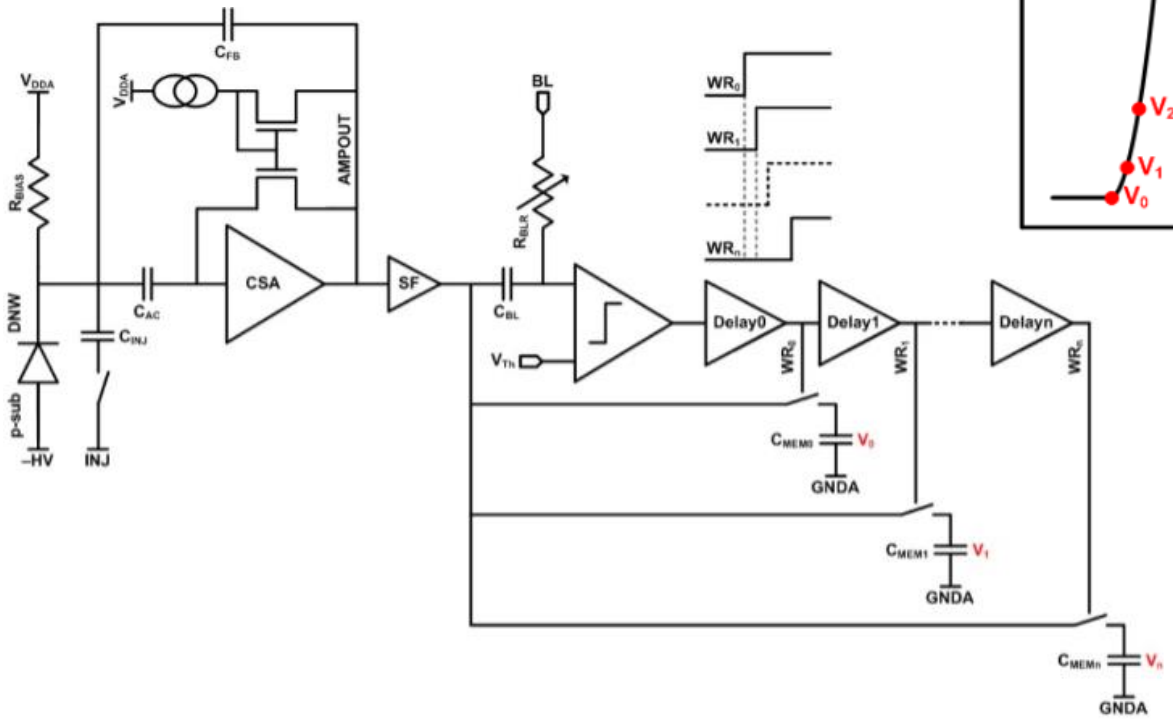
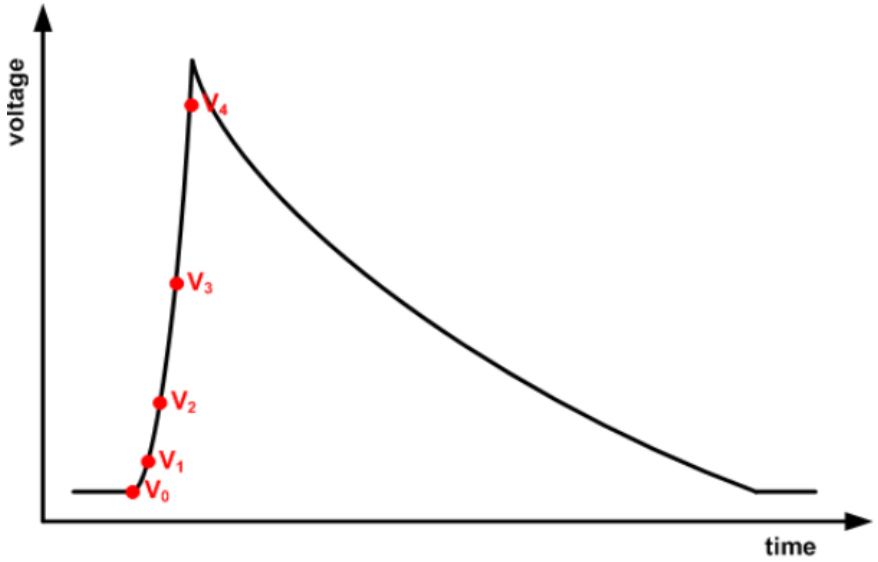
Simplified schematic and functionality





The main idea is to store up to 5 analog voltages.

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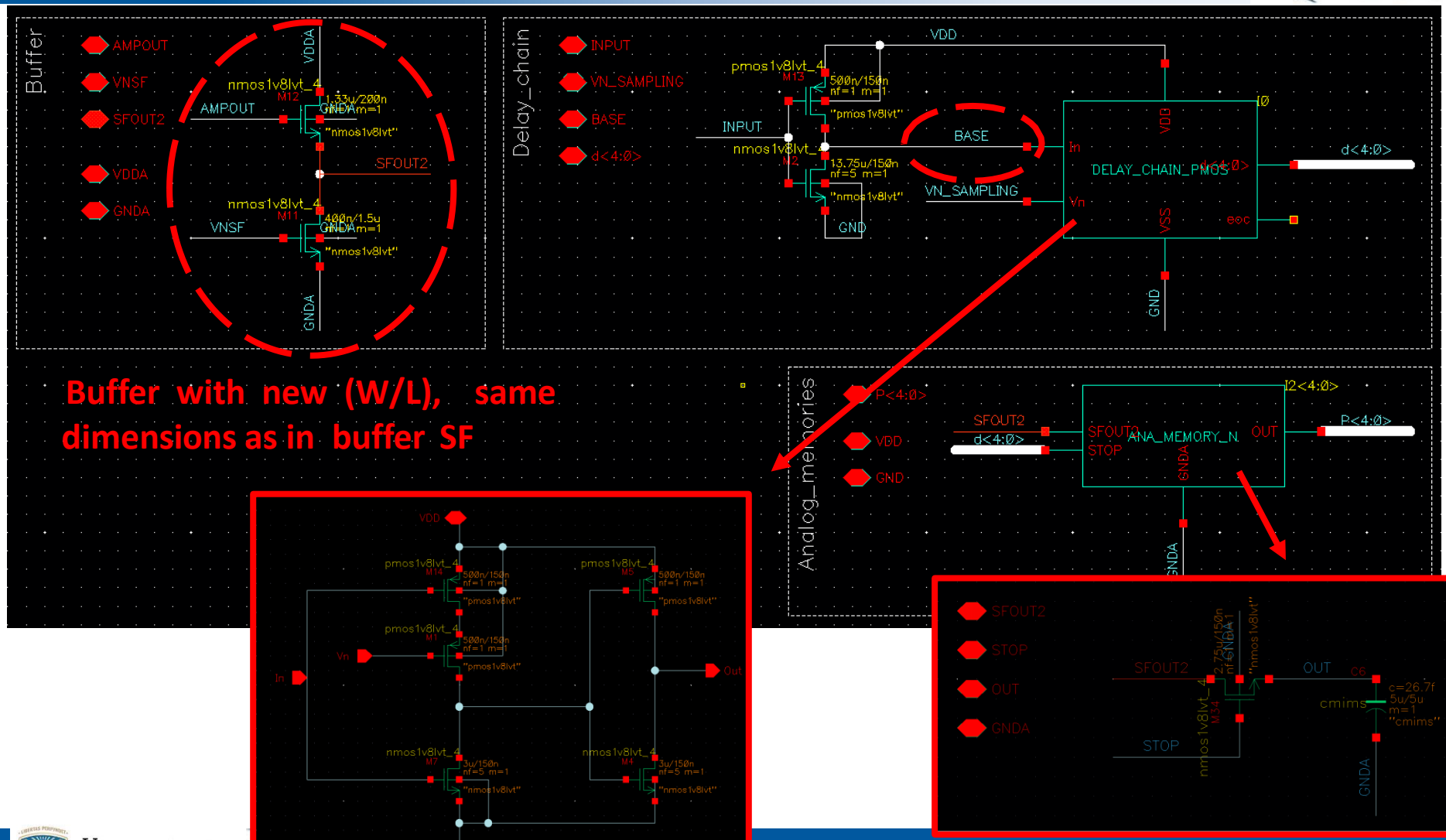

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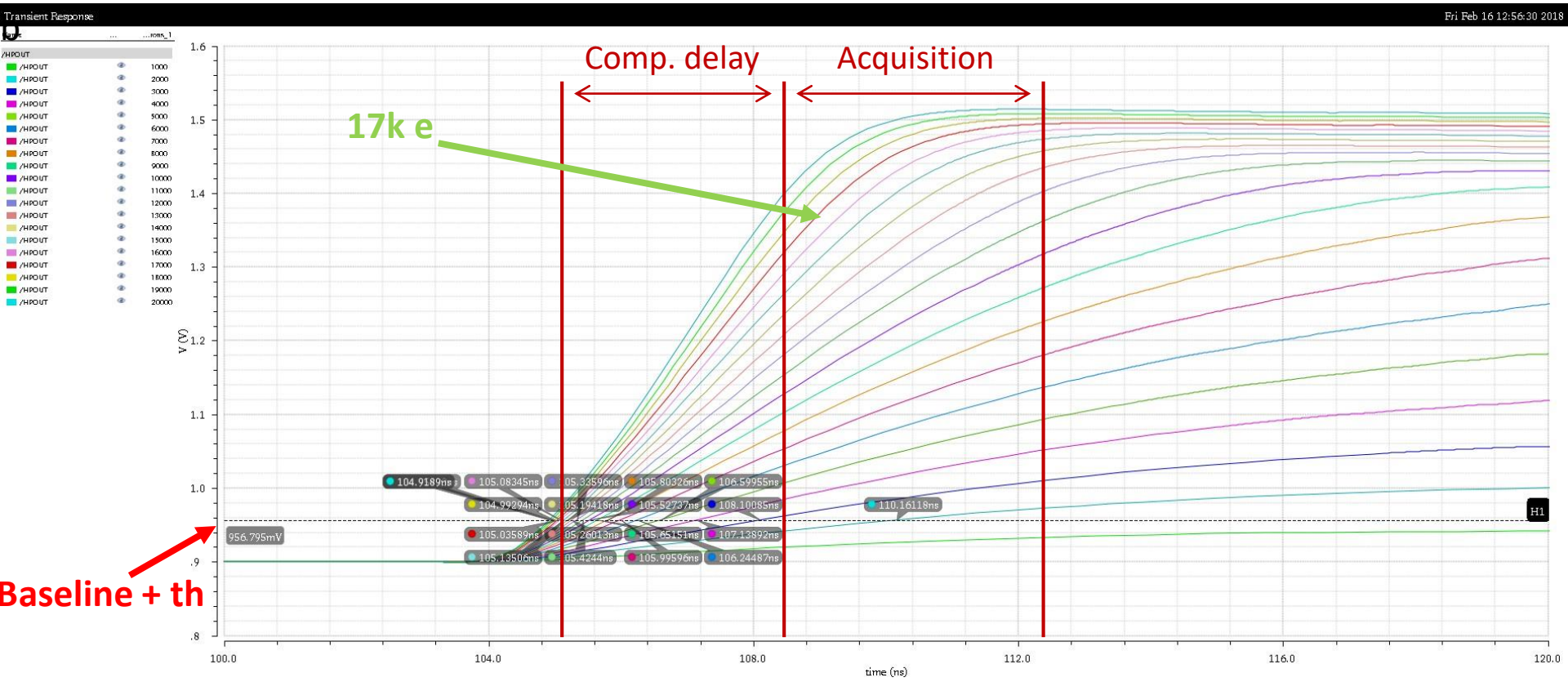

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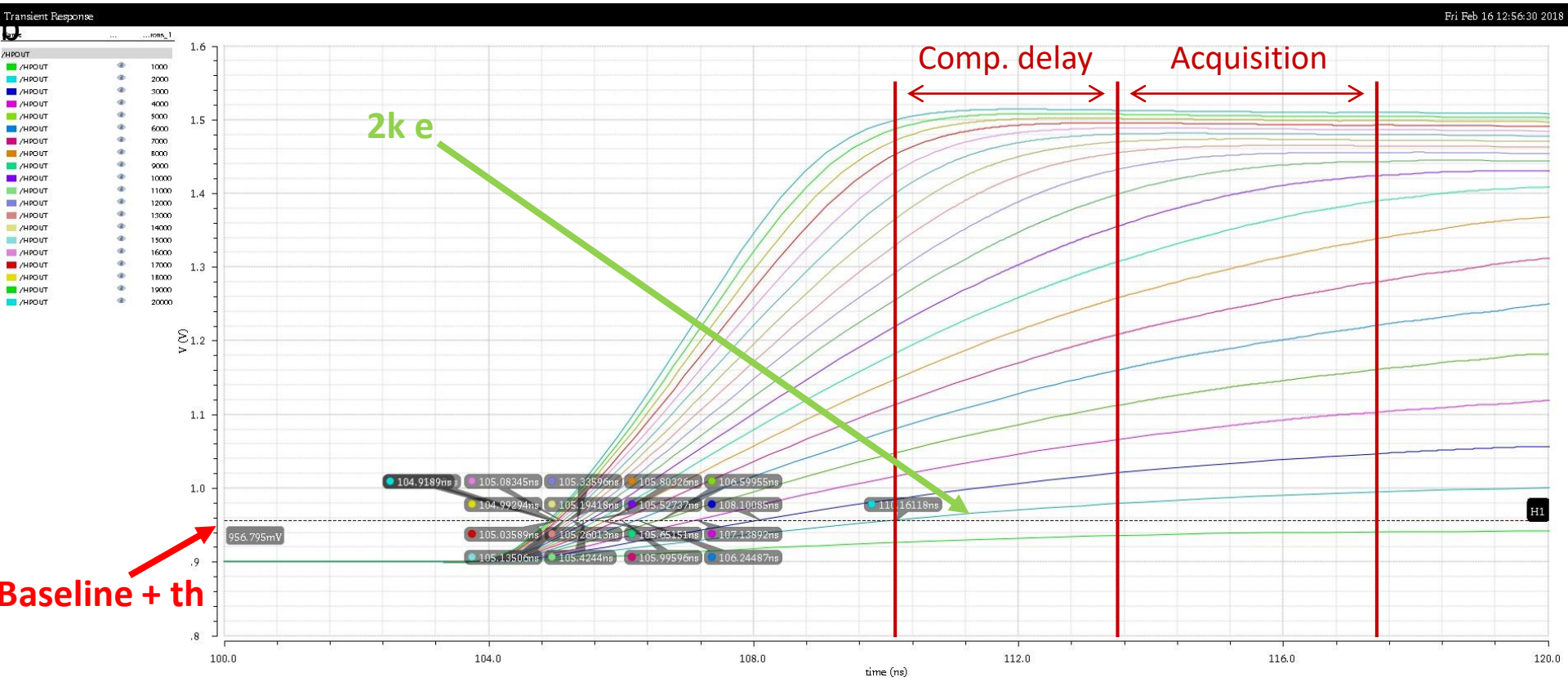

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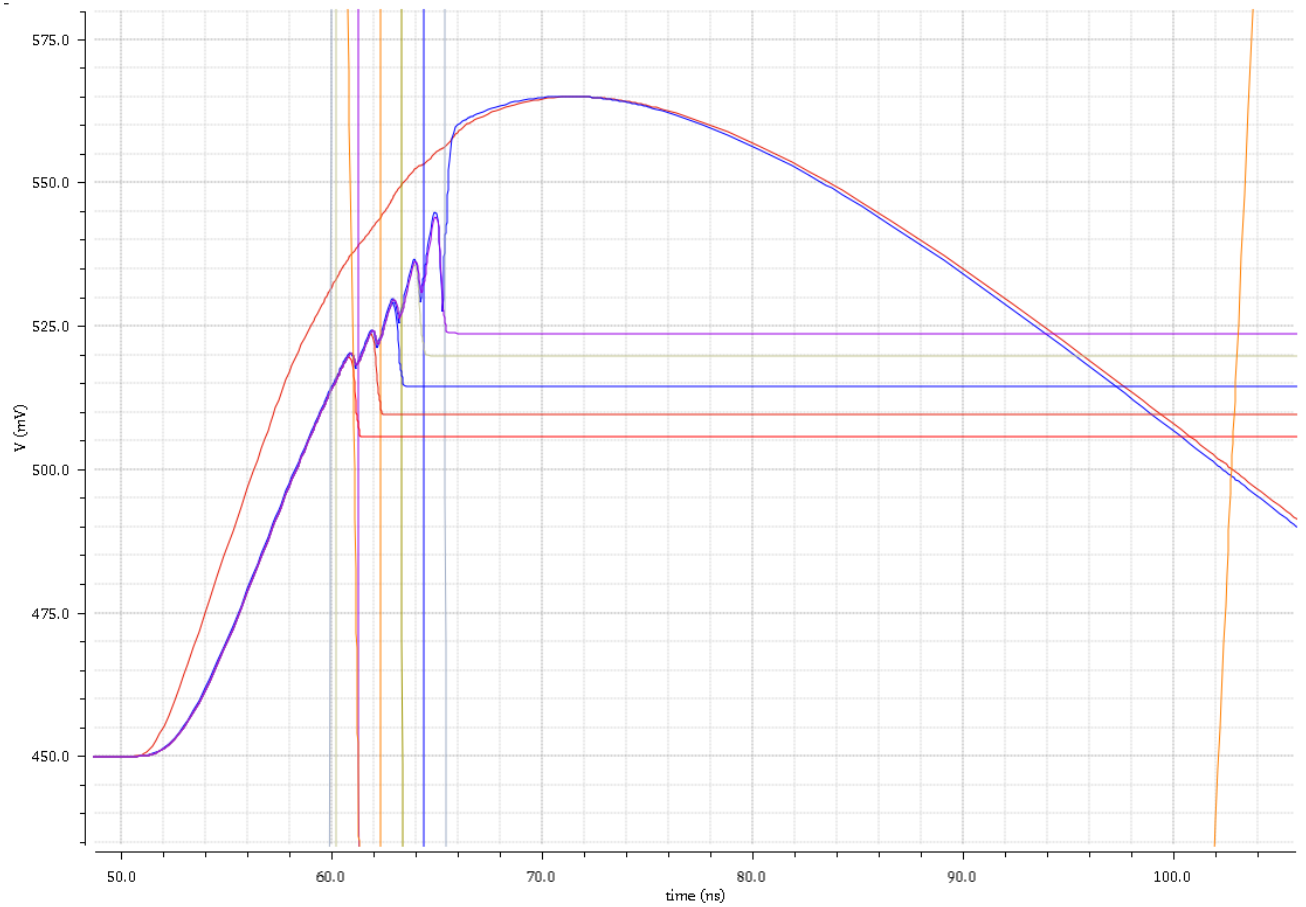

Input charge 2k - Power consumption = 25.72 µW

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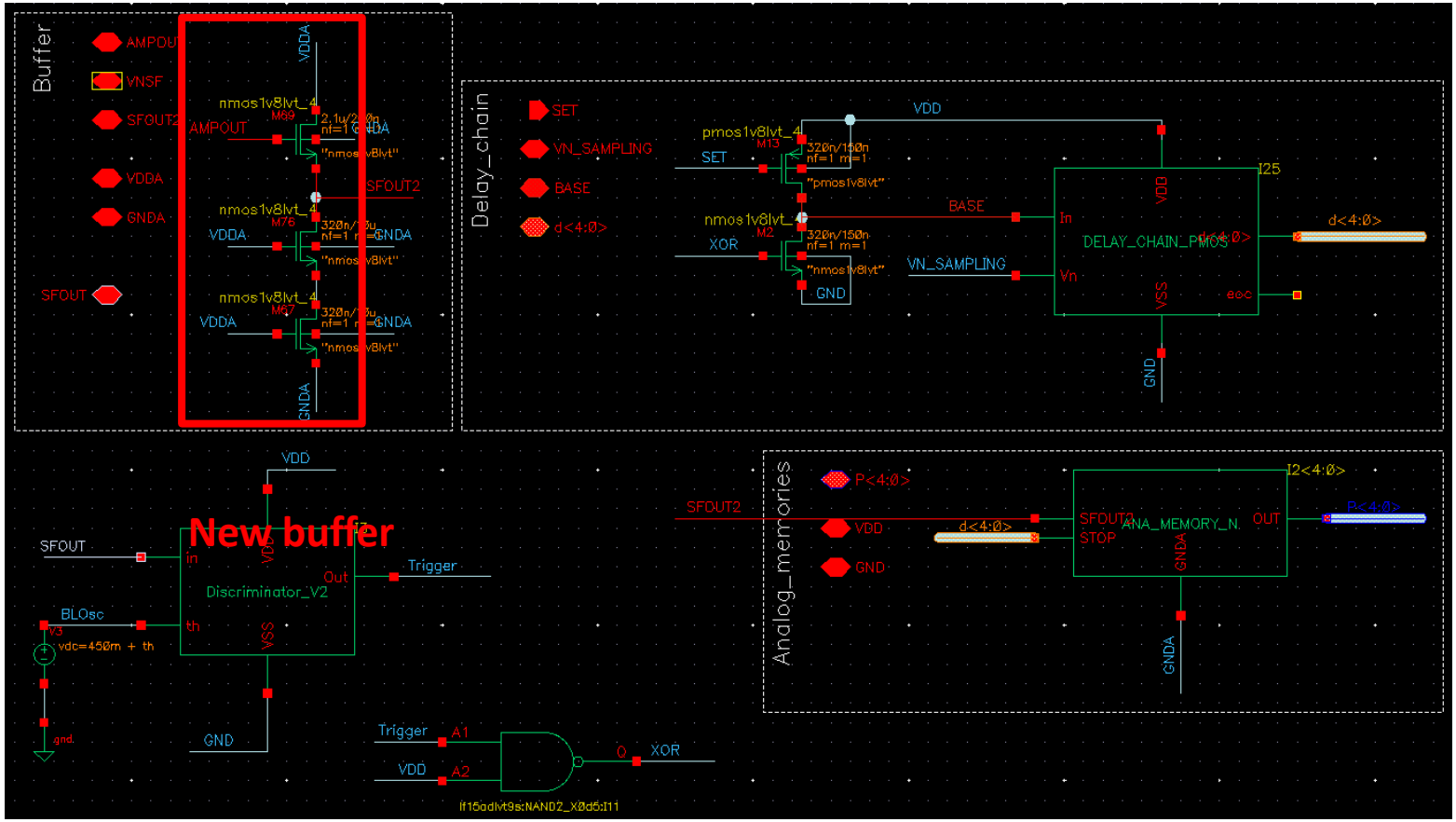

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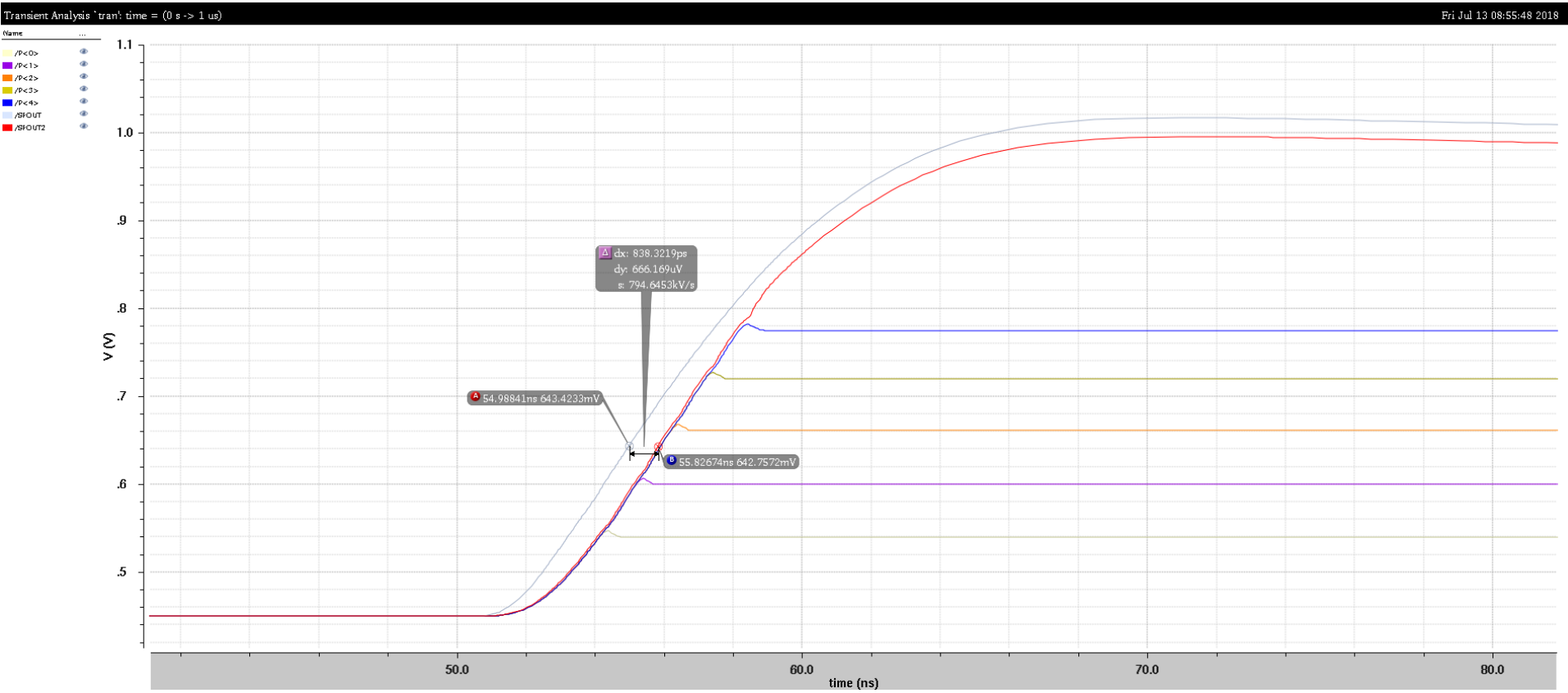
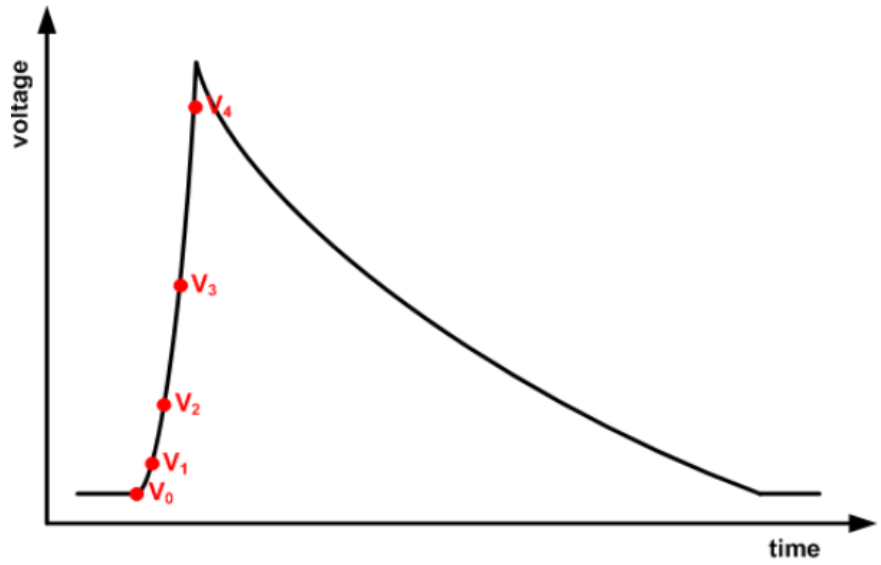


Input charge 9k - Power consumption ~ 28 µW

Conclusion

- The quality of the method depends on:
  - Value of VN → How do we choose the appropriate value of VN?
  - Comparator time response
  - It also depends on the amount of input electrons
    - Better time resolution at larger amounts of input electrons
  - It also depends on the proximity of the real event time to the Cadence/chip time-stamp
    - An event happening at 1.022 µs gives a better time resolution than an event happening at 2.385 µs, as 1.022 µs is closer to the time-stamp (1 µs = 20 * 50 ns) than 2.385 µs (2.35 µs = 47 * 50 ns).
  - Time-stamp period
- Power consumption of 28 uW per pixel with the possibility to reduce it to 22 uW
- Other solutions under study

Conclusion



- Instead of defining time axis we define the voltage axis

  => We are designing a TDC