Design of RD50-ENGRUN1 Matrix 3 – Fast pixels

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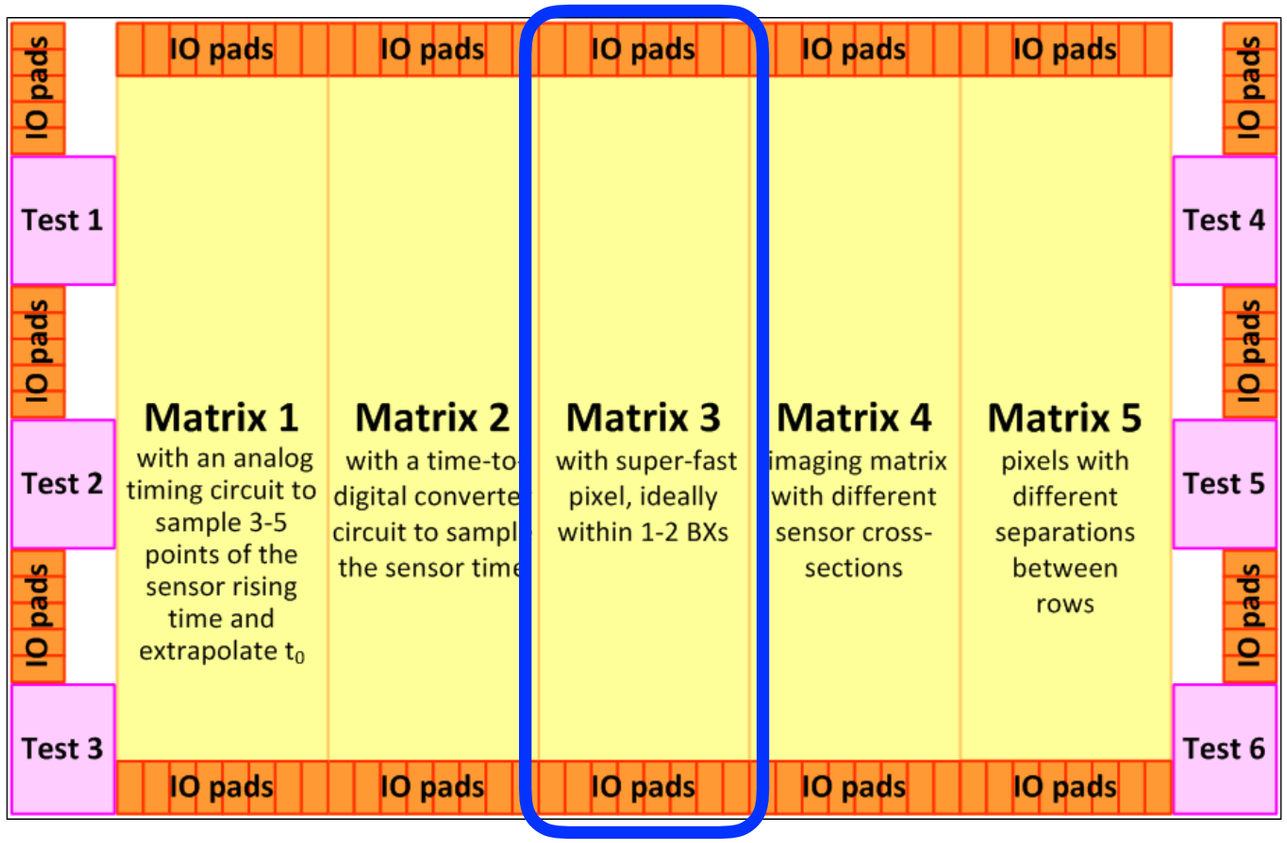
RD50-ENGRUN1 Matrix 3



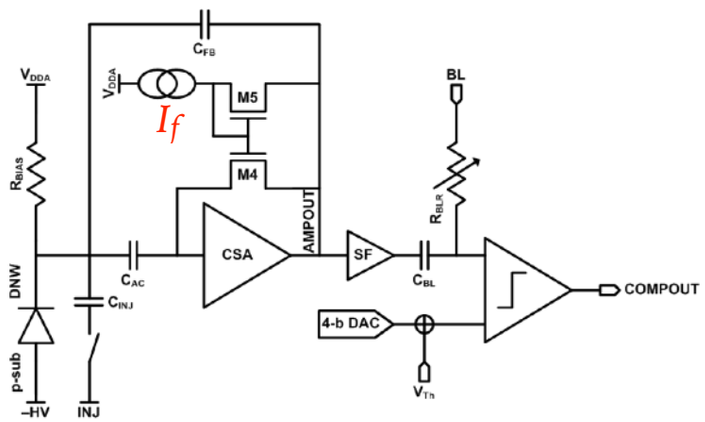
floor-plan of RD50-ENGRUN1

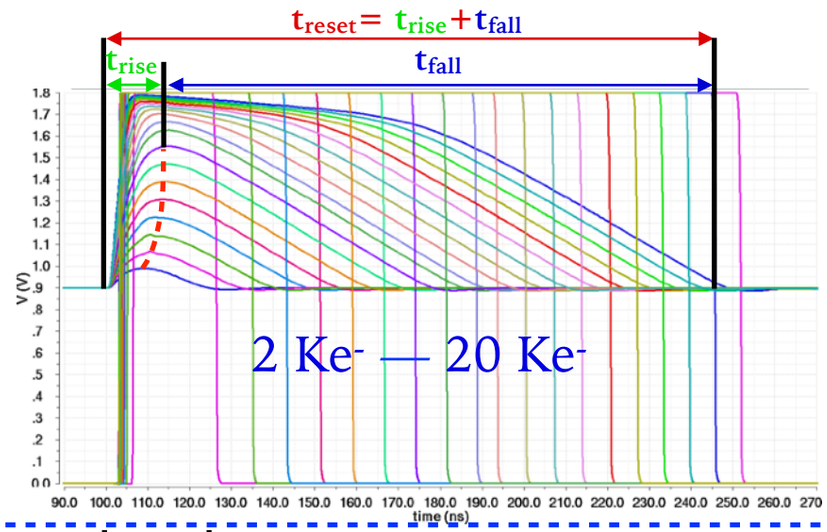
- To cope with the increasing hit rate in the future high energy physics experiments, it is necessary to have pixel detectors with high-speed front-ends.
- I have designed 6 fast pixel types with different flavours and they will be implemented in Matrix 3 of RD50-ENGRUN1 including:
  - 2 different reset strategies.
  - 3 types of pre-amplifiers.

Pixel flavours

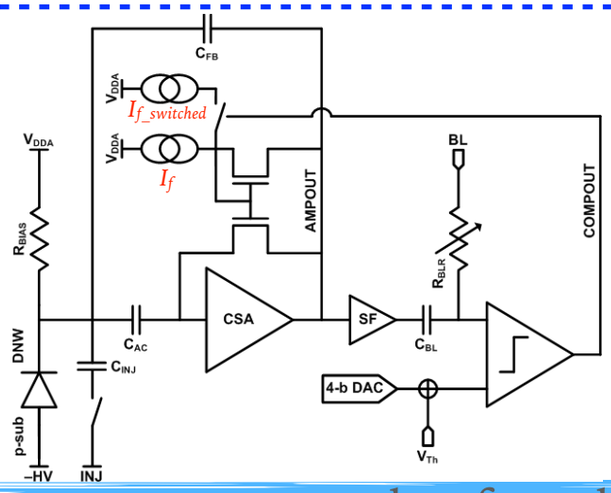
- The **Linear reset** strategy discharges the CSA continuously with a constant current $I_f(\sim nA)$ and can use ToT to measure the amount of input charges. The total processing time $\mathbf{t_{reset}}$ can be less than 40 ns for a 4000 e- signal.
- The **Switched reset** strategy discharges the CSA with a switched current $I_{f\_switched}(\sim \mu A)$ that flows only when a particle hit is detected and the comparator's output is high. The discharge process can be finished within 7 ns and $\mathbf{t_{reset}}$ stays below 25 ns no matter how many input charges. The power consumption does not increase a lot, because the large current $I_{f\_switched}$ flows only during $\mathbf{t_{reset}}$. Compared to the linear reset strategy, this one can deal with large signals much faster, but the ToT measurement is not possible.
- All **3 types of pre-amplifiers** use the single folded cascode structure. One uses a pMOS as the input device, the other two use nMOS. Different speed and noise performances are observed from them.

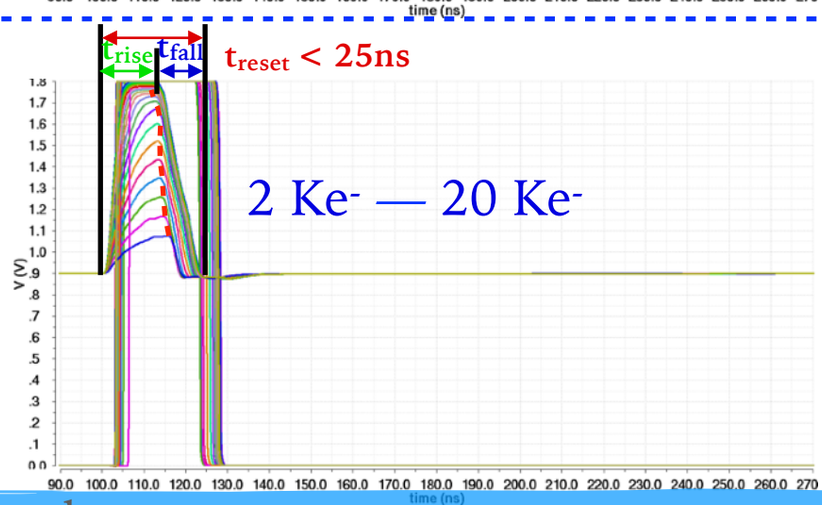
Linear reset





Switched reset





Simulation results & Comparison with State of the Art

input=4000 e⁻	Linear_ pMOS	Linear_ nMOS1	Linear_ nMOS2	Switched_ pMOS	Switched_ nMOS1	Switched_ nMOS2	ATLASpix (measurement)	LF-MonoPix (measurement)	CACTUS (simulation)
Technology	LFoundry 150 *nm* HV-CMOS						AMS_180	LF_150	LF_150
Pixel size (μm^2)	50 × 50						40 × 130	50 × 250	1000×1000
$C_{det.}$	150 *fF*	150 *fF*	150 *fF*	165 *fF*	165 *fF*	165 *fF*		~ 400 *fF*	1.5 *pF*
gain	255 mV	230 mV	345 mV	355 mV	325 mV	360 mV		76 mV	65 mV
ENC	94 e⁻	36 e⁻	42 e⁻	93 e⁻	30 e⁻	64 e⁻		~ 200 e⁻	~ 290 e⁻
t_{ries} (0-100%)	8.5 ns	8.4 ns	10.2 ns	14 ns	12.3 ns	9.9 ns		25 ns	2 ns
t_{fall} (100%-0)	31.9 ns	31.3 ns	28.6 ns	4.5 ns	5.8 ns	6.5 ns		105 ns	8 ns
t_{reset}	40.4 ns	39.7 ns	38.8 ns	18.5 ns	18.1 ns	16.4 ns		130 ns	10 ns
Power cons. per pixel	22 μW (880 mW/cm²)	22.5 μW (900 mW/cm²)	23.5 μW (940 mW/cm²)	22.5 μW (900 mW/cm²)	23 μW (920 mW/cm²)	24 μW (960 mW/cm²)	7.8 μW (150 mW/cm²)	36 μW (288 mW/cm²)	1450 μW (145 mW/cm²)

- The results of my pixels are based on simulations that use schematic models without digital readout circuits as they are currently under design.

Outlook

- Layout design of Linear_pMOS and Switched_pMOS front-ends have finished.
- Both analog front-end and digital readout electronics will be integrated into the 50 $\mu m \times 50\ \mu m$ sensing area.
- I am currently designing the digital readout circuits based on the **column-drain** architecture as it is simple to implement and has been used before.