Depleted Monolithic Pixel Sensors in LF150
RD50 meeting

Tomasz Hemperek
on behalf of Bonn Group

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- **IC Design:**

  Hans Krüger , Tomasz Hemperek, Tianyang Wang ,

  Konstantinos Moustakas , Piotr Rymaszewski (~2FTE for CMOS)

Mostly CMOS Testing :

Toko Hirono, Ivan Caicedo-Sierra , Christian Bespin

Other:

RD53, DEPFET about 10 people

Bonn Group

Mayor ASIC chip developments

- FE-I3, FE-I4, FE-65p2, **RD53A**
- DHP (Belle II PXD)
- MPEC, CIX (counting)
- PixCap (capacitance measurements)
- CMOS pixel prototypes in several technologies (LF, Toshiba, ESPROS, TJ, XFAB)

Pixel modules developemnt:

- bump bonding (since 1997)
- modules for ATLAS pixels, IBL, upgrade
- DEPFET modules for Belle II
- TSVs

Test system development

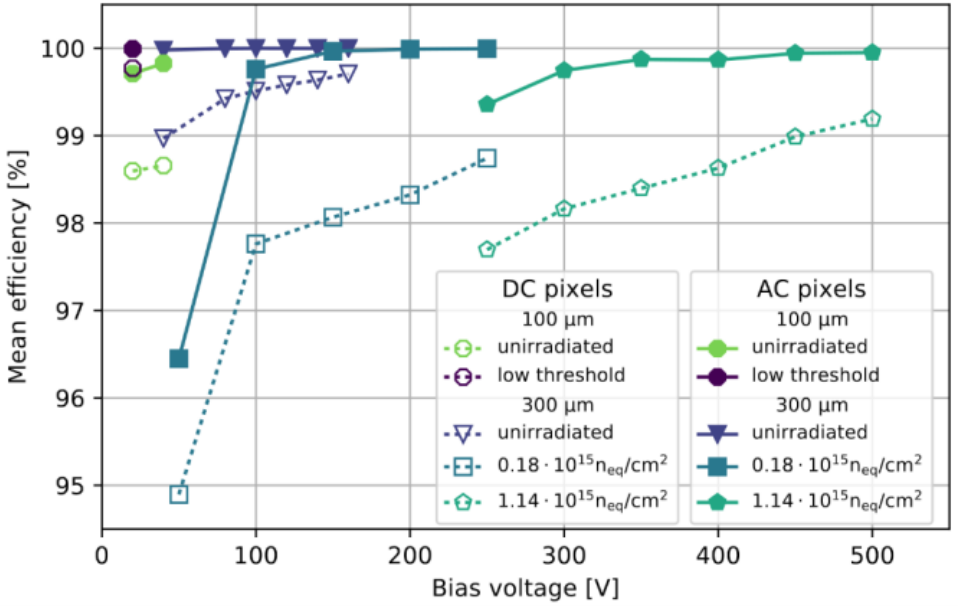
- USBpix1 … USBpix3 –> BDAQ53 (for RD53A/B)

Used Foundries for CMOS development

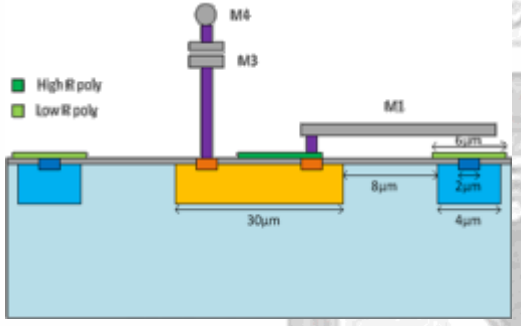
- AMS 180 nm
- **LFoundry 150 nm**
- ESPROS 150 nm
- Toshiba 130 nm
- TowerJazz 180 nm
- XFAB 180 nm

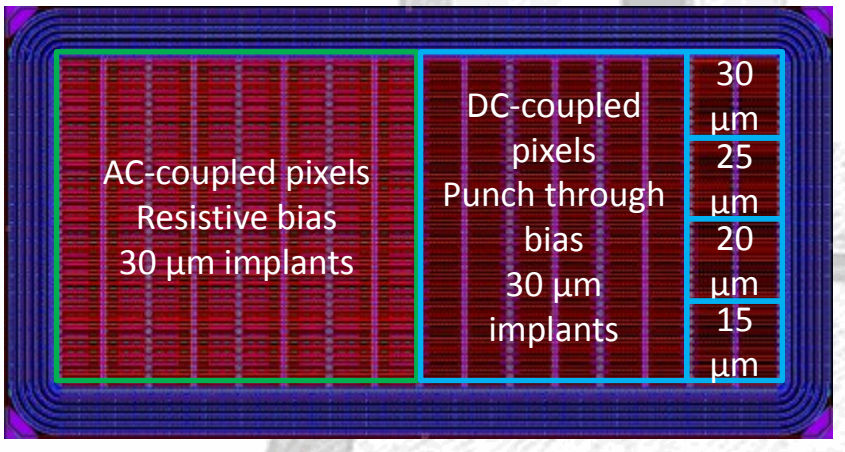
Passive LF-CMOS sensor prototype

- LFoundry 150 nm CMOS technology
- >2 kΩ-cm p-type bulk, 8“
- 100/300 µm thick, backside processed
- Bump bonded to the **ATLAS FE-I4**
- Pixel size: 50 µm x 250 µm
- Matrix size: 16 x 36 pixels (1.8 mm x 4 mm)
- Bonn + MPI

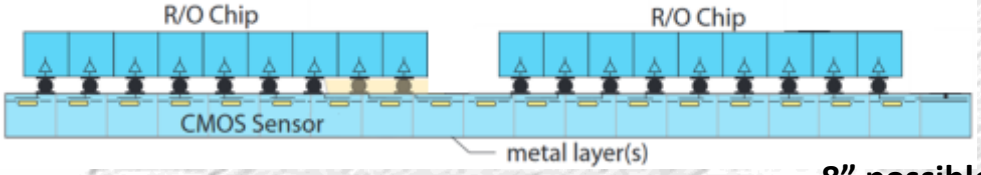


D.-L. Pohl et al., JINST 2017



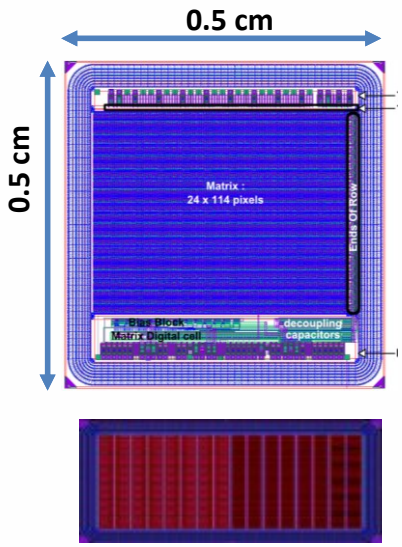


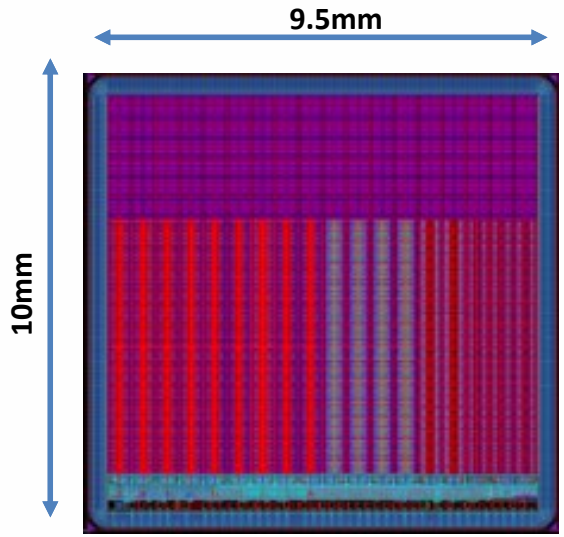
Near future (sensors for ATLAS Phase 2 Upgrade):

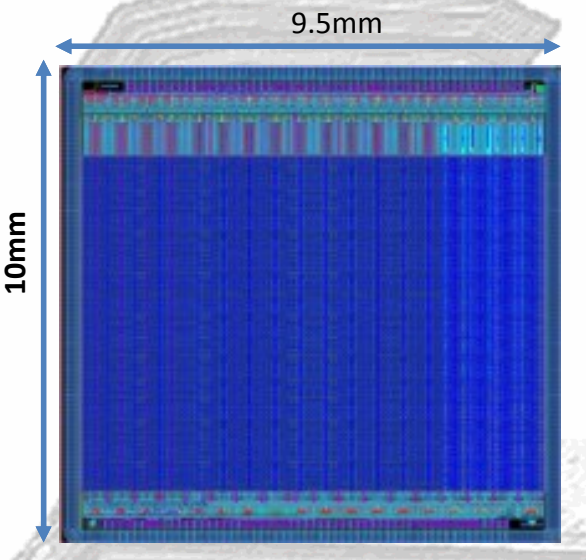


8” possible

LFoundry submission timeline







CCPD_LF prototype:

- Pixel size: 33um x 125 µm (FEI4)
- Chip size: 5 mm x 5 mm (24 x 114 pix)
- Bondable to FEI4 (+pixel encoding)
- **300um and 100um** version
- Bonn + CCPM +KIT

(Aug. 2014)

LF-CPIX (demonstrator)

- Pixel size: 50um x 250 µm
- Chip size: 9.5mm x 10 mm
- **200um and 100um version**
- Bonn + CPPM + IRFU

(April 2016)

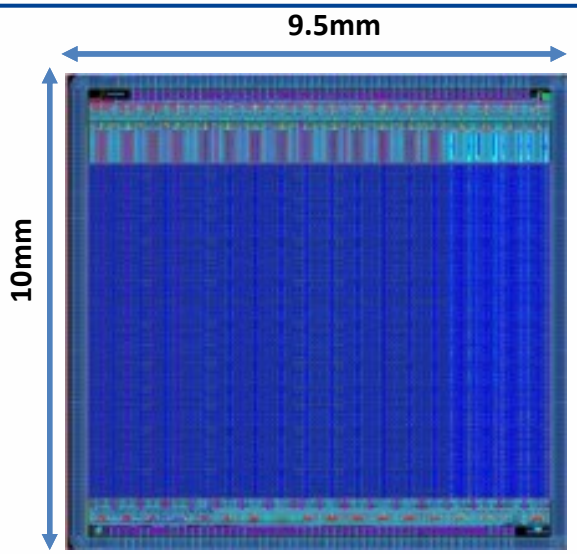
+ smaller test structures

LF-Monopix (monolithic)

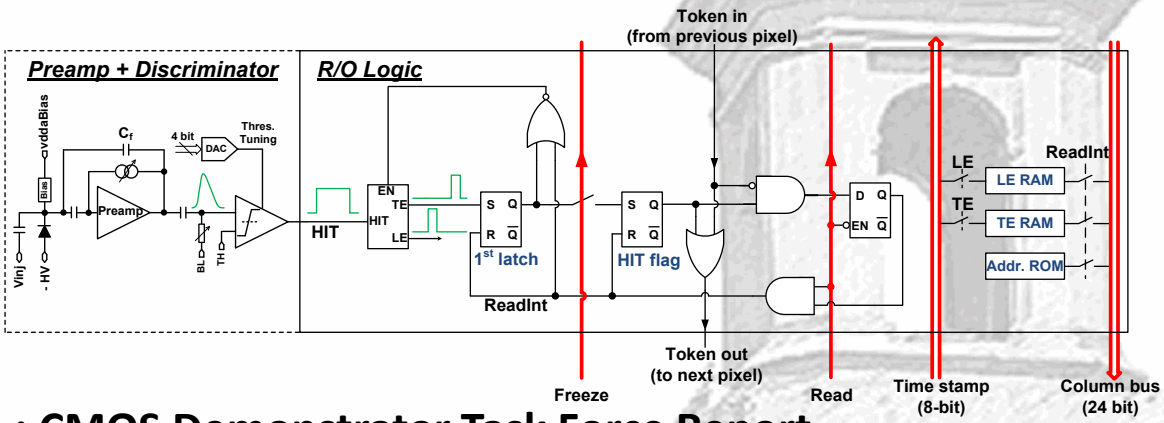
- Pixel size: 50um x 250 µm
- Chip size: 9.5mm x 10 mm
- **200um and 100um version**
- Bonn + CPPM + IRFU

(Aug. 2016)

LF-Monopix prototype



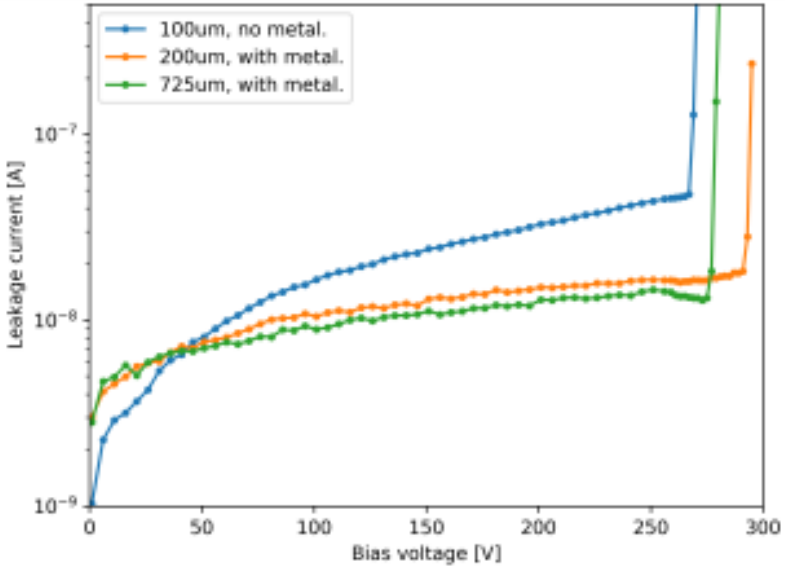
In pixel data processing:



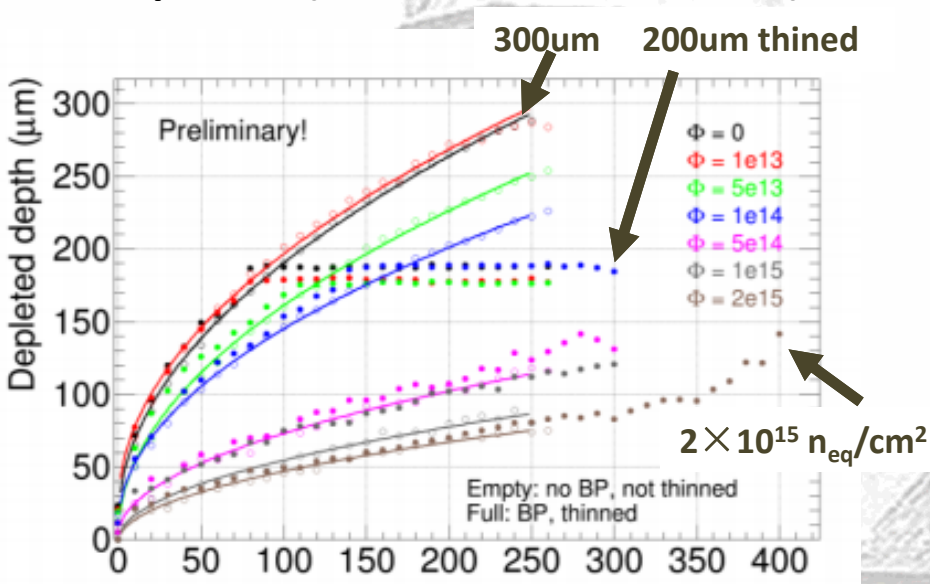
- **Design and testing according to : CMOS Demonstrator Task Force Report**
- Pixel size: 50x250 um^2 (the size is driven by historical reasons)
- Noise: ~150e- (signal for 200um is ~16000e-)
- Radiation tolerance: TID > 0.5MGray and NIEL > $10^{15}n_{eq.}$
- Readout: Data driven 40MHz time stamping
- Minimum detection threshold: ~1500e-
- Charge information: 8bit
- Thinned and back processed (BSI): 100 and 200um
- Efficiency: >99% particle (MIP) detection after high neutron/proton radaition
- Breakdown voltage: >280V (>400 on test structures)
- Data output: LVDS@160Mbit/s

LF-Monopix Results

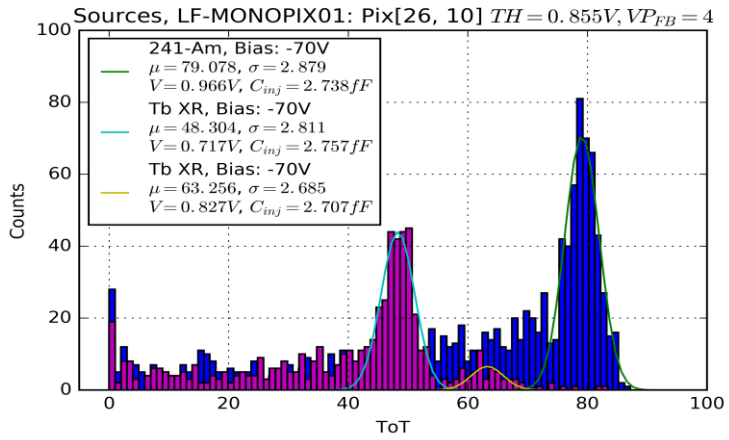
Breakdown voltage



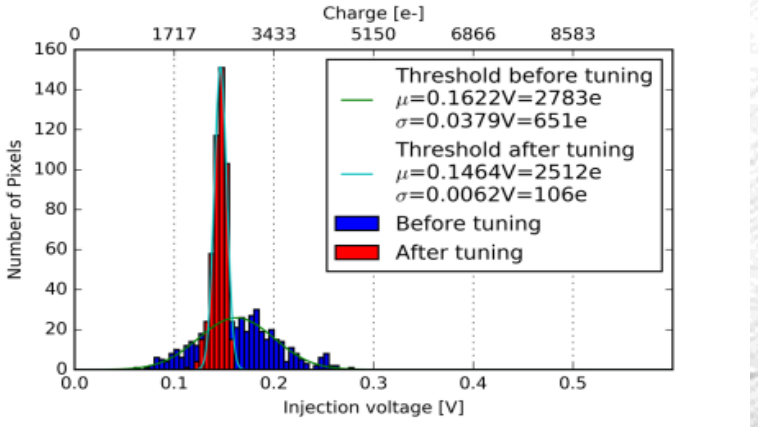
Depletion (E-TCT on test structures)



X-ray spectrum



Threshold equalization



Efficiency at ELSA (2.5GeV electrons, 775um)

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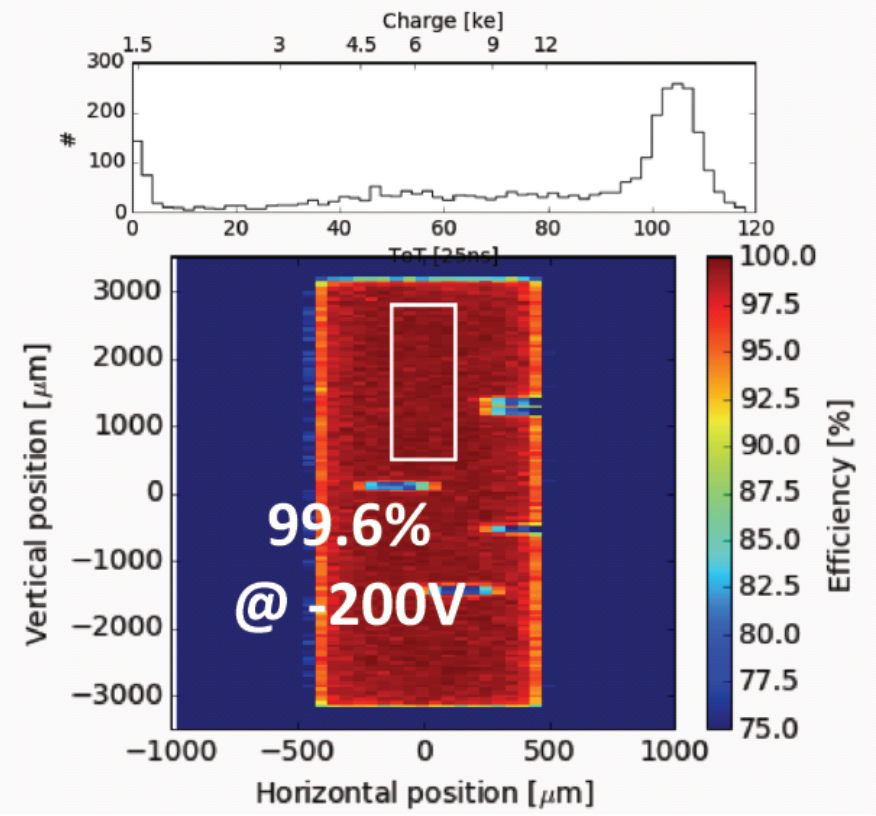
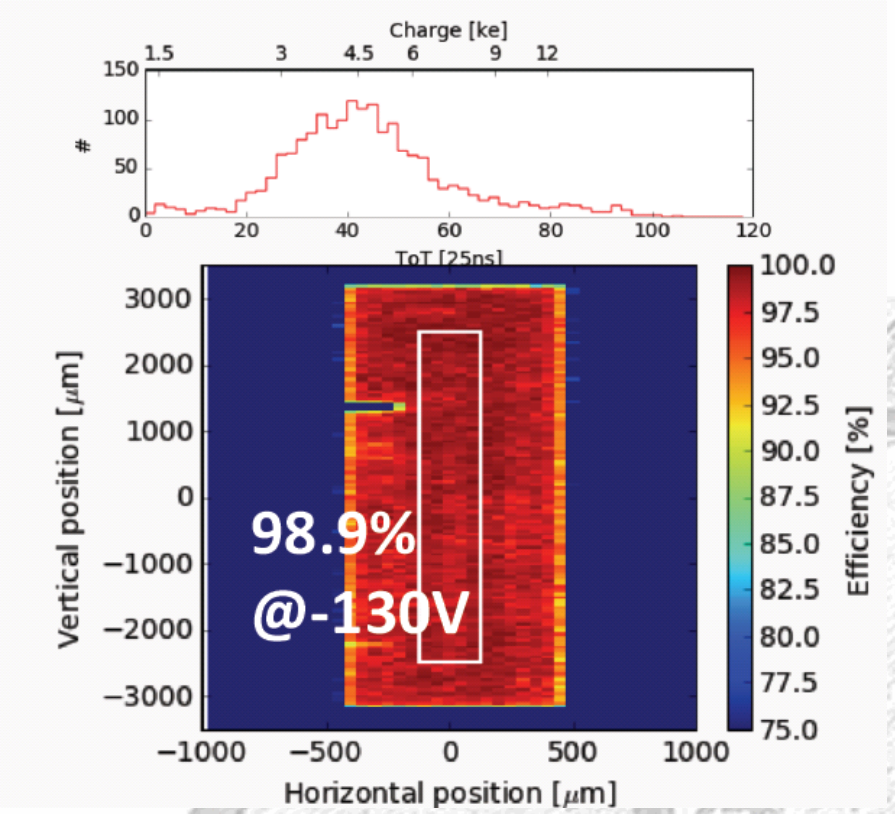
Un-irradiated



Neutron irradiated (1 x 10^{15} n_{eq}/cm^2)

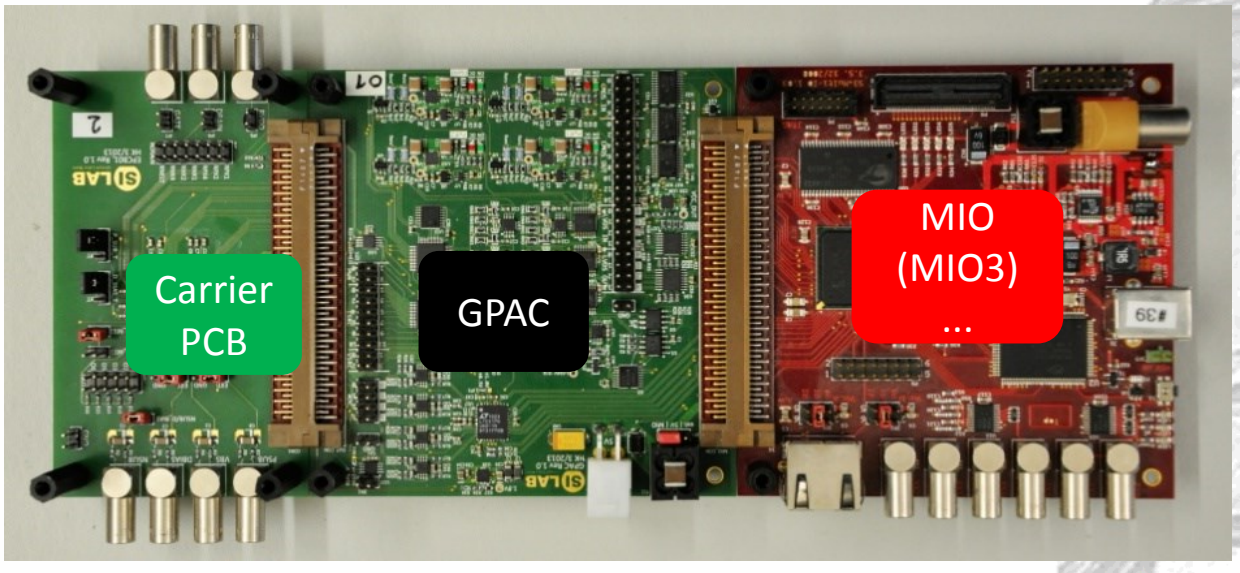


Noise rate < 10^{-6} hit/pix/s

T. Hirono, Bonn

CMOS-CSA, V1-D-Discr. Curr-Token In-pix readout

DAQ (Basil)



Modular readout system in Verilog and python.
Different communication interfaces : USB2, USB3, Gb Ethernet, UART

Successful used for different ASICS: e.g.. FE-I4, RD53A, TimePix3, Mimosa26, LF-MonoPix, TJ-Monopix ...

Based on Basil: https://github.com/SiLab-Bonn/basil

Possible contribution to RD50

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- Experience from LF/TJ-Monopix, RD53 and other monolithic designs
- Possible design contribution
  - Sensor design
  - Pixel design
  - Readout architecture
  - Digital data processing and verification
  - Gbit links
  - ShuntLDO (with Dortmund)
- Possible improvement to LF-Monopix:
  - Analog TOT
  - Smaller pixel
  - Lower digital power

Move to 110nm?

General Interest

- **Radiation hard monolithic pixel detectors (> $10^{15} n_{eq.}$) eg. MonoPix**
- Low mass/high resolution hybrid detector incorporating CMOS layer as sensor
- X-ray imaging sensors
- Timing detectors