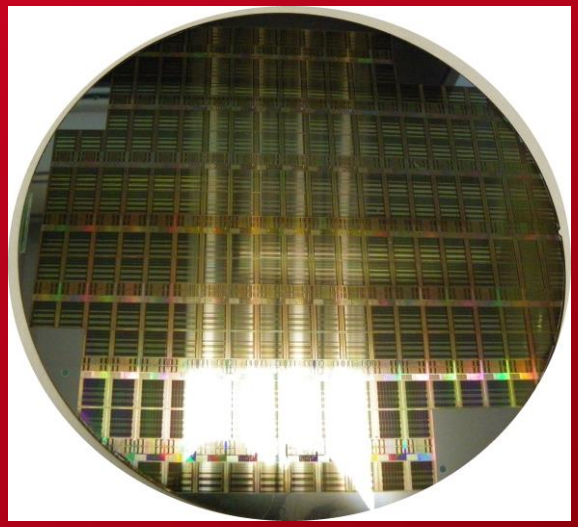
DE LA RECHERCHE À L'INDUSTRIE

cea

HVCMOS ACTIVITIES AT IRFU FOR ATLAS UPGRADES



Y. Degerli, F. Guilloux (*microelectronics design*)

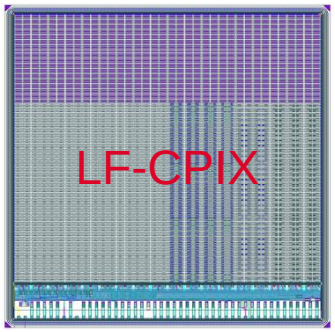
F. Balli, C. Guyot, J.P. Meyer, A. Ouraou, Ph. Schwemling, M. Vandenbroucke (*physics & instrumentation*)

www.cea.fr

Irfu

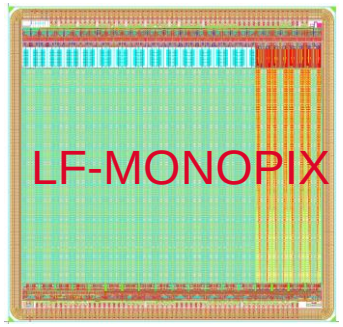
HV-CMOS SENSOR PROTOTYPES DEVELOPPED IN LF 150NM PROCESS
(FOR ATLAS UPGRADE PHASE II)

ATLAS ITk Upgrade
(Inner layers)
HV-CMOS + FE-I5



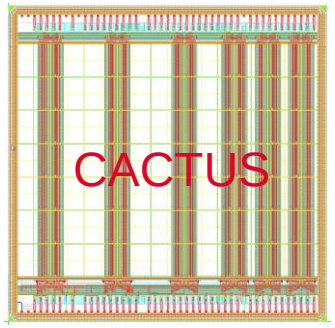
LF-CPIX demonstrator
- CPPM, **IRFU**, Bonn col.
- Sub. March 2016
- Fast R/O coupled to FE-I4
  also pixels stand alone testable
- 50 x 250 µm^2 pixels **(tracking)**
- Promising results; tests on-going

ATLAS ITk Upgrade
(Outer layers)
HV-MAPS (full monolithic)



LF-MONOPIX demonstrator
- Bonn, **IRFU**, CPPM col.
- Sub. August 2016 / Back Feb. 2017
- LF-CPIX + FE-I3 RO
- 50 x 250 µm^2 pixels **(tracking)**
- Promising results; tests on-going

ATLAS Muons High Eta Tagger Upgrade
(Other applications possible)



CACTUS demonstrator
- Mainly **IRFU** design
- Re-use of several parts of LF-CPIX
- 1 x1 mm^2 and 0.5 x 1 mm^2 pixels
- Very fast RO (**timing**)
- Expected timing resolution ≤ 100 ps
- Submitted to fabrication in Dec. 2017
- First diced wafer received last week

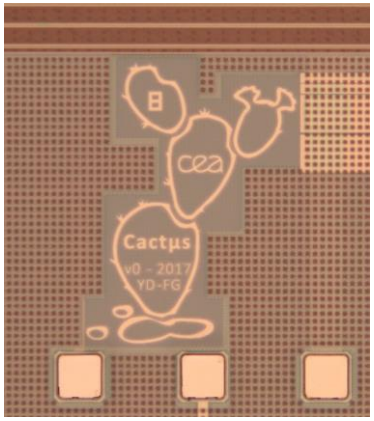
[Y. Degerli, FEE'2018, May 2018, Jouvence, CA]

yavuz.degerli@cea.fr

SUMMARY OF IRFU CONTRIBUTION TO HVCMOS CHIPS IN LF

Chip	Process	Chip size	Pixel pitch	Status	IRFU Contribution	
					Design	Tests
LF-CPIX	LFoundry 150nm HV-CMOS on HR wafers	1 cm²	50 x 250 µm²	Fabricated & Tests on-going	Strong contribution (Analog front-end design, pixel optimization, assembly, global checks and simulations)	Significant contribution to in-lab tests
LF-MONOPIX		1 cm²	50 x 250 µm²	Fabricated & Tests on-going	Significant contribution (Analog front-end design, LVDS block, global simulations)	Significant contribution to in-lab tests
CACTUS (**C**MOS **Ac**tive **T**iming **µS**ensor)		1 cm²	1 x 1 mm² & 0.5 x 1 mm²	Fabricated & Tests will start soon	Mainly IRFU design (re-use of several parts of LF-CPIX)	Test-bench developed at IRFU In-lab tests will be done at IRFU

CACTUS chips before dicing



yavuz.degerli@cea.fr

CONCLUSIONS & FUTURE

❑ CONCLUSIONS

- Very promising experimental results obtained in LF 150nm process for **tracking** with **LF-CPIX** and **LF-MONOPIX** demonstrators

❑ NEXT STEPS

- **CACTUS** timing chip designed and submitted to fabrication in December 2017
- First diced standard wafer received last week, in-lab tests will start soon
- Some wafers will be thinned and post-processed with different thicknesses (50, 100 µm et 200 µm)
- The test-bench of CACTUS is being prepared
- A high timing resolution cosmic ray telescope has been developed to characterize this chip
- A first test-beam is planned at a LINAC (5 MeV electrons) available at IRFU
- People from Fermilab propose a testbeam at Fermilab (Q4 2018)

❑ MAIN GOALS OF IRFU ARE

- Development of a CMOS monolithic sensor for ATLAS ItK
- Development of « cheap » CMOS monolithic sensor with good **timing** performance for the ATLAS Large Eta Tagger upgrade

❑ SECONDARY GOALS

- Exploration of performance of CMOS MAPS in the general HEP context, especially with LF150 technology

❑ AVAILABLE MAIN EXPERTISE AREAS

- Sensor development and characterization
- Analog/mixed design (front-end and peripheral blocks)

yavuz.degerli@cea.fr