SNS Ring BPM Old and New

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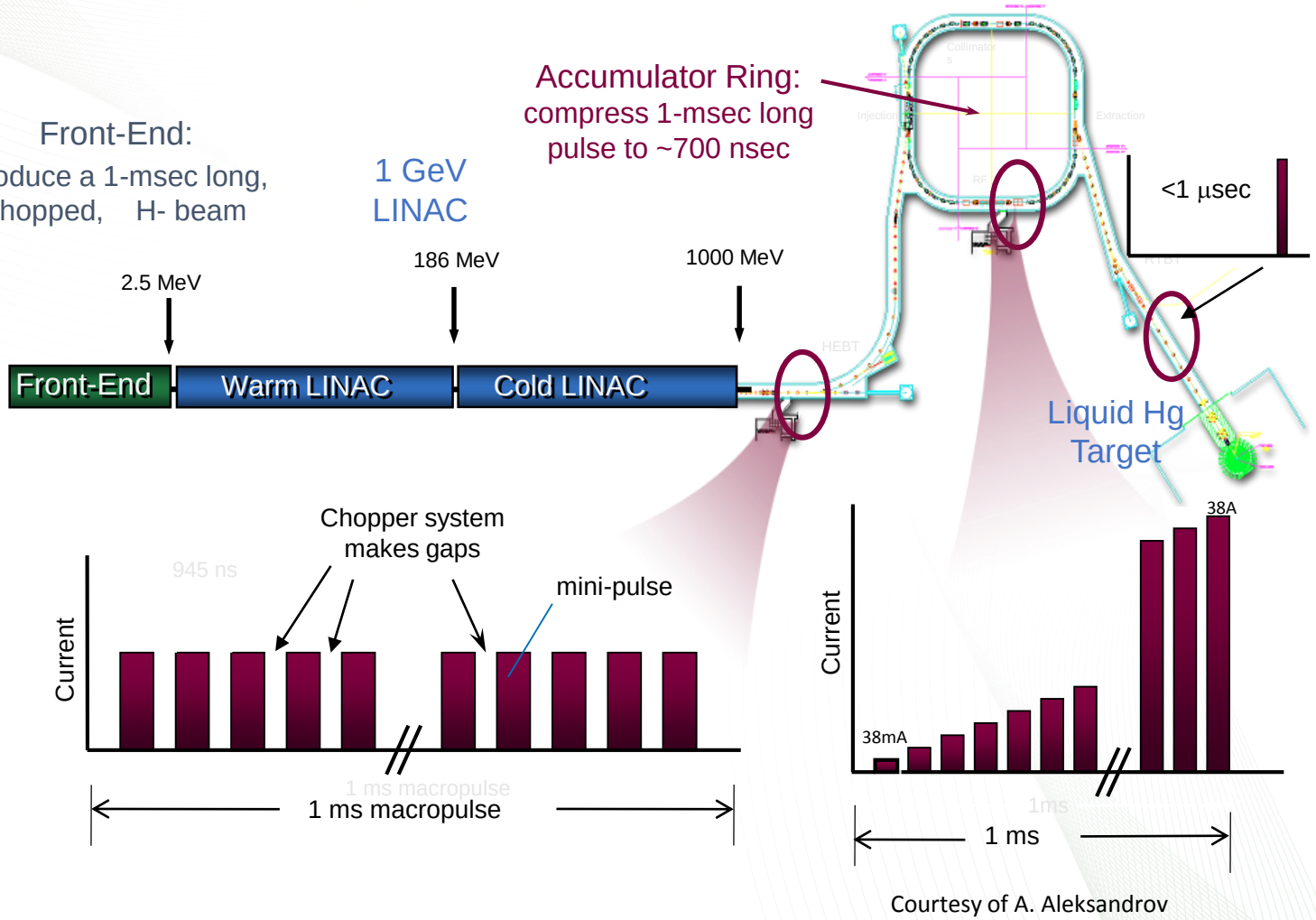
Nov 12, 2018

Topics:

- Facility overview
- Old system and requirements
- New system topology and functional diagrams
- Data compression
- Jitter reduction
- New capabilities

Spallation Neutron Source (SNS) Accelerator Complex

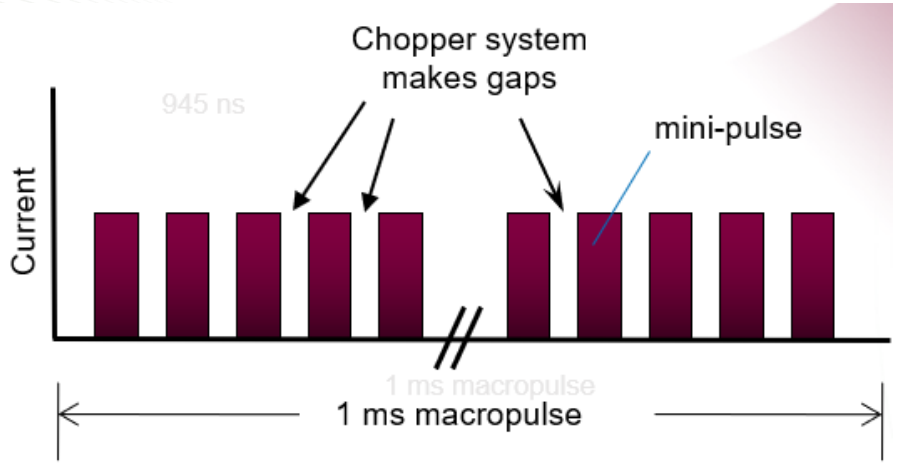


Courtesy of A. Aleksandrov

The SNS is located in Oak Ridge, Tennessee (U.S.)

OAK RIDGE National Laboratory | SPALLATION NEUTRON SOURCE

Ring Beam Structure

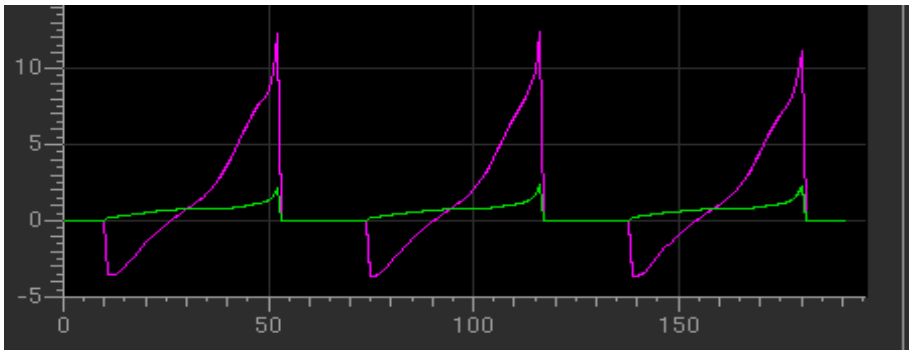


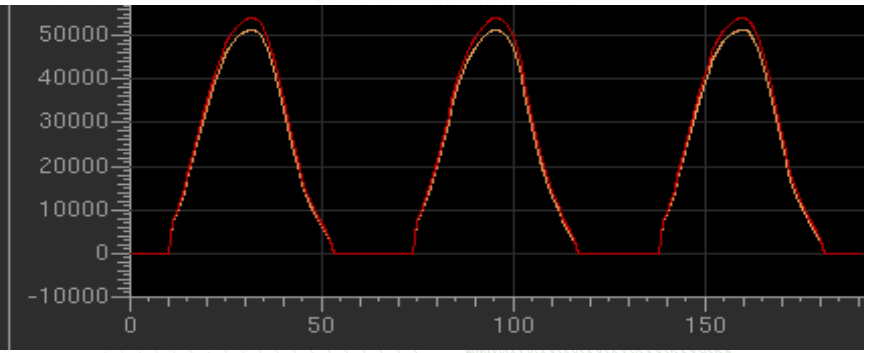
Nice square pulses: **Not!**

Beam varies within and between each turn in:

- Intensity
- Position
- Energy

Beam in 4/5 of beam turn.
(~800nS of ~1000nS)





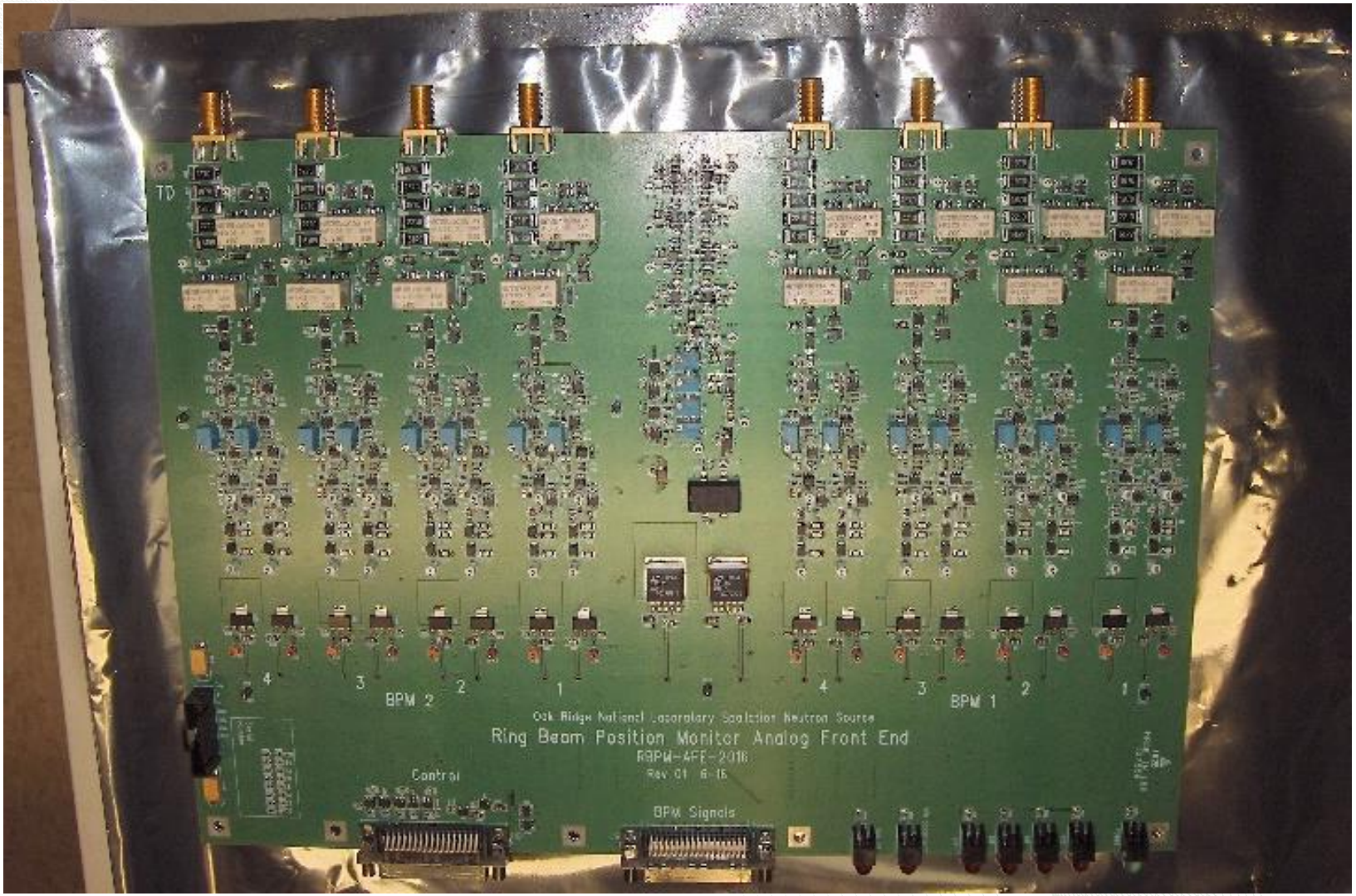
SNS Ring Beam Position Monitors (BPMs)

- 44 floated strip-line BPMs of aperture: (28) 21cm, (8) 26cm, (8) 30 cm
- Position Resolution and Accuracy of +/- 1% half aperture
- Original requirement of ~5E10 to 2E14 protons per pulse (~8mA to 35A).
  - Now ~6E9 to 6E14 ppp (~1mA to 100A)
  - Dynamic range is of major importance
- Custom made PCI AFE and digital cards (no in-house expertise)
- LV 2001 SW with Embedded Windows XP on individual PCs (one per BPM)
- Meets accuracy specs but reliability is poor

New System Motivation

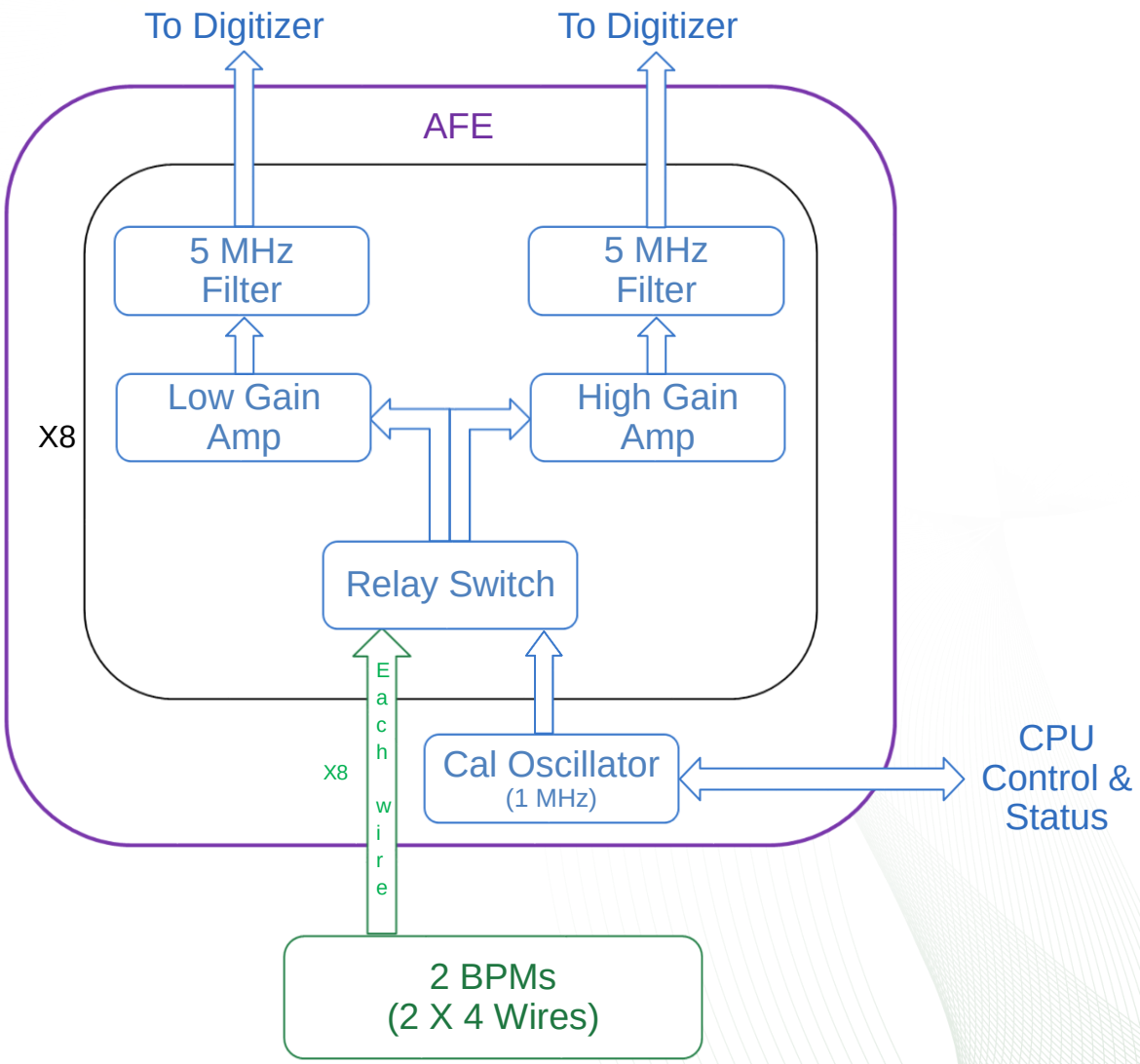
- Hardware obsolescence is major problem
  - Parts, cards, PC motherboards
- Software obsolescence is major problem
  - Impossible to upgrade OS, security concerns
- Lost ability to repair boards with personnel attrition
- Original system limited to 1Hz.
  Would like to include 60Hz acquisition.
- Long term solution: New System

New Analog Front End

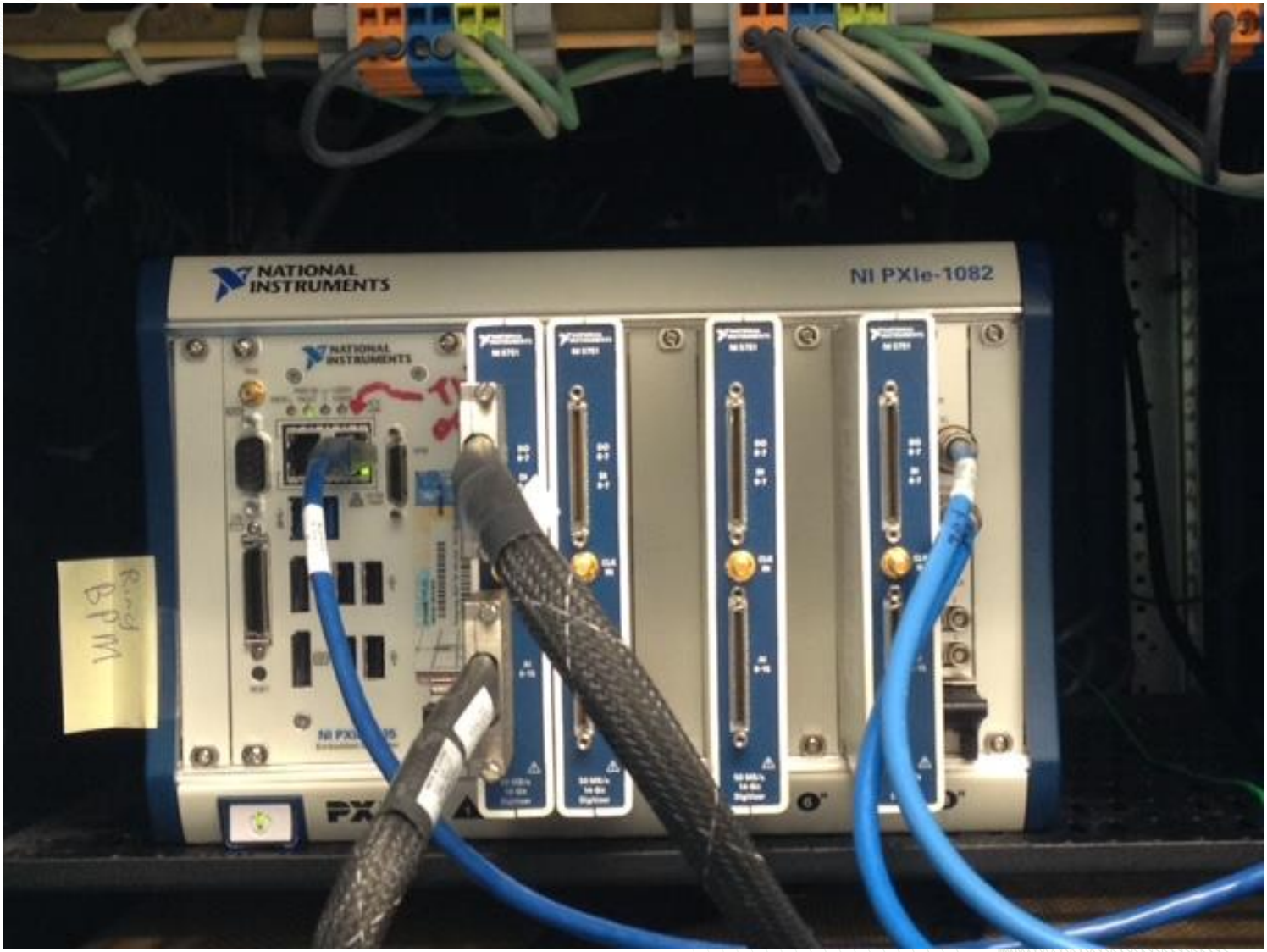


Analog Front End System Diagram

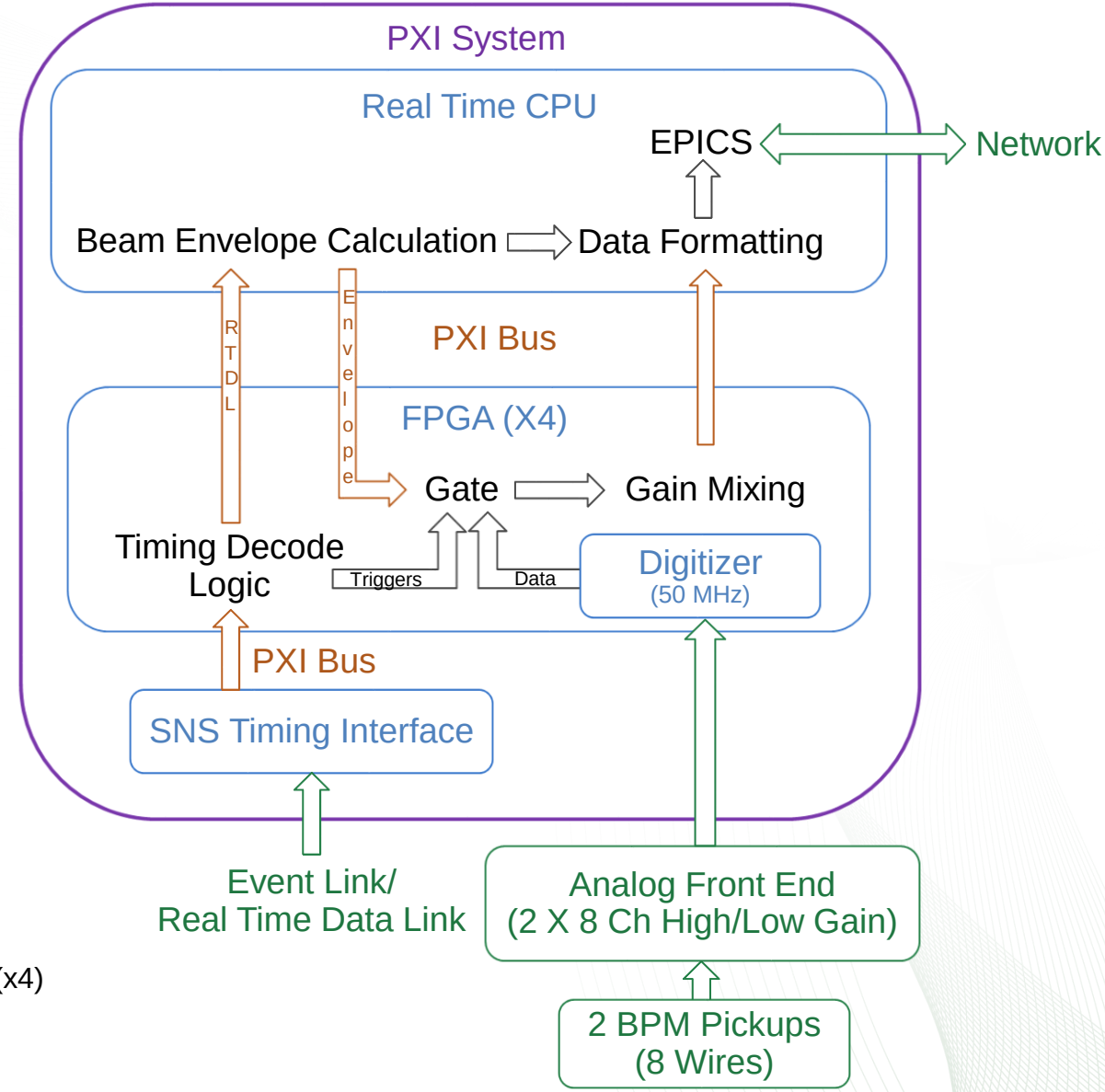
(Each AFE hosts 2 BPMs)



PXIe system with four FPGA/Digitizer(center blue), processor running LabVIEW RealTime (left) and SNS timing card (right).
1/4 space, 1/5 power consumption of previous system.



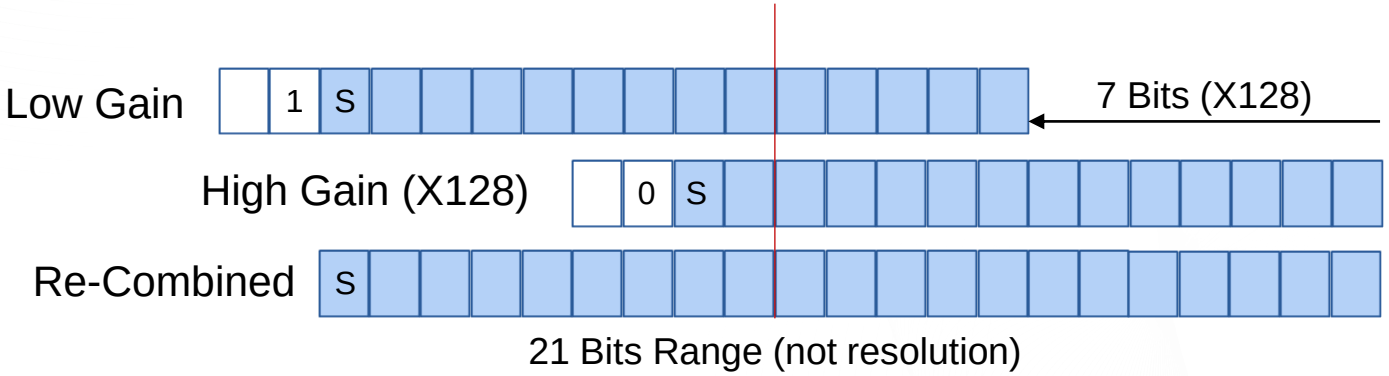
System Diagram



NI PXIe-8880 CPU
NI PXIe-7971 FPGA (x4)
NI 5751B ADC (x4)

Data Compression

ADC resolution of 14 bits delivered in 16 bits.
Each BPM wire has high and low gain analog channels (2 ADC channels)
Data is compressed by FPGA for transfer to RT CPU as follows:



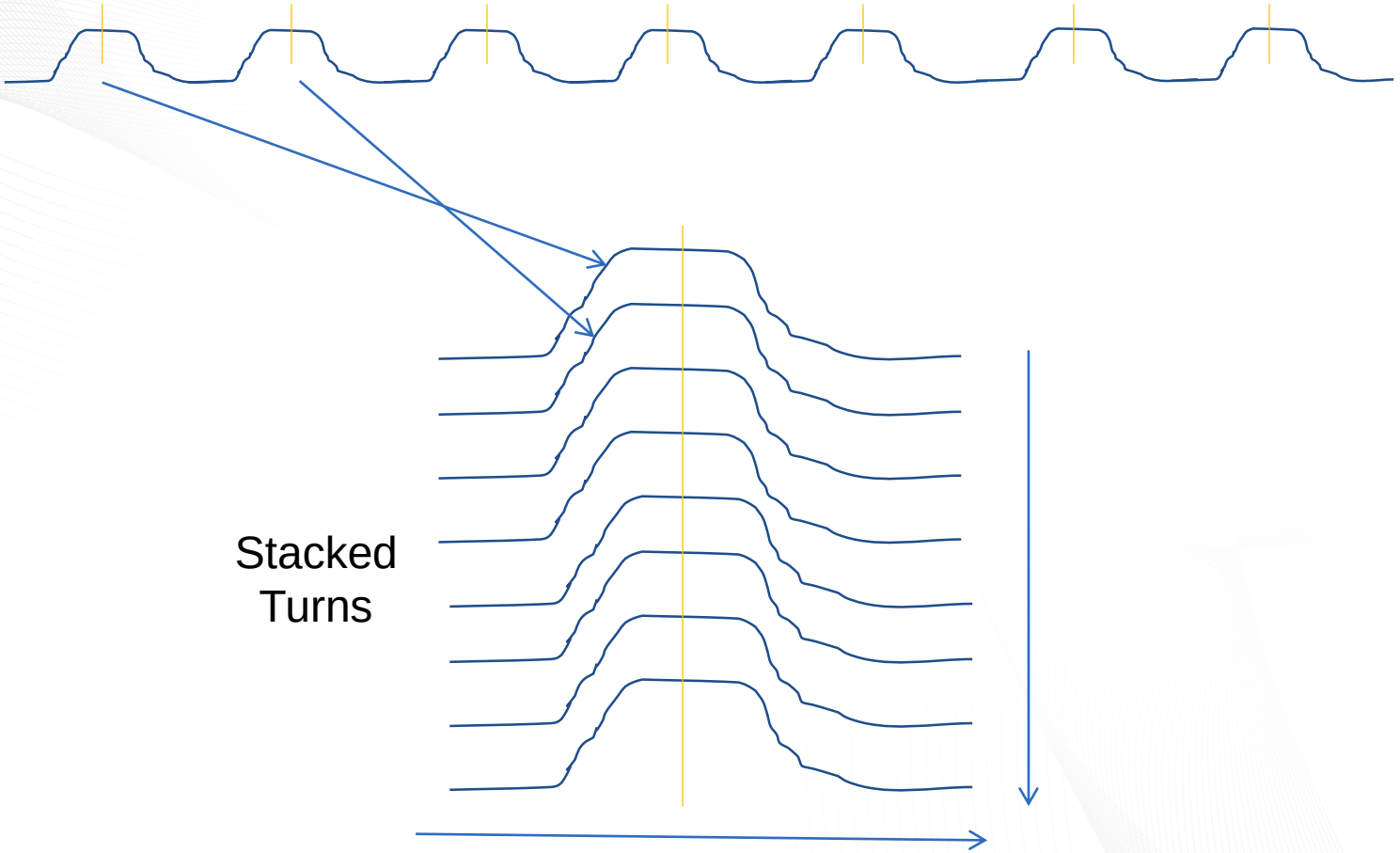
Data Rates (per BPM, after compression):

- 1 Hz rate 50 MHz full accumulation: 1.31 mS (512 kB/s)
- 60 Hz rate single turn position (22.5 kB/s)
- 60 Hz rate orbit data (30 kB/s)

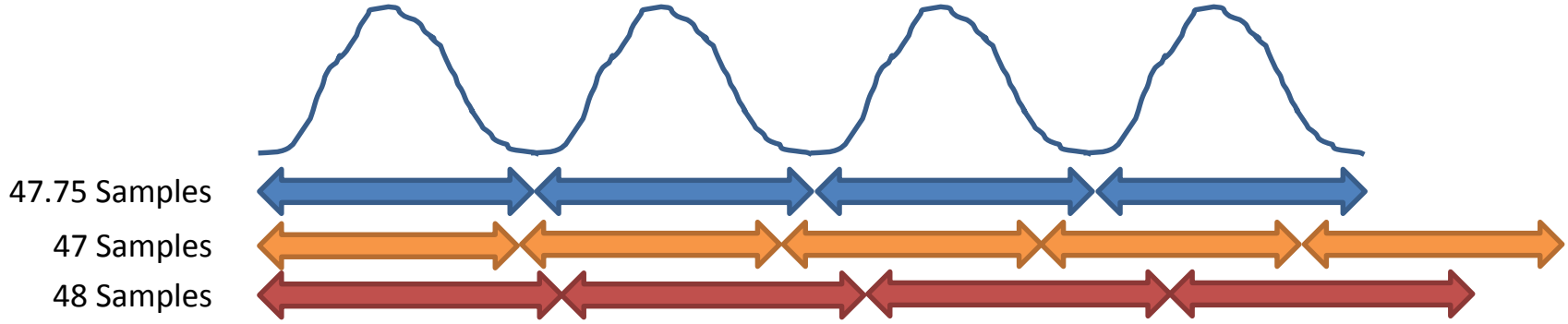
Each FPGA supports two BPMs (16 ADC channels)
Each system supports four FPGAs (64 ADC channels)

Jitter Reduction

Ring turns as seen by BPM



Jitter Type 1: Sampling Mismatch Jitter

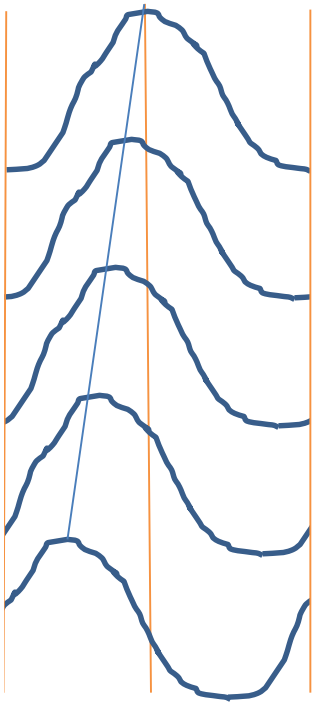


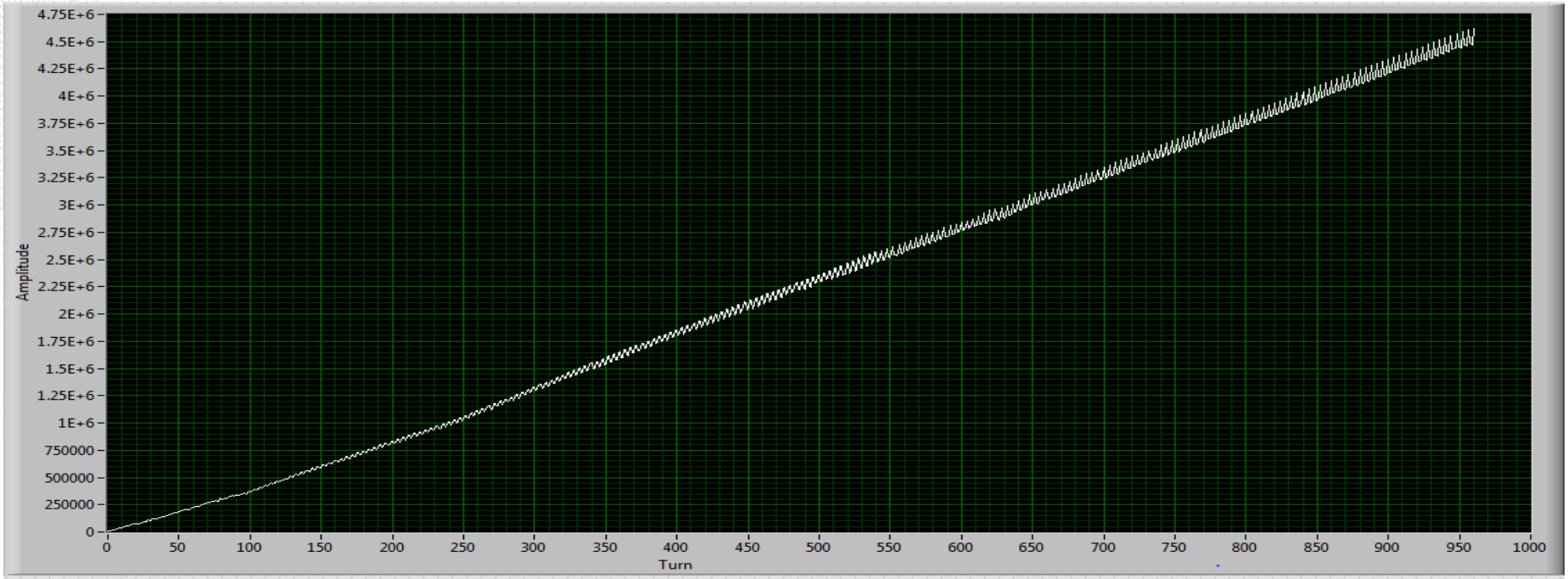
50 MHz ADC

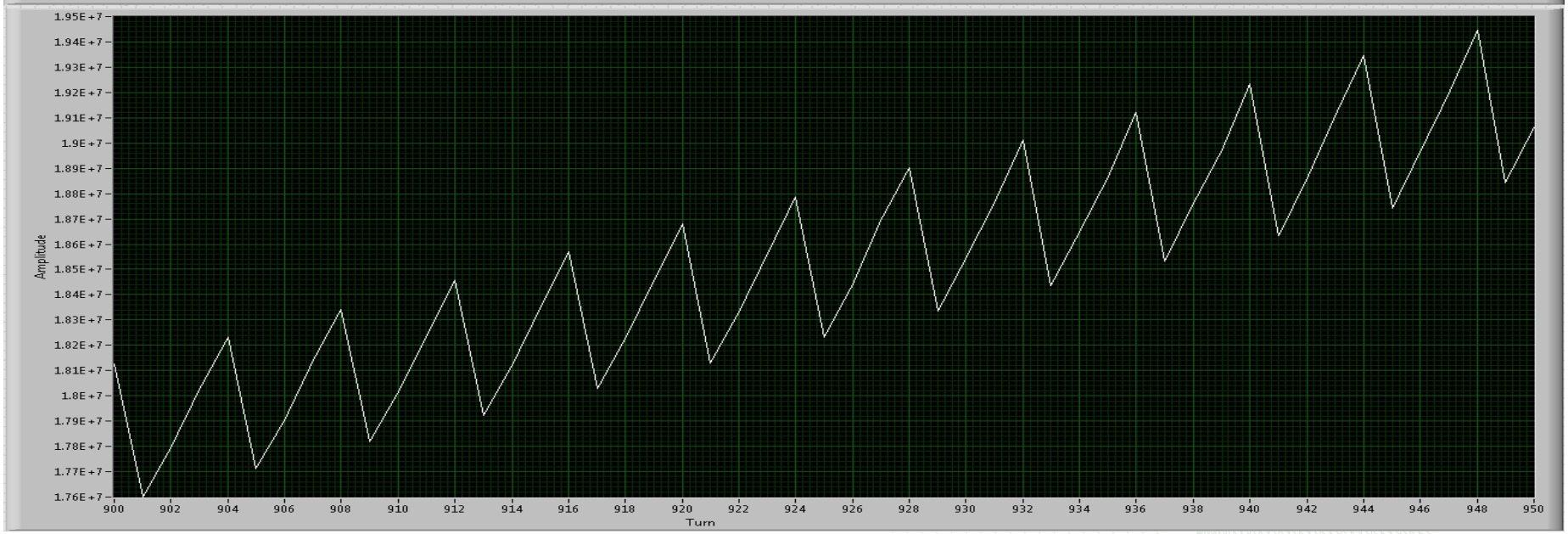
With (for example):

1.047115 MHz Ring

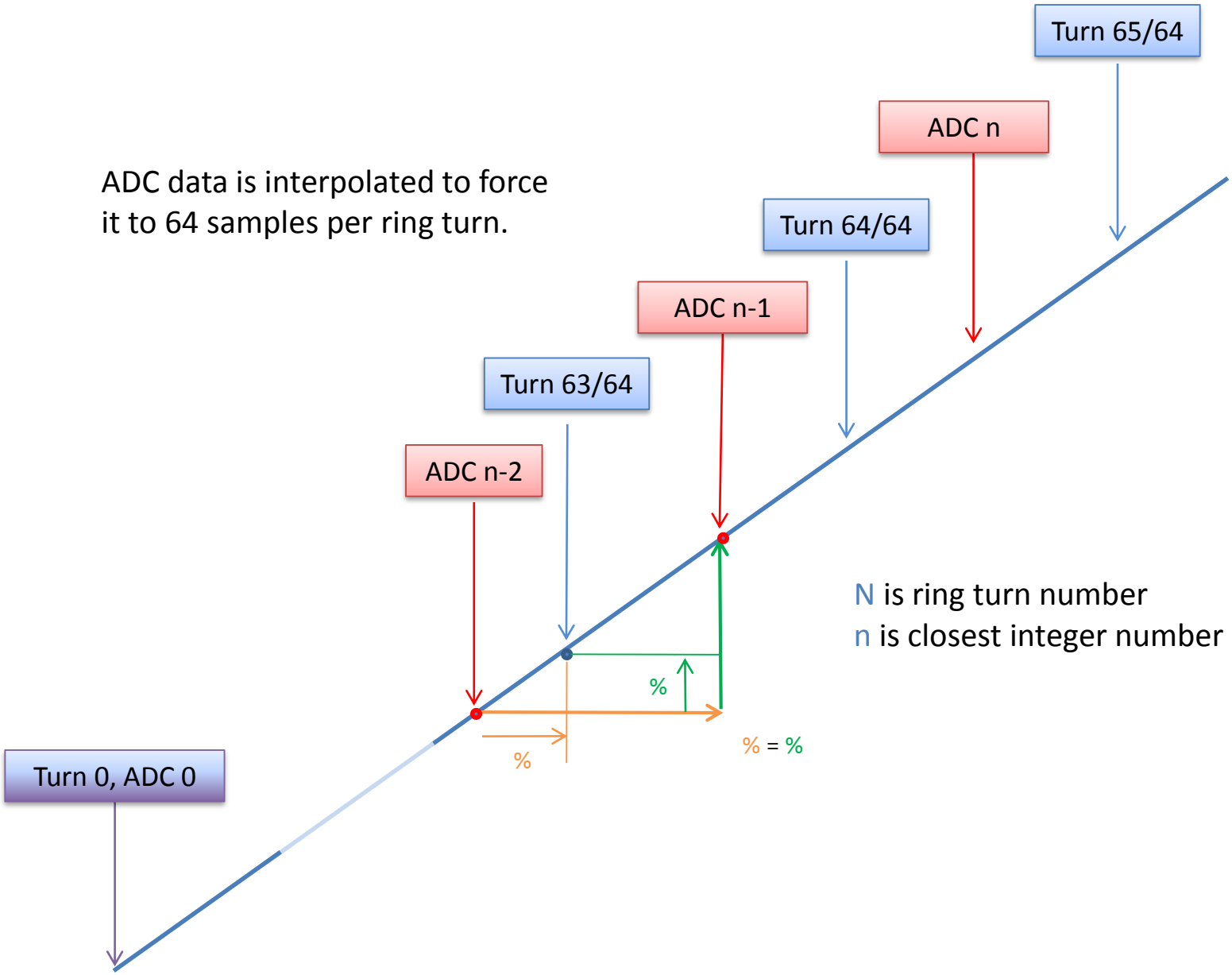
50/1.047115 = 47.75 samples/turn




Amplitude
4.75E+6
4.5E+6
4.25E+6
4E+6
3.75E+6
3.5E+6
3.25E+6
3E+6
2.75E+6
2.5E+6
2.25E+6
2E+6
1.75E+6
1.5E+6
1.25E+6
1E+6
750000
500000
250000
0
0 50 100 150 200 250 300 350 400 450 500 550 600 650 700 750 800 850 900 950 1000
Turn

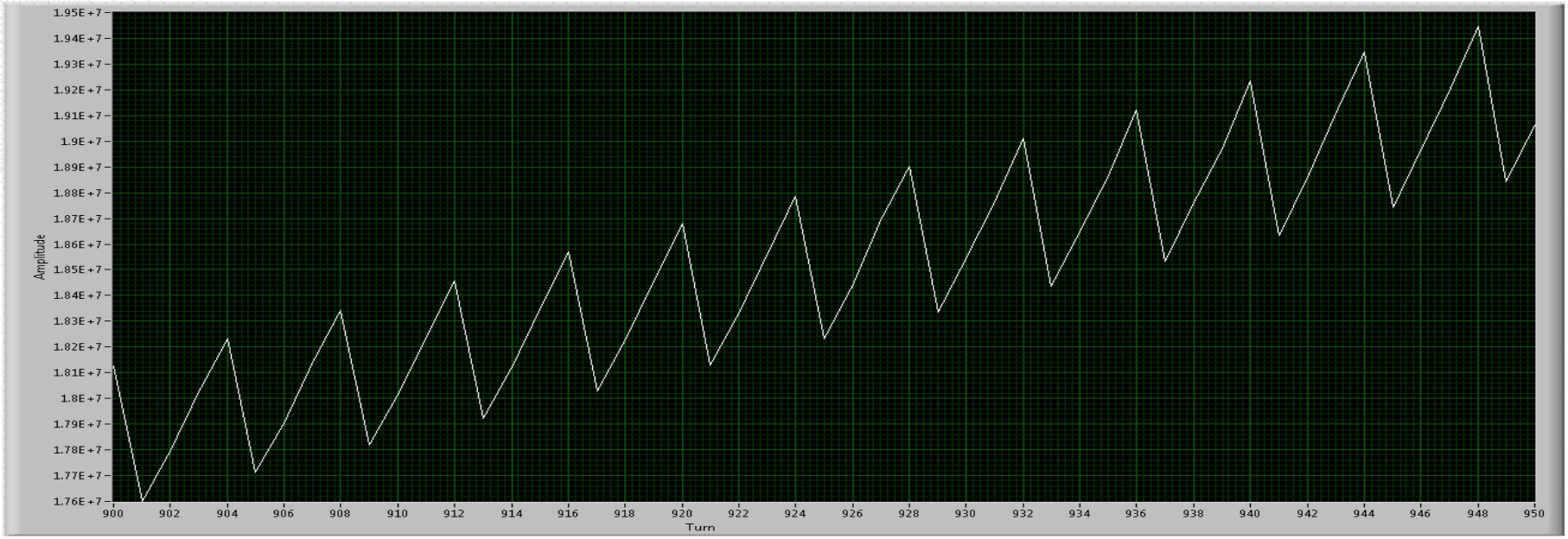

Amplitude
1.95E+7
1.94E+7
1.93E+7
1.92E+7
1.91E+7
1.9E+7
1.89E+7
1.88E+7
1.87E+7
1.86E+7
1.85E+7
1.84E+7
1.83E+7
1.82E+7
1.81E+7
1.8E+7
1.79E+7
1.78E+7
1.77E+7
1.76E+7
900 902 904 906 908 910 912 914 916 918 920 922 924 926 928 930 932 934 936 938 940 942 944 946 948 950
Turn

ADC data is interpolated to force it to 64 samples per ring turn.

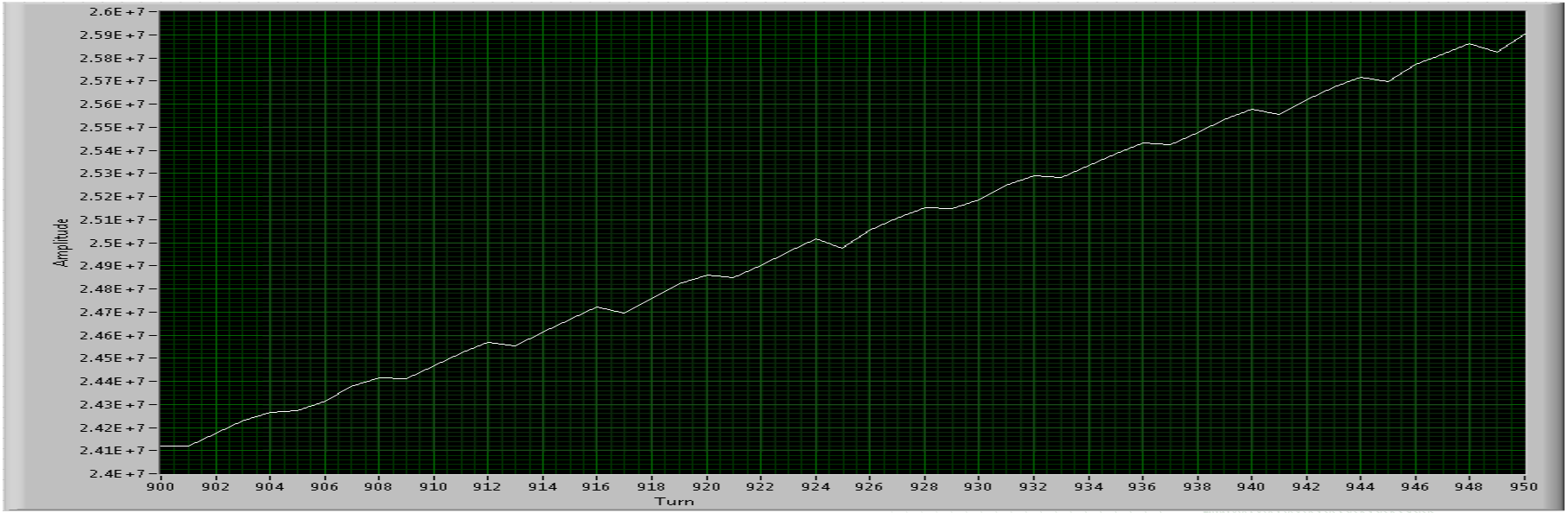


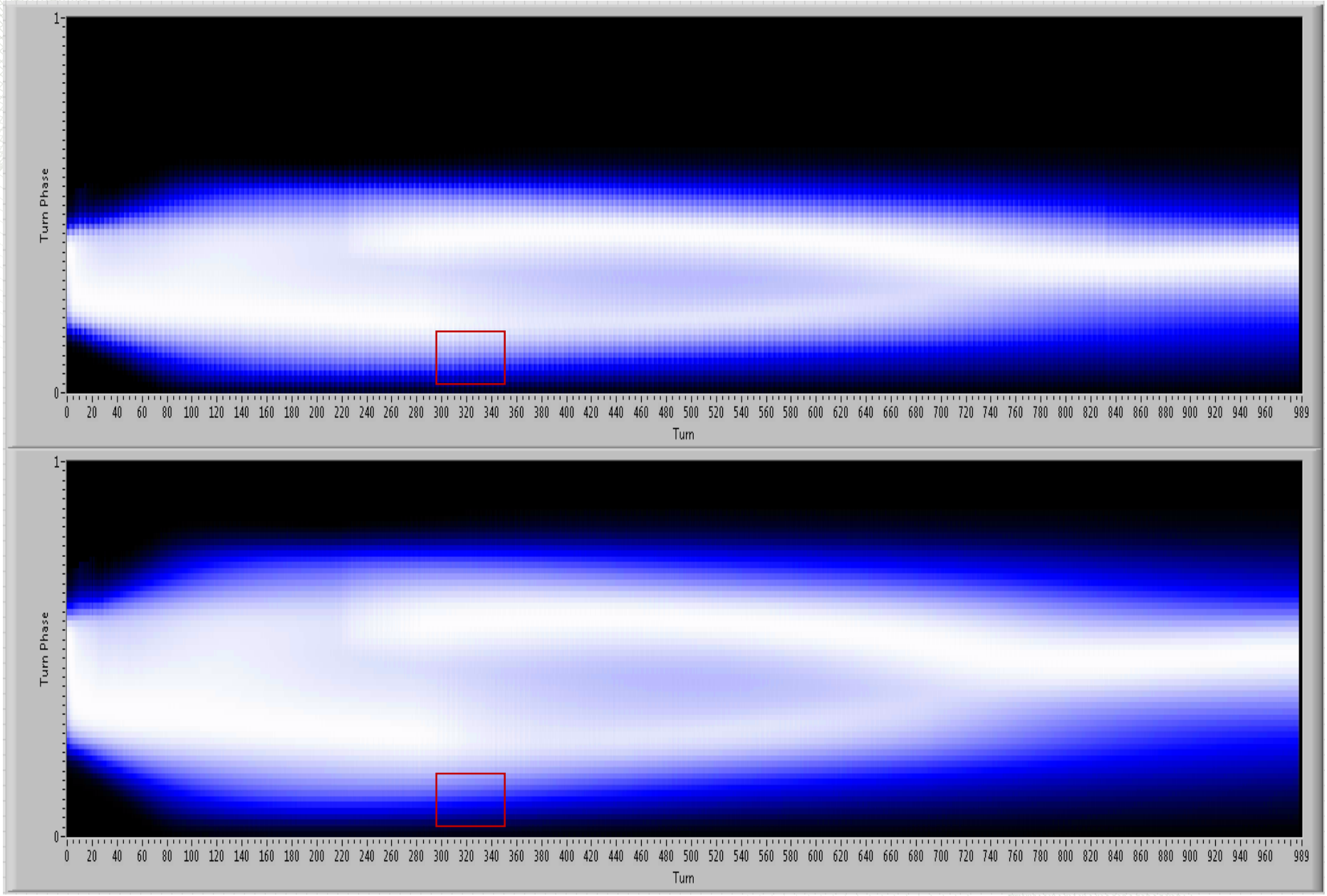
N is ring turn number
n is closest integer number of samples

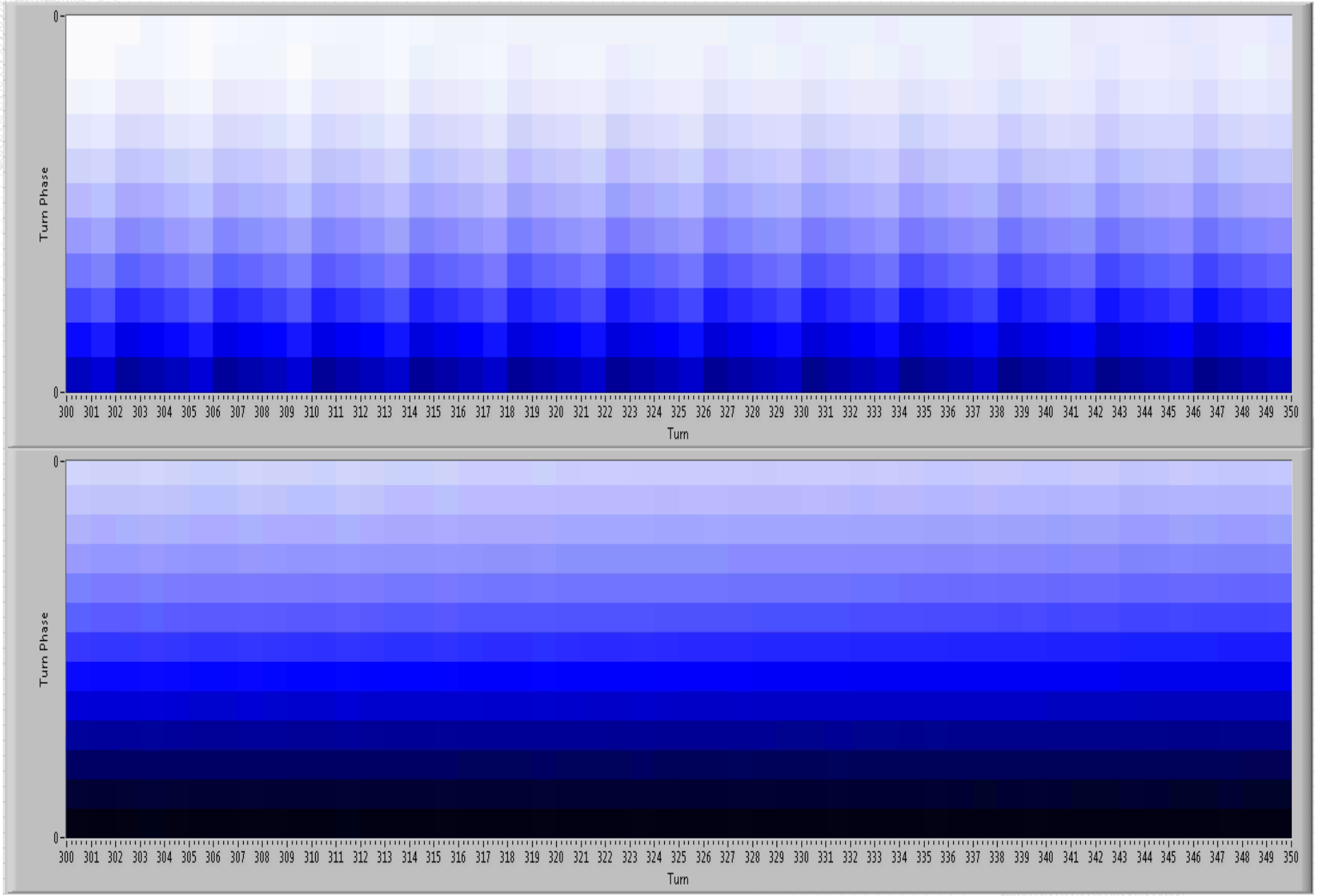
Before:



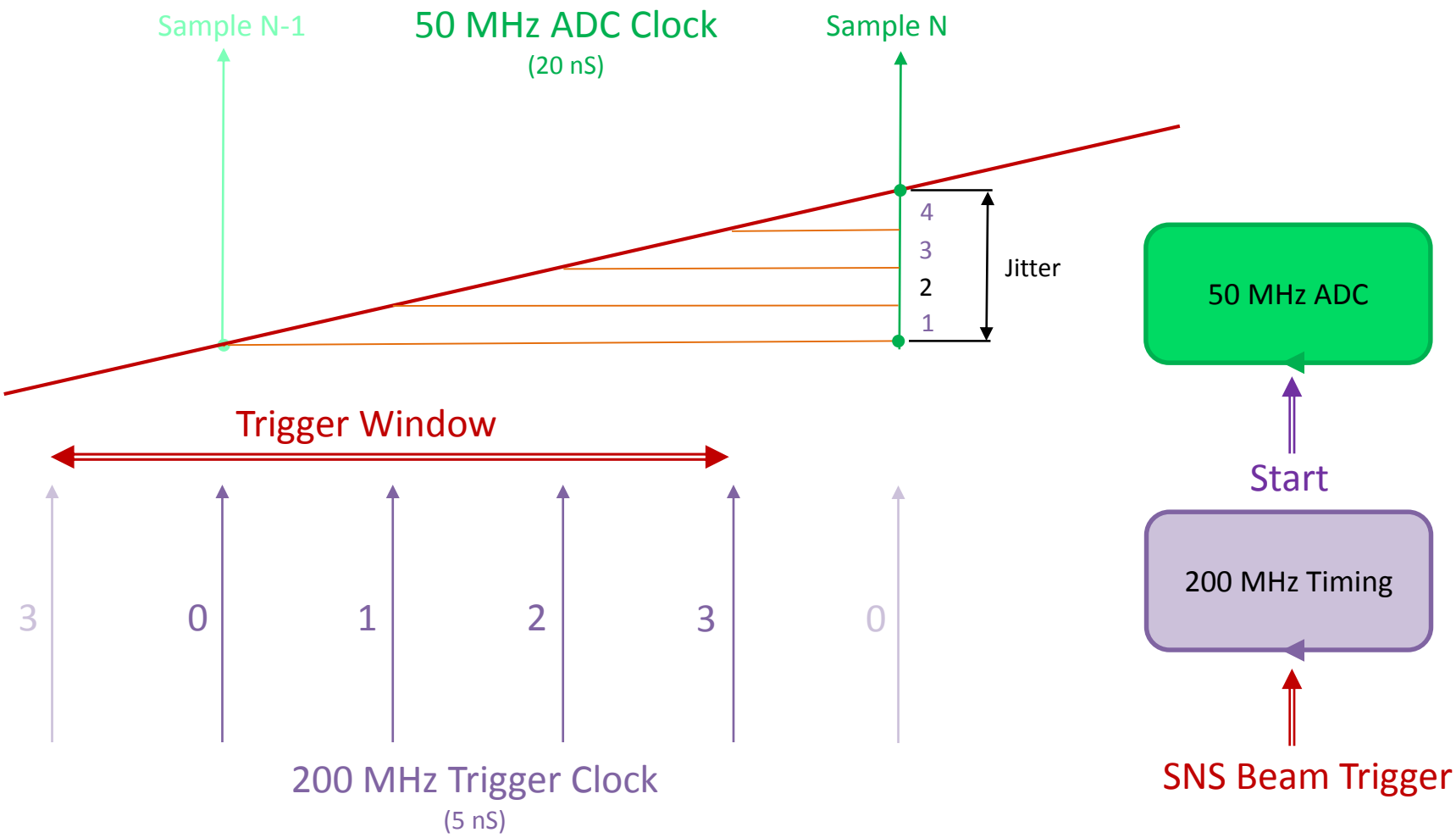
After:

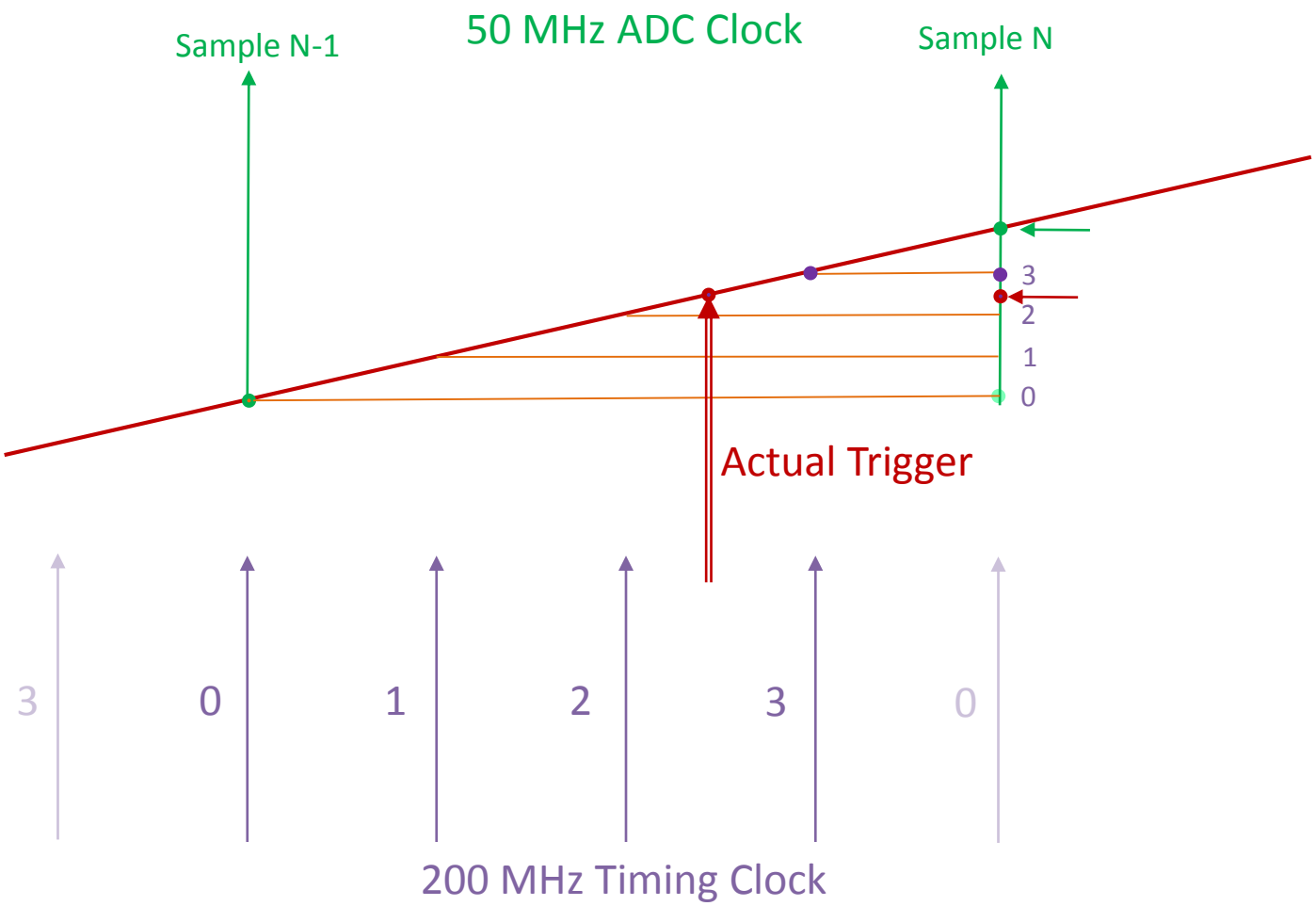


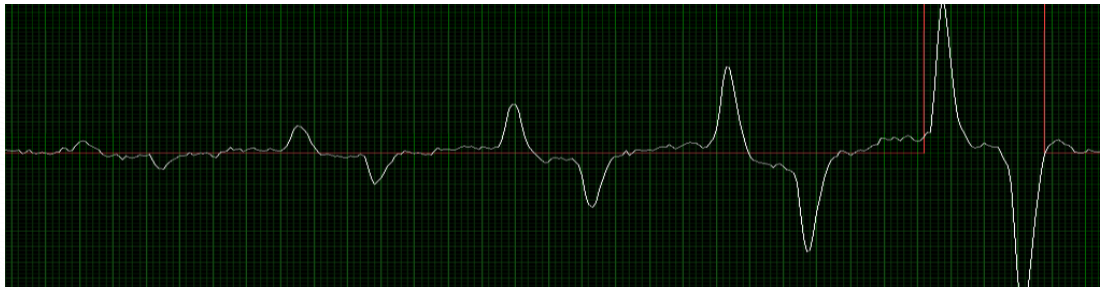

Turn Phase
1
0
0 20 40 60 80 100 120 140 160 180 200 220 240 260 280 300 320 340 360 380 400 420 440 460 480 500 520 540 560 580 600 620 640 660 680 700 720 740 760 780 800 820 840 860 880 900 920 940 960 989
Turn
Turn Phase
1
0
0 20 40 60 80 100 120 140 160 180 200 220 240 260 280 300 320 340 360 380 400 420 440 460 480 500 520 540 560 580 600 620 640 660 680 700 720 740 760 780 800 820 840 860 880 900 920 940 960 989
Turn

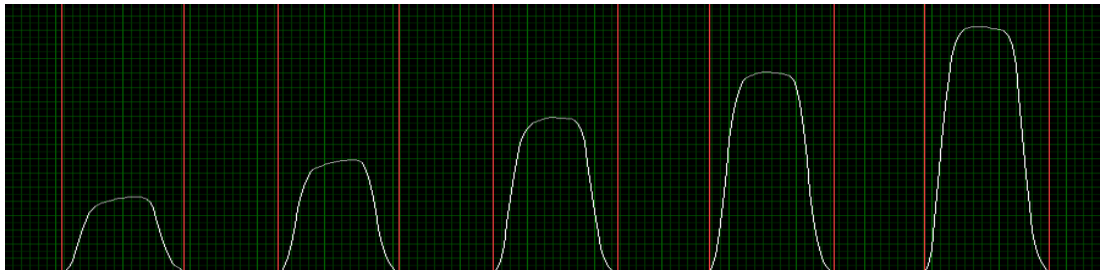

0
Turn Phase
0
300 301 302 303 304 305 306 307 308 309 310 311 312 313 314 315 316 317 318 319 320 321 322 323 324 325 326 327 328 329 330 331 332 333 334 335 336 337 338 339 340 341 342 343 344 345 346 347 348 349 350
Turn
0
Turn Phase
0
300 301 302 303 304 305 306 307 308 309 310 311 312 313 314 315 316 317 318 319 320 321 322 323 324 325 326 327 328 329 330 331 332 333 334 335 336 337 338 339 340 341 342 343 344 345 346 347 348 349 350
Turn

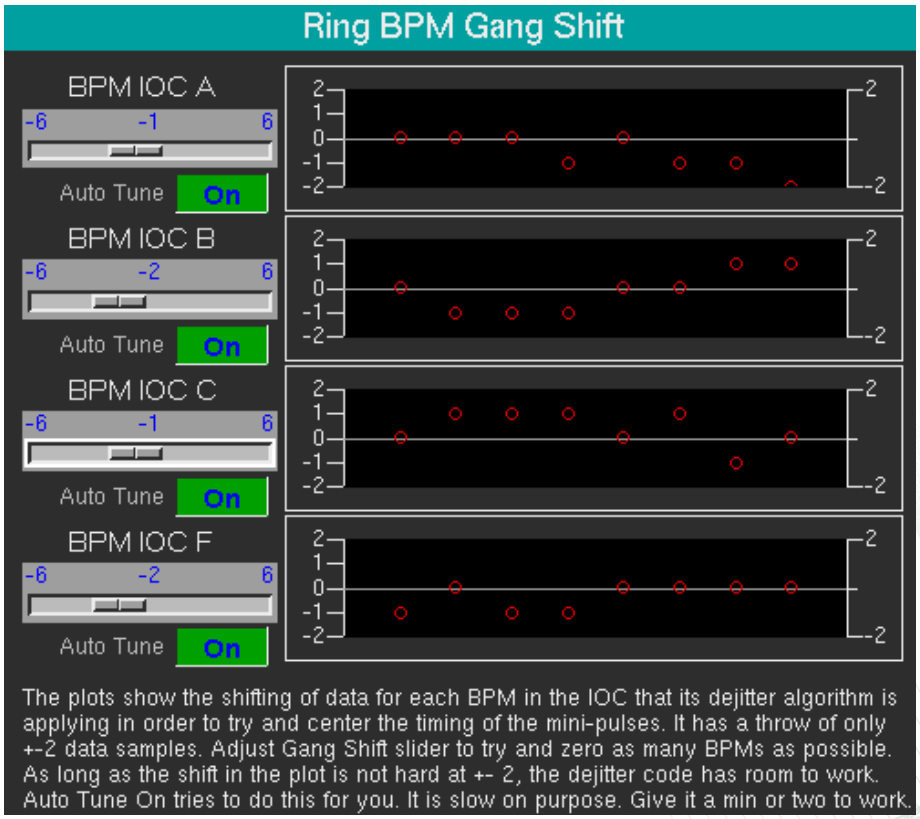
Jitter Type 2: Trigger Jitter




Sample N-1
50 MHz ADC Clock
Sample N
3
2
1
0
Actual Trigger
3
0
1
2
3
0
200 MHz Timing Clock





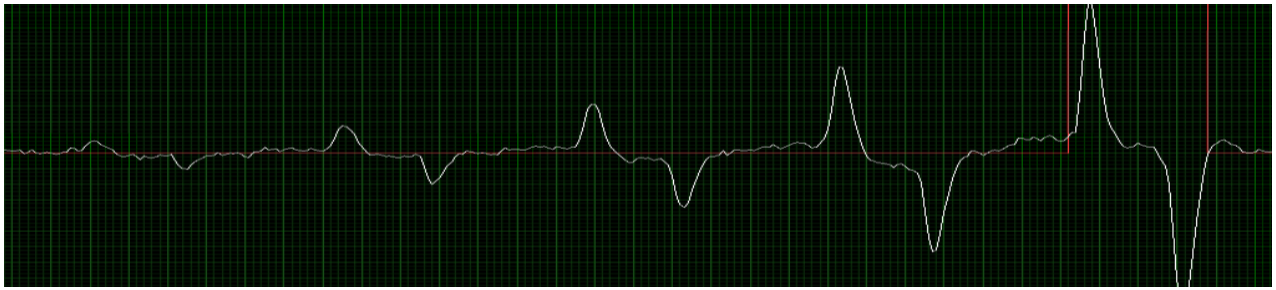

Ring BPM Gang Shift
BPM IOC A
-6
-1
6
Auto Tune
On
BPM IOC B
-6
-2
6
Auto Tune
On
BPM IOC C
-6
-1
6
Auto Tune
On
BPM IOC F
-6
-2
6
Auto Tune
On
2
1
0
-1
-2
The plots show the shifting of data for each BPM in the IOC that its dejitter algorithm is applying in order to try and center the timing of the mini-pulses. It has a throw of only +-2 data samples. Adjust Gang Shift slider to try and zero as many BPMs as possible. As long as the shift in the plot is not hard at +- 2, the dejitter code has room to work. Auto Tune On tries to do this for you. It is slow on purpose. Give it a min or two to work.

New Features

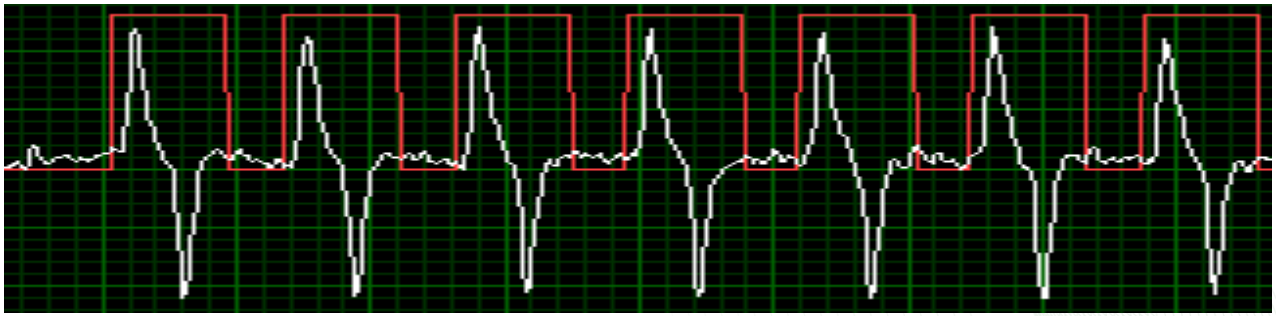
- Orbit synthesis
- Centroid/Peak phase display
- Single turn motion
- Combined screen

Orbit Synthesis

Multi Pulse Beam



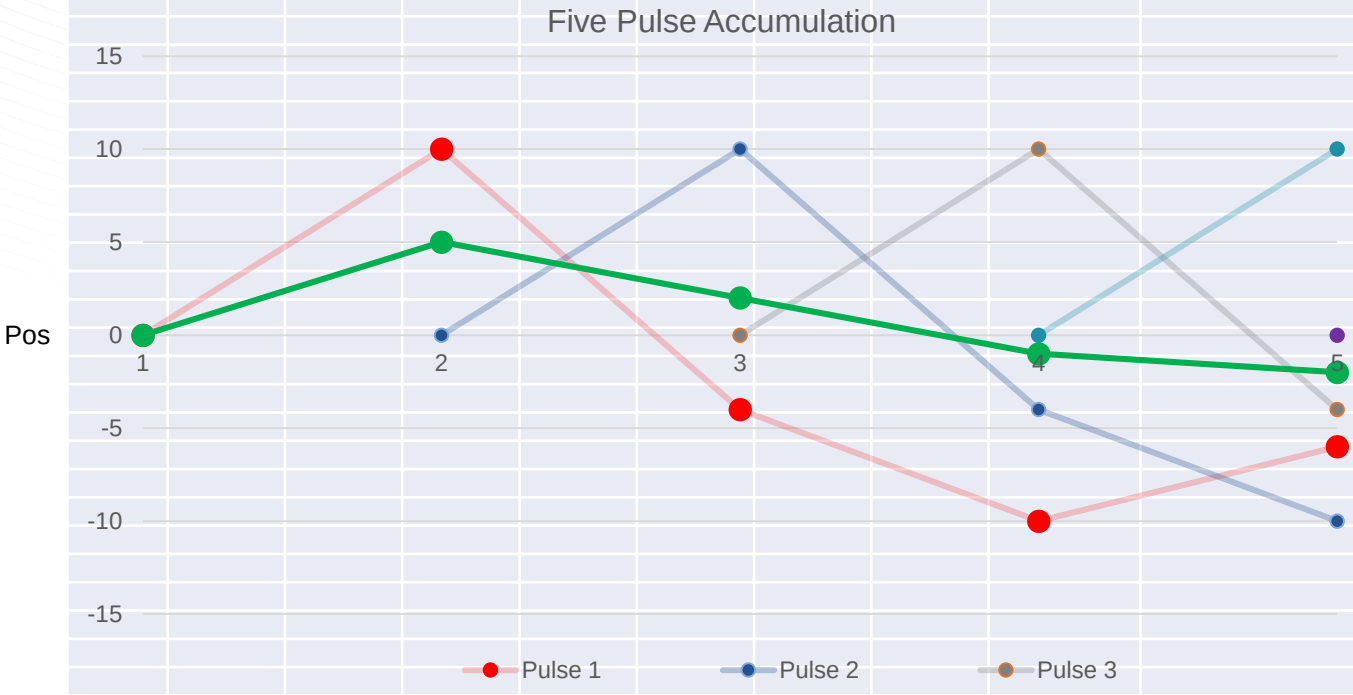
Single Pulse Beam (many Stored Turns)



(Used during tuning to compute “Orbit” of particles in ring)

Single Pulse Orbit De-Convolution

Turn	Pulse 1	Pulse 2	Pulse 3	Pulse 4	Pulse 5	Measured M
1	0					0
2	10	0				5
3	-4	10	0			2
4	-10	-4	10	0		-1
5	-6	-10	-4	10	0	-2

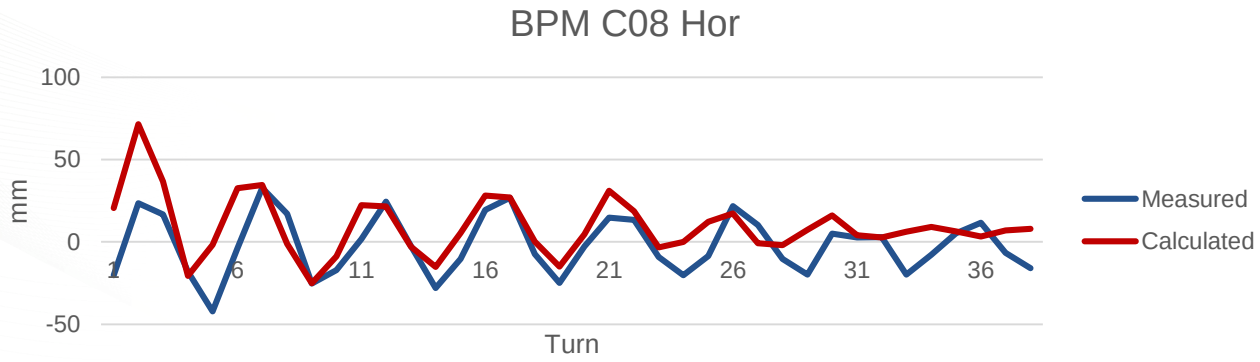


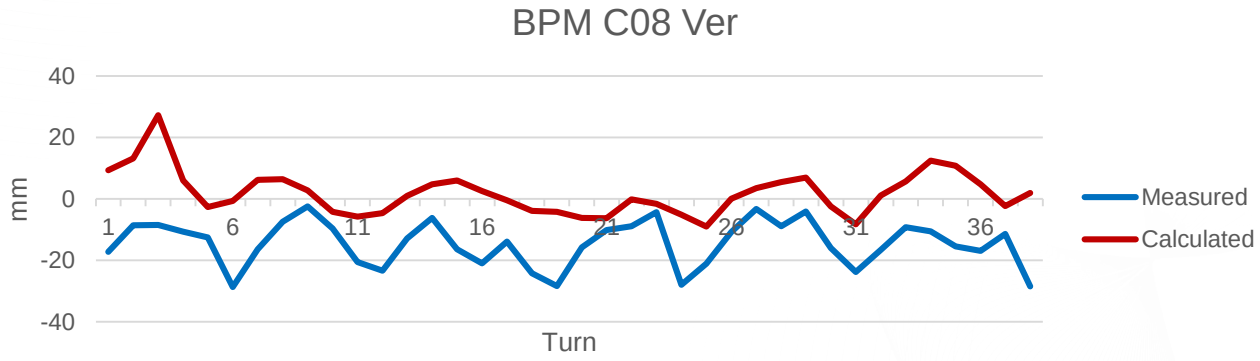
On1 = Om1	M1 = O11			O11 = M1
On2 = Om2	M2 = (O12+O21)/2	2*M2 = O12+O21	O12 = 2*M2 - O21	O12 = 2*M2 - M1
…	M3 = (O13+O22+O31)/3	3*M3 = O13+O22+O31	O13 = 3*M3-(O22+O31)	O13 = 3*M3 - 2*M2
Ont = Omt	M4 = (O14+O23+O32+O41)/4	4*M4 = O14+O23+O32+O41	O14 = 4*M4-(O23+O32+O41)	O14 = 4*M4 - 3*M3

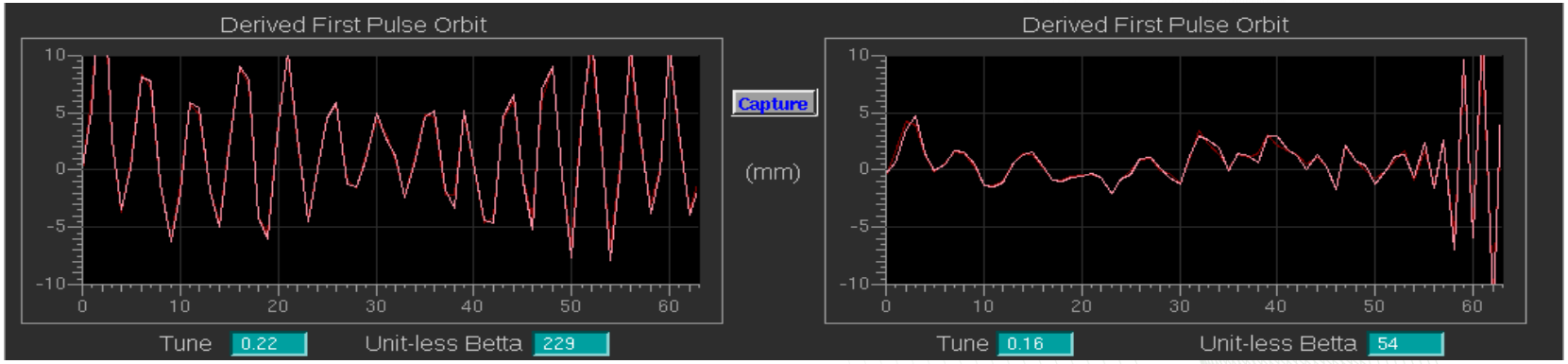
* Ont is the orbit (position) of the n'th injected pulse on its t'th turn around the ring.

Mt is the measured agragate position of all mini-pulses on turn t.

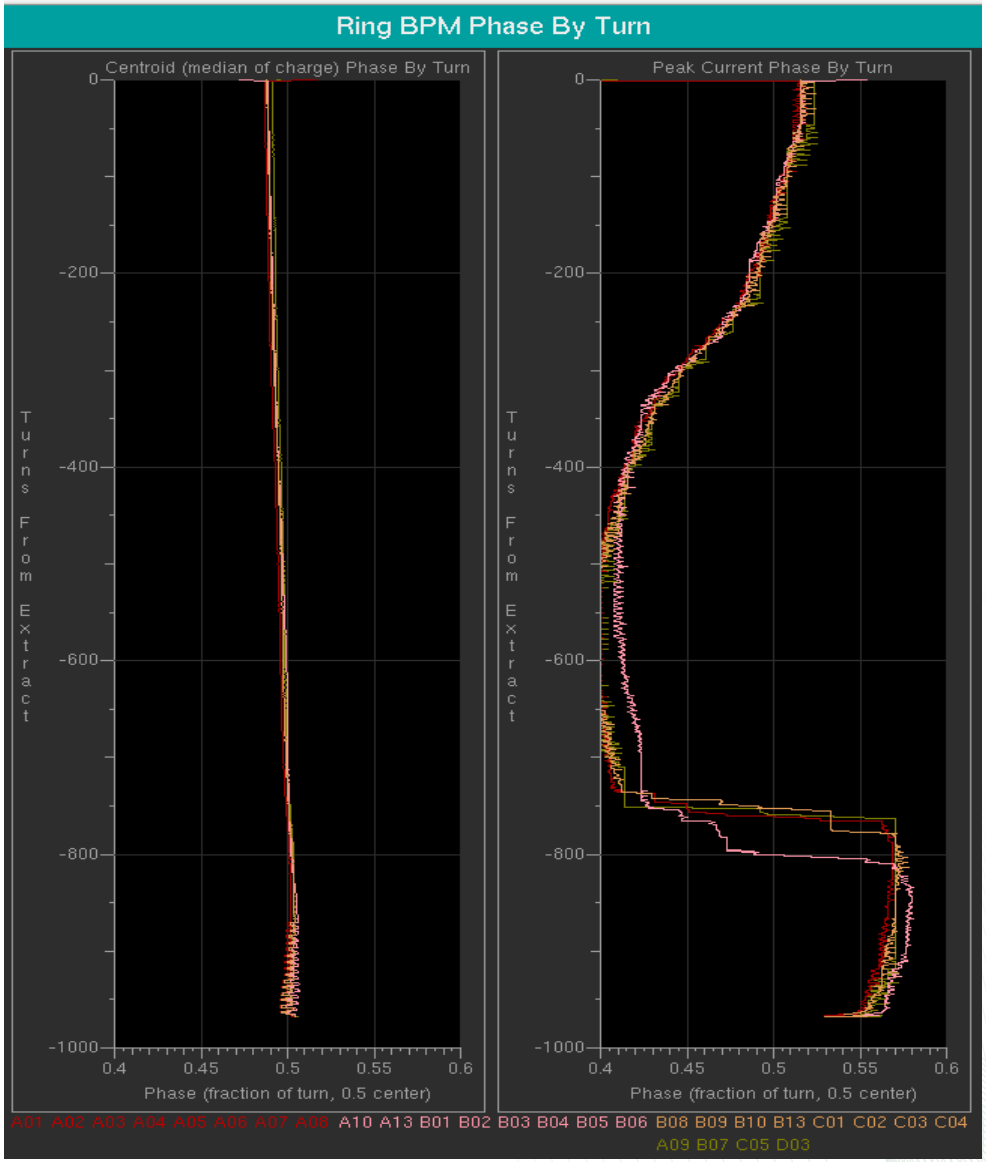
$$O1t = t*M(t) - (t-1)*M(t-1)$$



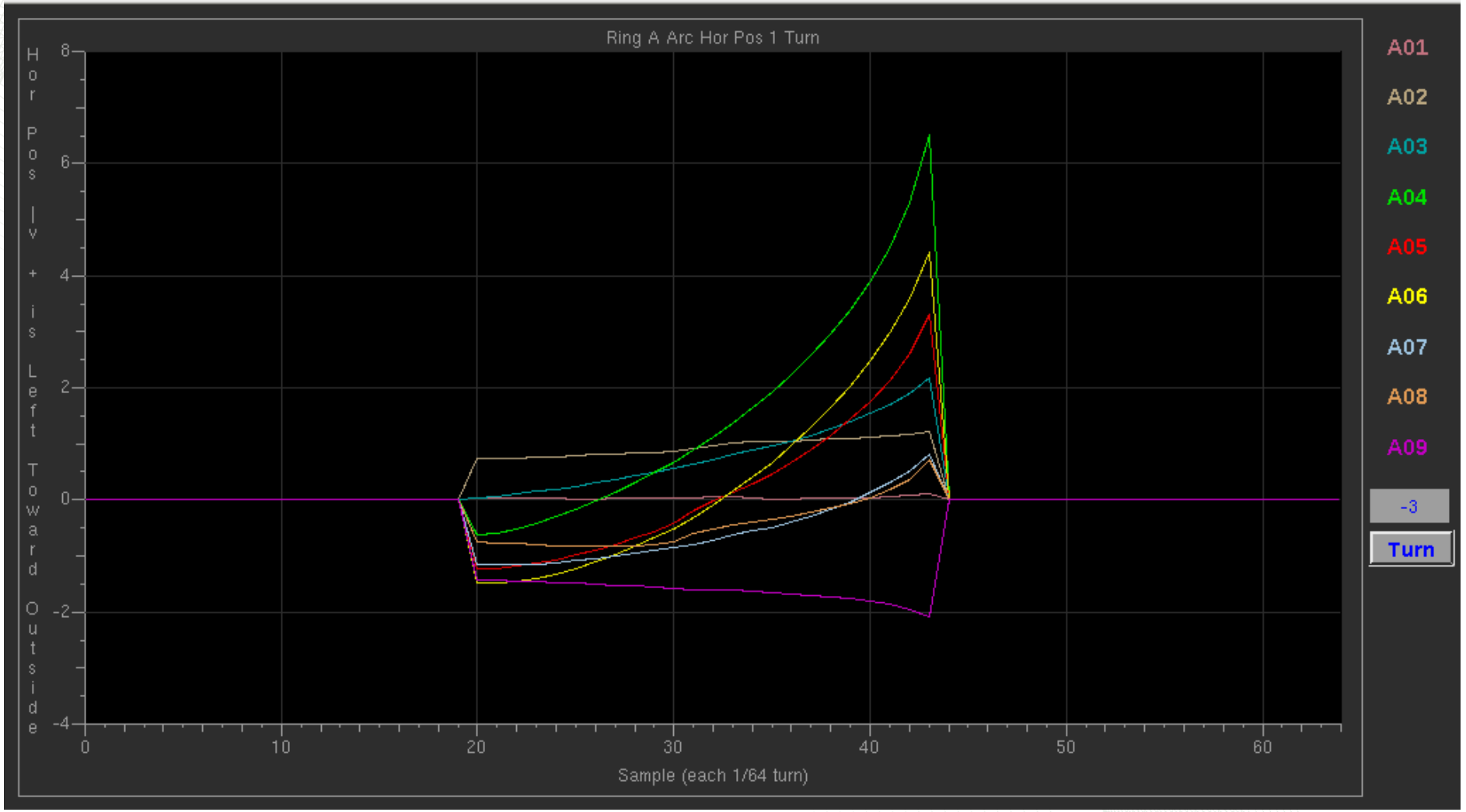




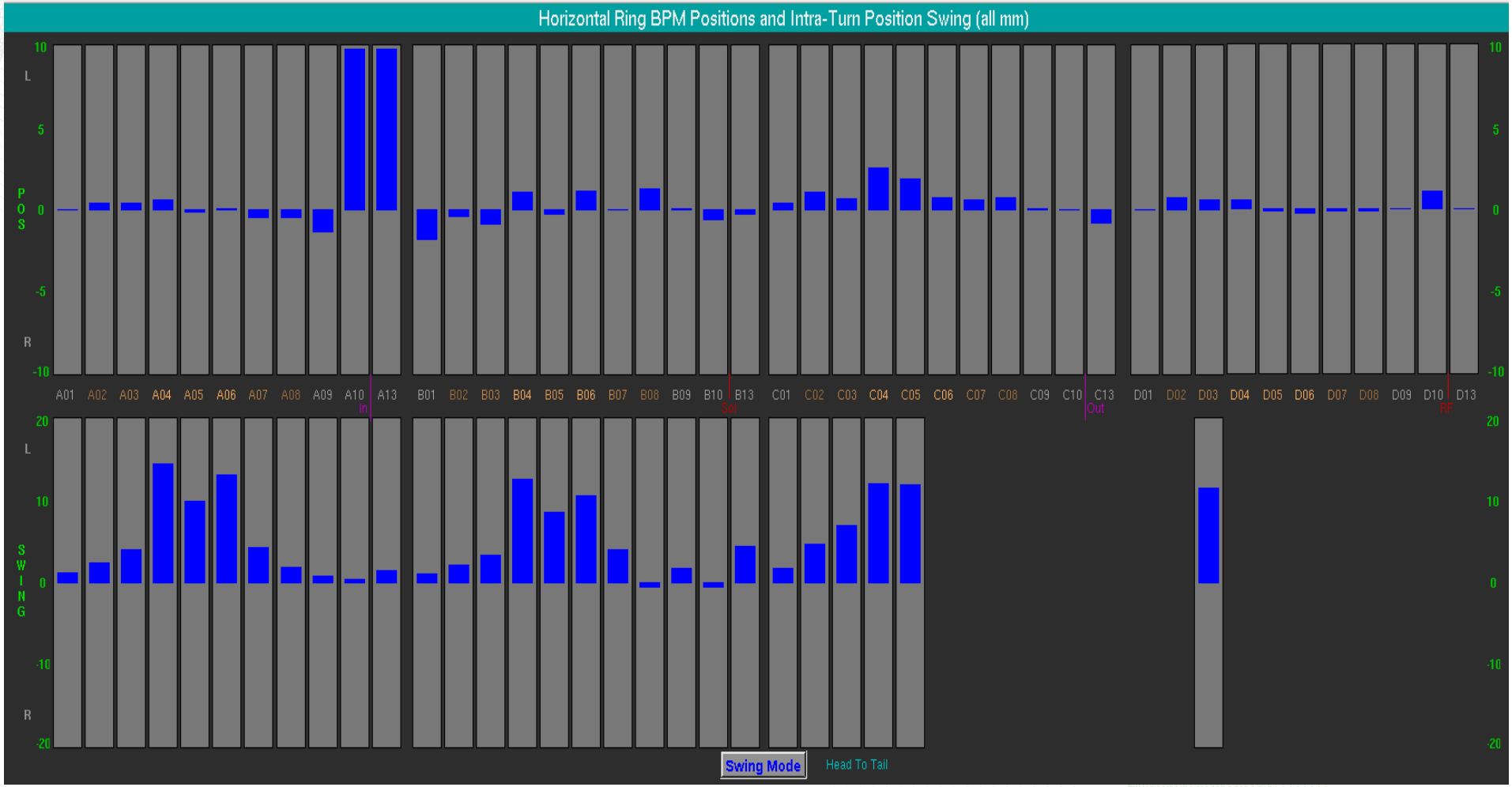
Centroid Phase



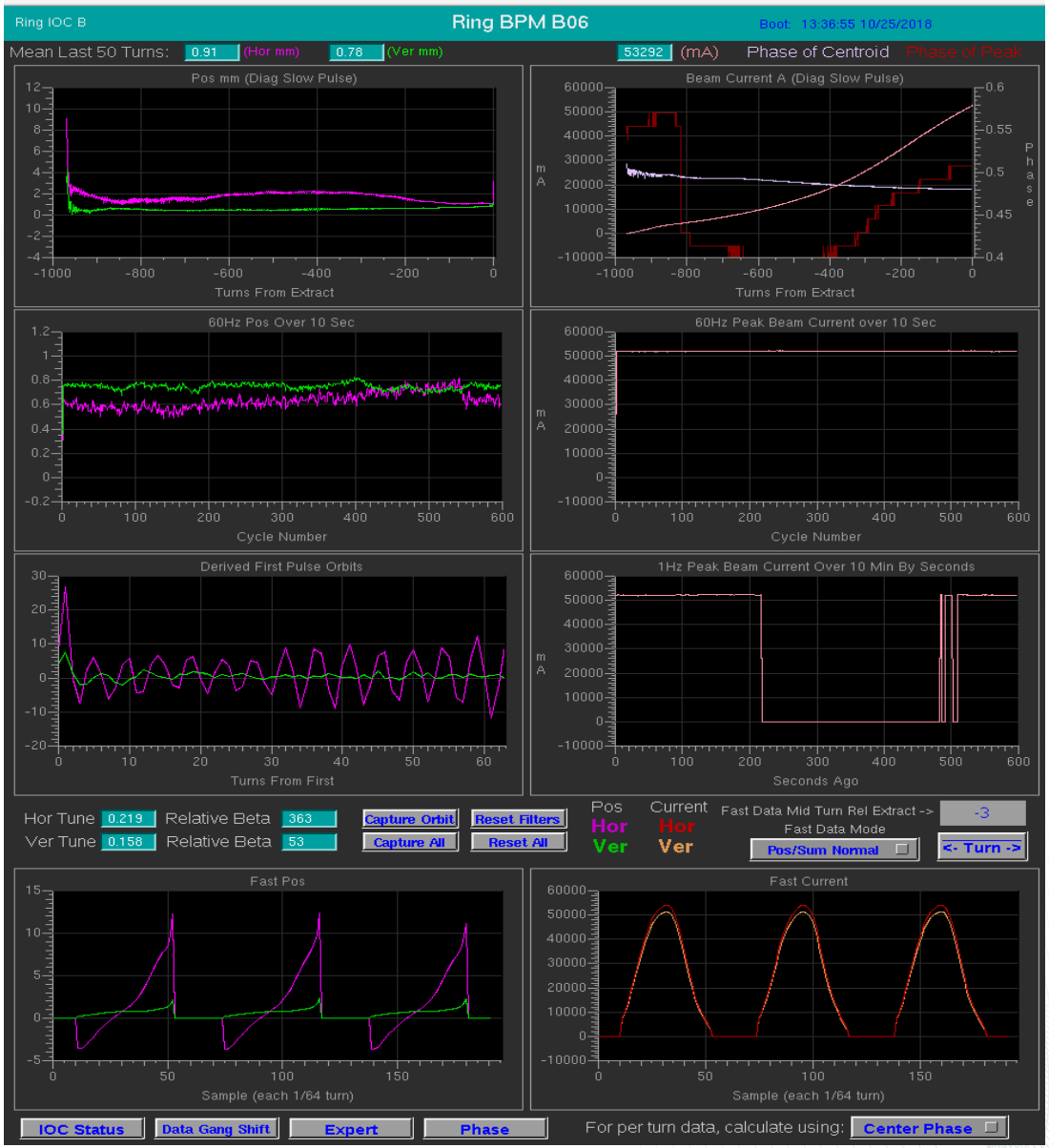
Single Turn Position



Position and Swing Bars



Combined Screen



SNS Ring BPM Old and New

Questions?

System development thank you to:

- Alexander Aleksandrov
- Taylor Davidson
- Alysse Dawson
- Anthony Webster

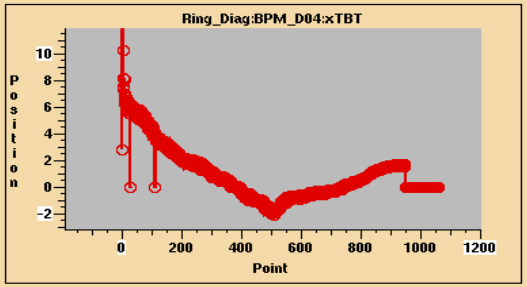
The following slides are not part of this presentation.
They are included only in anticipation of being
needed to answer questions.

./BPMRing.edl (on ics-srv-accl2)

Diagnostics | Ring_Diag:BPM_D04 | Novice | Operator Mode | Timing

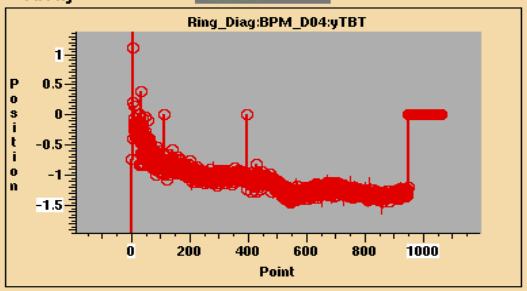
Horizontal Position

Array 0.46



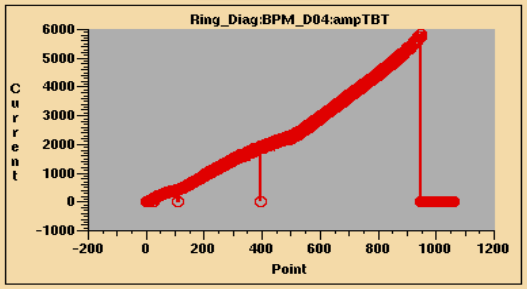
Vertical Position

Array -1.14



Beam I(mA)

Array 2551.8



Stage No.	No of Turns Enter	No of Turns Readback	Channel Gain Setting
1	0	25	30 dB
2	0	85	20 dB
3	0	284	10 dB
4	0	554	0 dB

Stage 1

Stage 1

Base Band -10 dB
Base Band 0 dB
Base Band 10 dB
Base Band 20 dB
Base Band 30 dB
Base Band 40 dB
Base Band 50 dB
Base Band 60 dB
RF 0 dB
RF 10 dB
RF 20 dB
RF 30 dB

Analysis

Turns			Turns		
1	0	948 RMS	5	0	0 RMS
2	0	0 RMS	6	0	0 RMS
3	0	0 RMS	7	0	0 RMS
4	0	0 RMS	8	0	0 RMS

Turn 1

Turns 1 | RMS | Peak | Integration | Zero

Trigger Delay

0.00 170.00e-0

First Turn Delay

0.00 0.00e+00

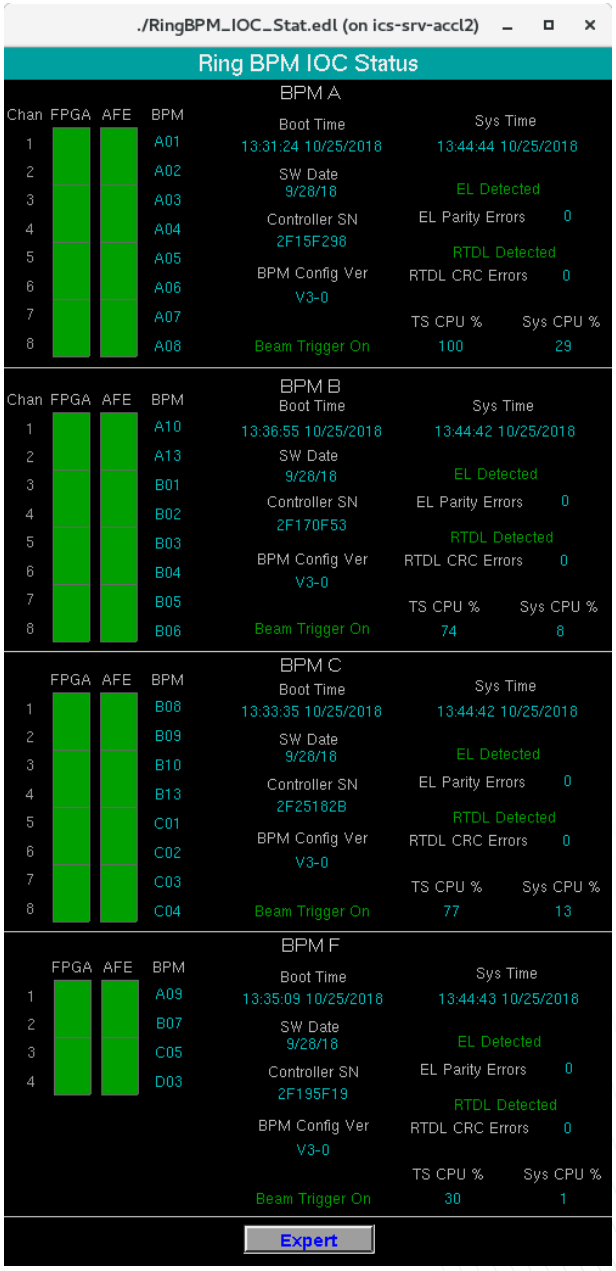
Ring Clock Setting

Ring Frequency 1.059660 Beta 0.876392

Direct

Ring Frequency 1.00e+00

Beta 0.85




1000
800
600
400
200
0
-200
-400
-600
-800
-1000
Amplitude
7000
7050
7100
7150
7200
7250
7300
7350
7400
7450
7500
7550
7600
Time
30
25
20
15
10
5
0
-5
-10
-15
-20
-25
-30
Amplitude
7000
7050
7100
7150
7200
7250
7300
7350
7400
7450
7500
7550
7600
Time