A next generation digital BPM system for the LHC

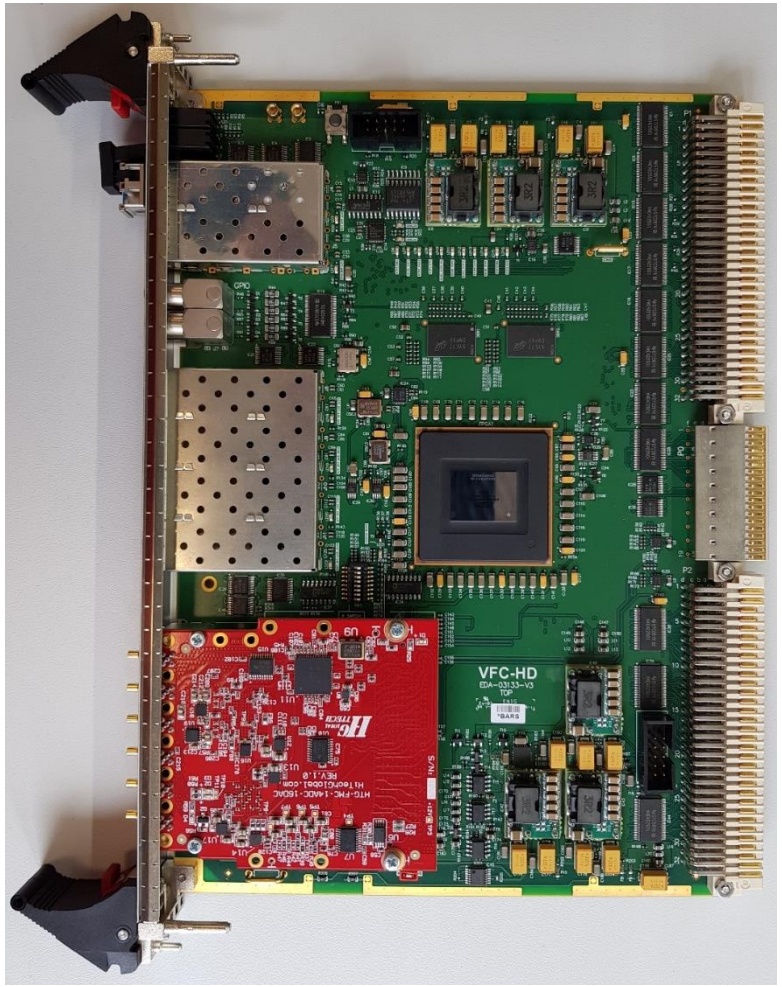
Considerations about a system to be..

Outline

- The LHC BPM-Interlock system's DAQ: a testbed
- Challenges in scaling the BPM-Interlock system to the full LHC
- Possible routes

LHC BPM Interlock system's DAQ

- Comb filter (see Manfred's presentation)
- Gsps ADC



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- With the due caviat….

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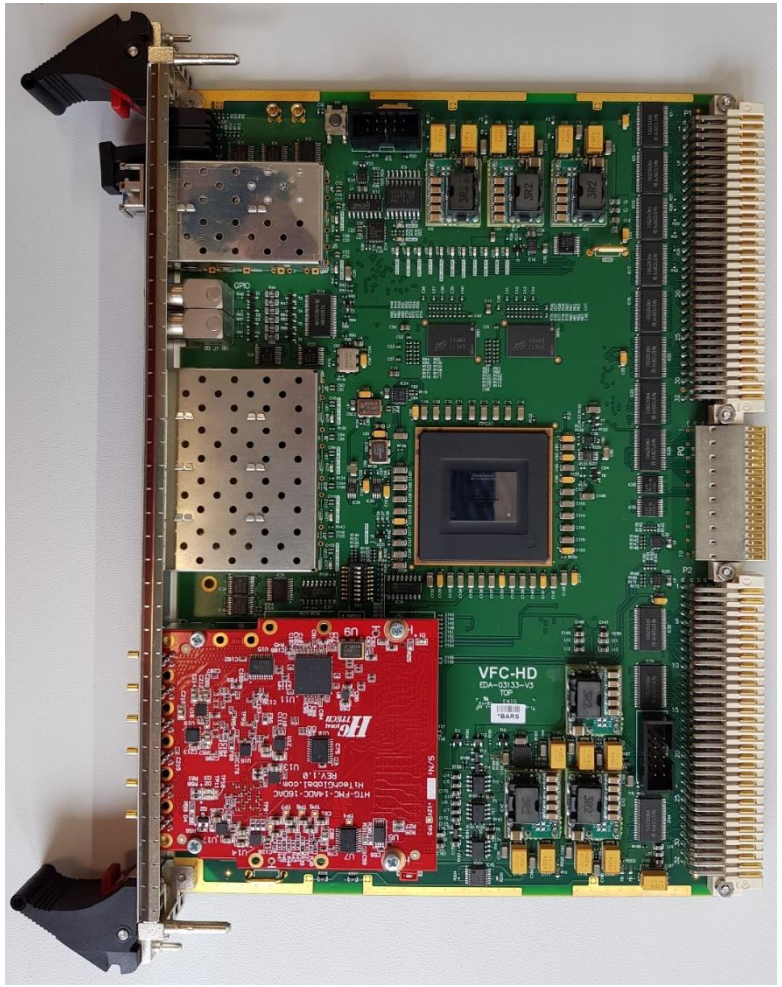

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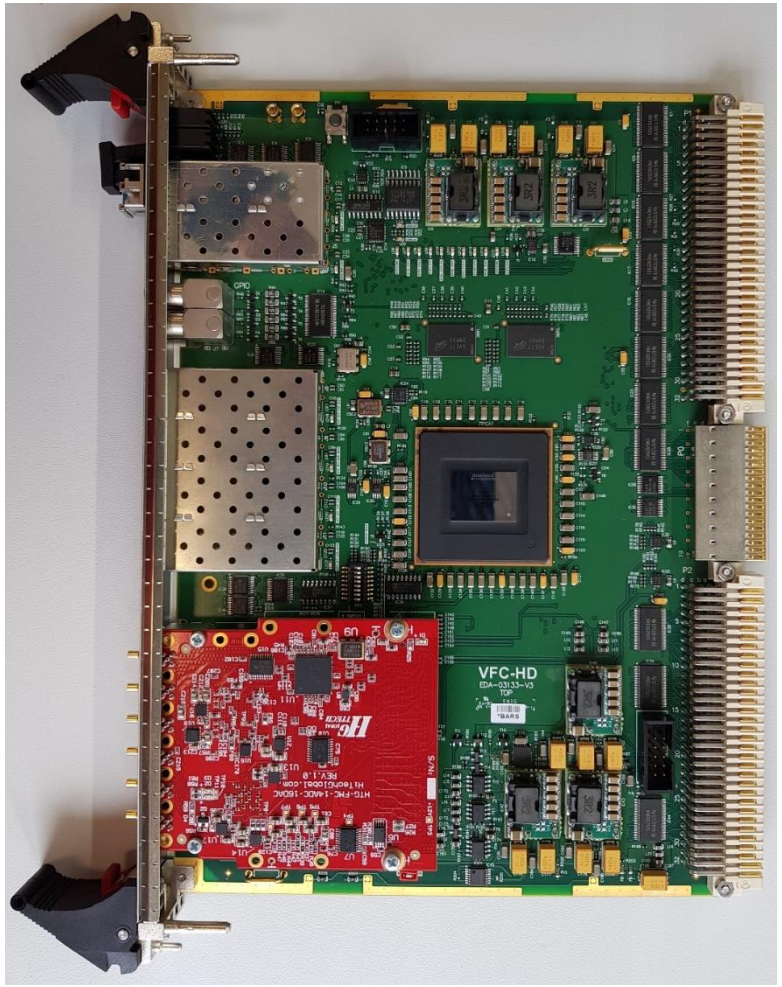
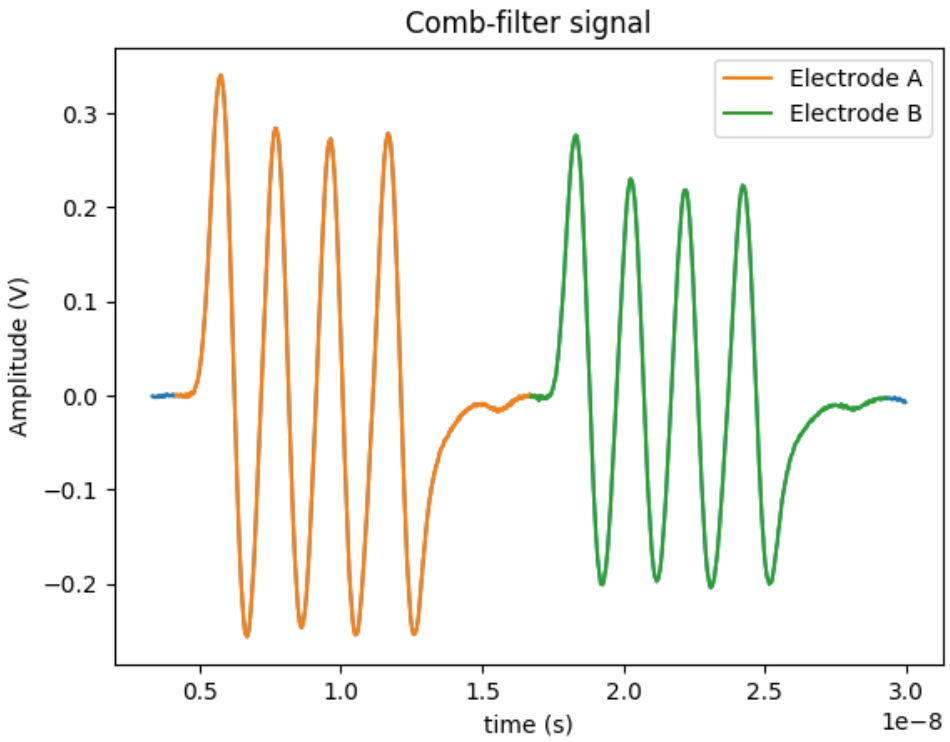
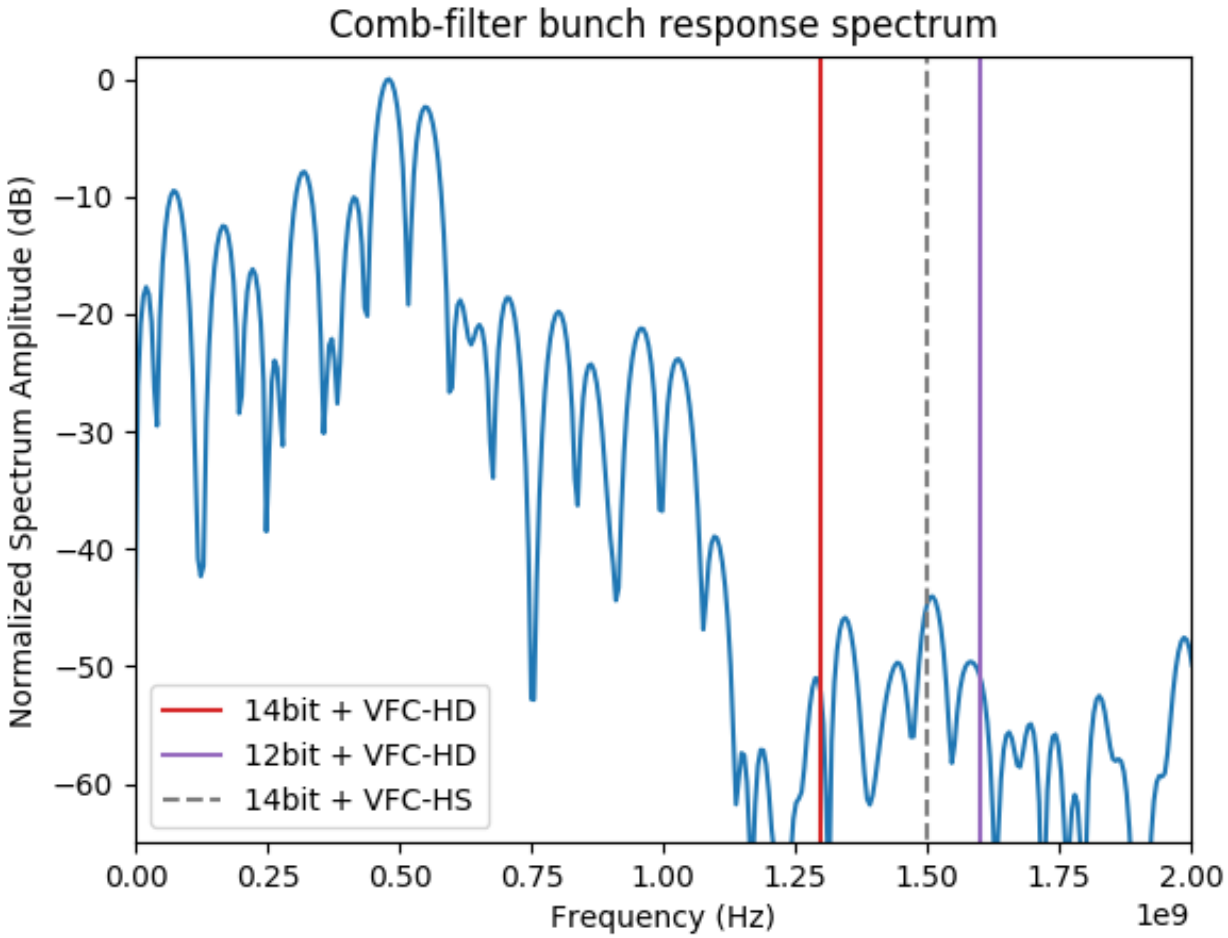
$$LaneRate \propto ENOBS * Fs$$



The actual signals



LHC P5, USC55, BPMSY4L5 (Stripline)
1.24e11 Bunch Intensity
Acquired with 8 bit – 18 GHz scope



Beam Results : position estimation algorithm

Electrode signal power estimation and Delta/Sigma normalization to extract the displacement x:

$$x = k\,\frac{A - B}{A + B}$$

$$\mathrm{A} = c * I * (1 + a * x)$$

$$\mathrm{B} = c * I * (1 - a * x)$$

Beam Results : position estimation algorithm

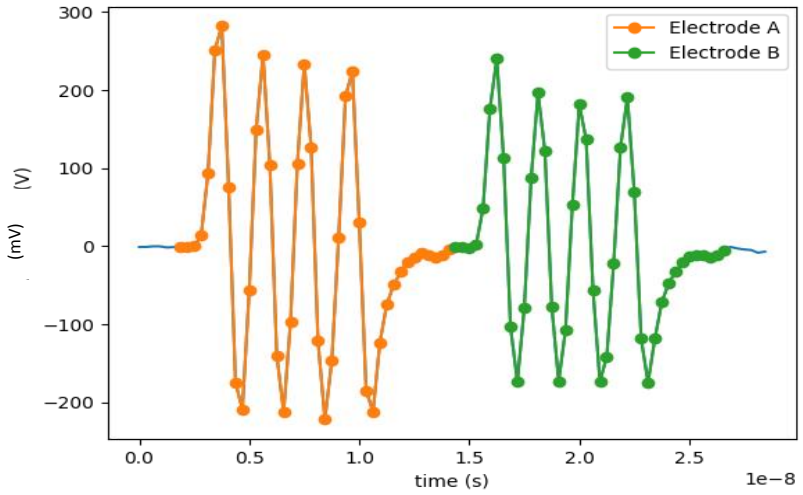
- A and B estimated from the signal power
- Signal power estimation by **Root Mean Square** (RMS) algorithm

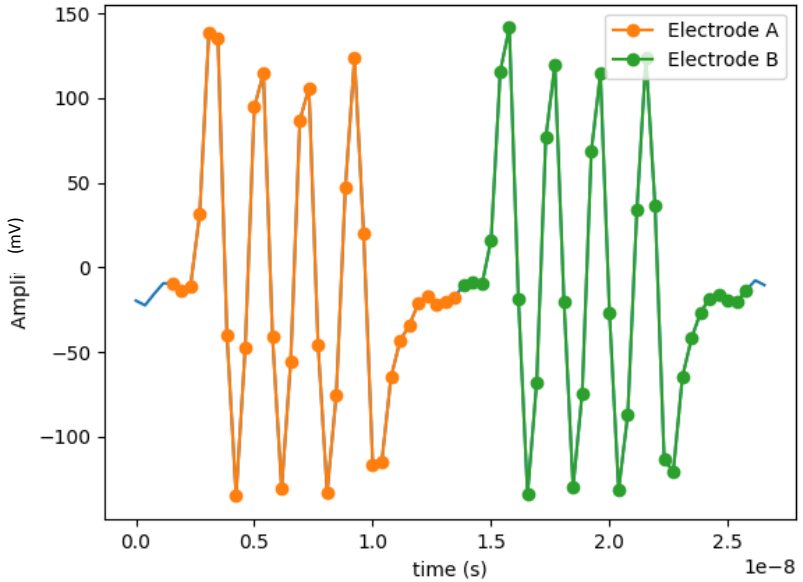
$$A = g * \sqrt{\sum S_i^2}$$

$$\frac{A^2 - B^2}{A^2 + B^2} = \frac{2 * a * x}{(1 + a^2 * x^2)}$$

We can think of using a very simplified trigger condition: $|A^2 - B^2| < T_h * (A^2 + B^2)$

The tested mezzanines (ADCs)

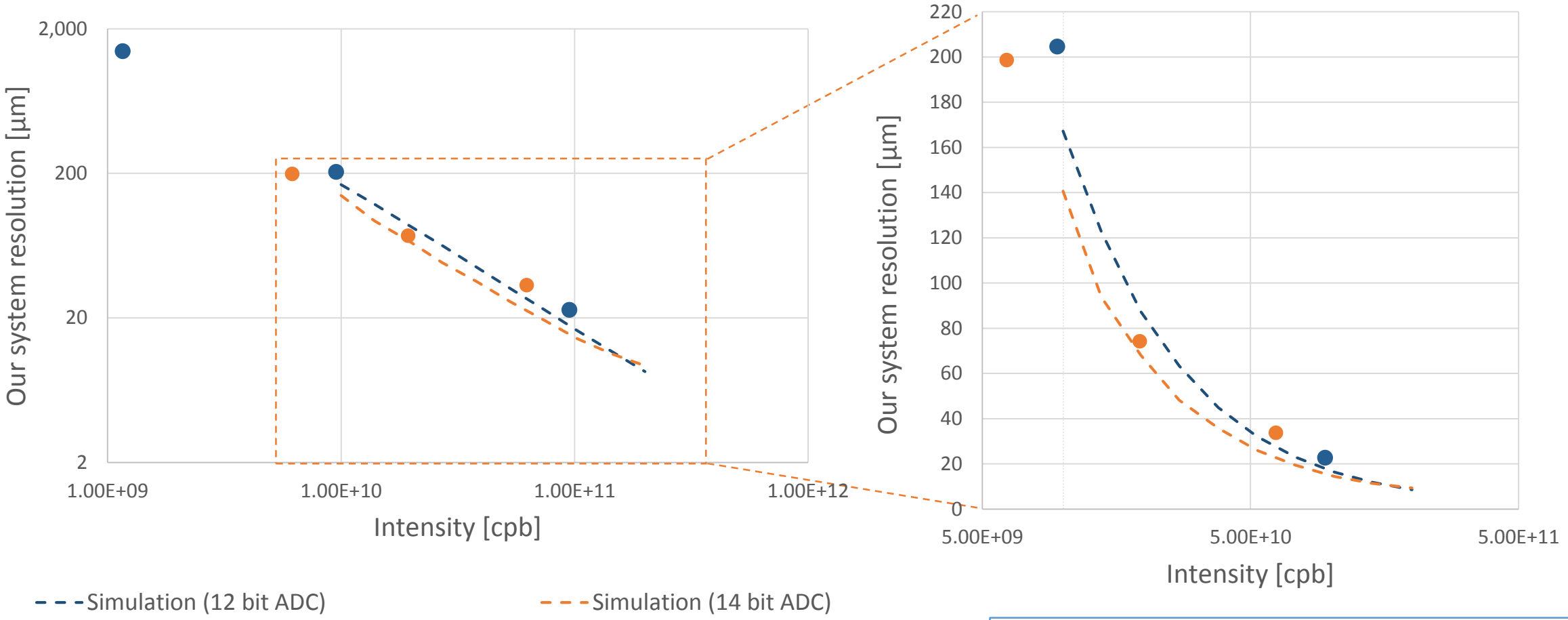




- Vadatech FMC (ADC12J4000)
  - 12 bits(8.8ENOBs)
  - 4.0 Gsps
- Resolution for 1E10 protons:
  - Obtained @3.2Gsps : 200um
  - Ultimate @4.0Gsps : 180um

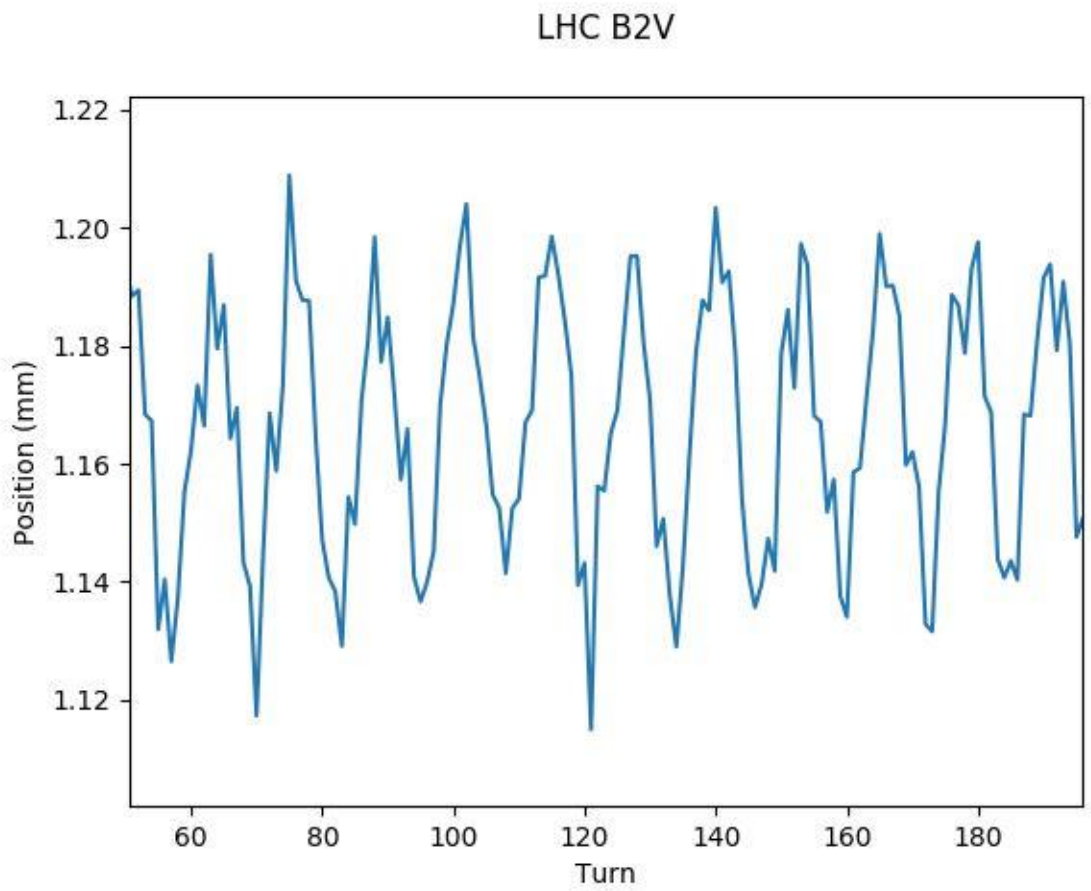
- HTG FMC (AD9208)
  - 14 bits(9.6ENOBs)
  - 3.0 Gsps
- Resolution for 1E10 protons:
  - Obtained @2.6Gsps : 130um
  - Ultimate @3.0Gsps : 120um

Measurements Vs Simulation



Intensity is scaled in order to cover the full ADC range with maximum intensity (2e11) and displacement (± 7.5 mm).

Synchronous Vs Asynchronous



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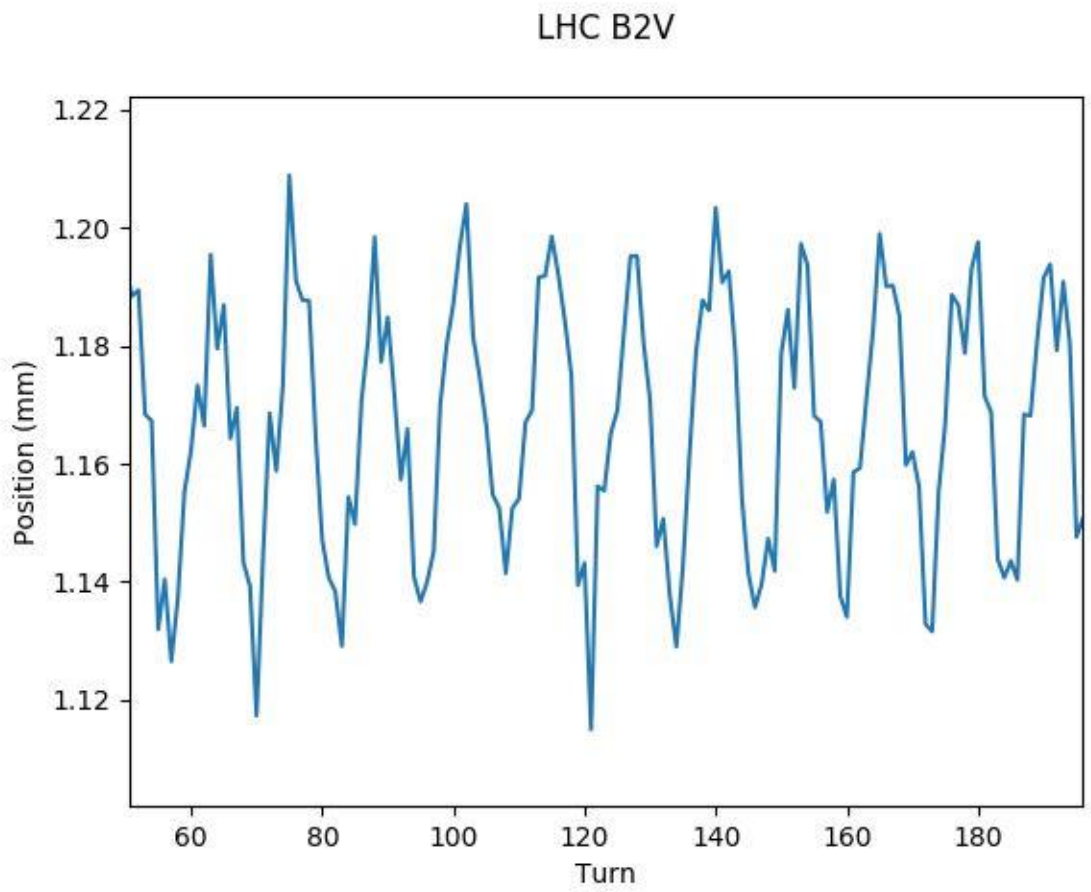
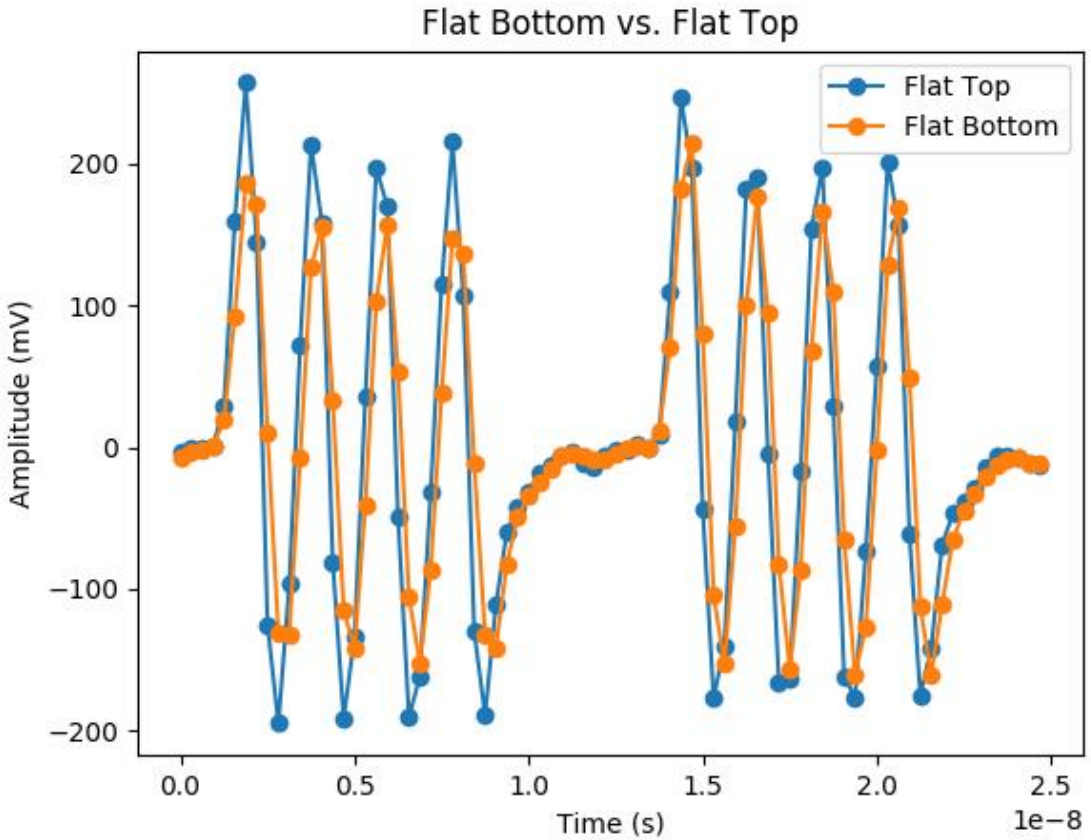




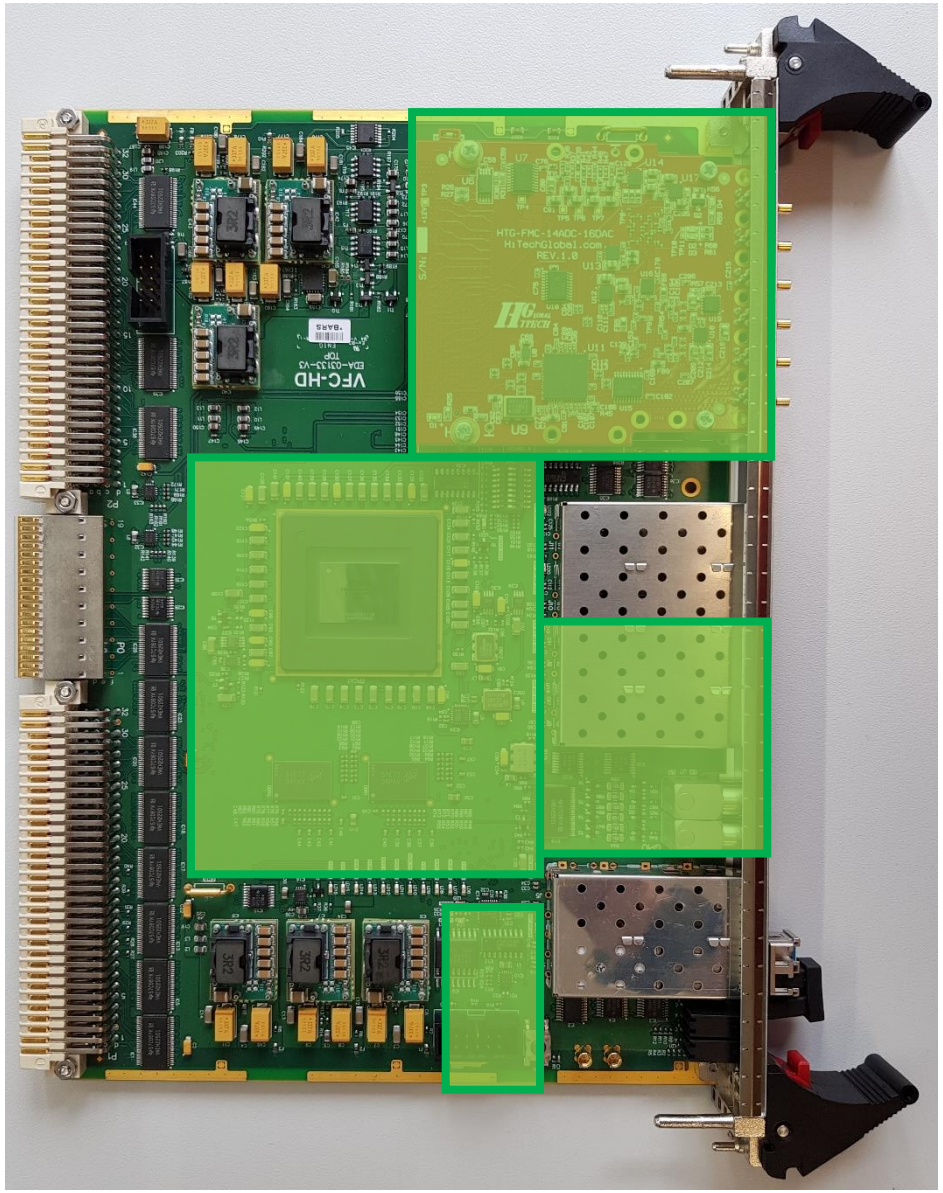
Scaling the BPM-Interlock system to HL-LHC

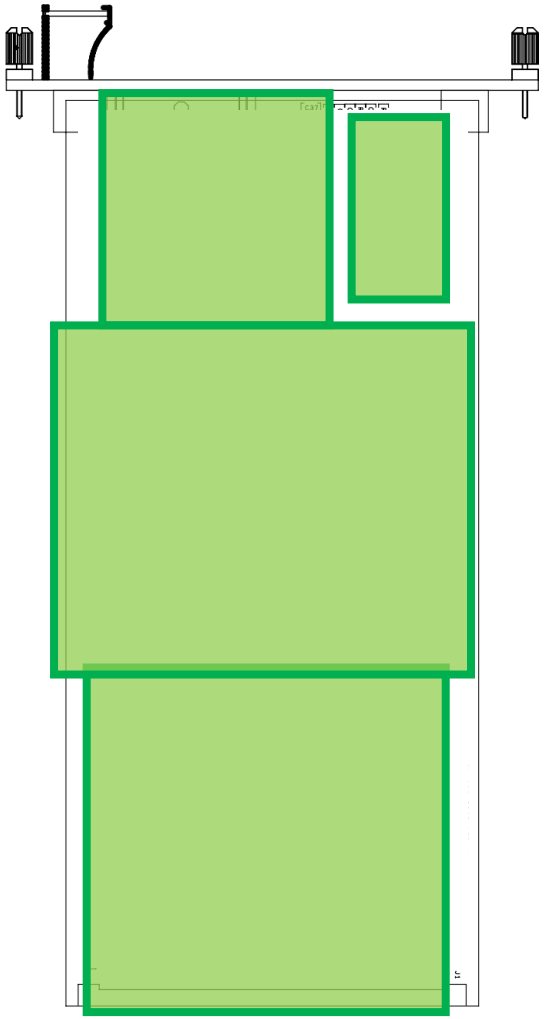
- Cost
- Real estate
- Radiation tolerance

Scaling the BPM-Interlock system to HL-LHC

- Cost - @5k per plane: 10*10k => 1000*10k
- Real estate
- Radiation tolerance

Scaling the BPM-Interlock system to HL-LHC





Scaling the BPM-Interlock system to HL-LHC

- SEL
- TID
  - Failure level
  - Speed of components…
- SEU
  - Dataflow
  - PLLs
  - Filters and acquisition parameters
  - Configuration memory

Rad tol ADC example

ADC12D1620QML-SP 12-Bit, Single Or Dual, 3200- or 1600-MSPS RF Sampling Analog-to-Digital Converter (ADC)

1 Features

- Total Ionizing Dose (TID) to 300 krad(Si)
- Single Event Functional Interrupt (SEFI) Tested
- Single Event Latch-up (SEL) > 120 MeV-cm^2/mg
- Cold Sparing Capable
- Wide Temperature Range –55°C to +125°C
- Power Consumption = 3.8 W or 2.7 W (1600- or 800-MHz Clock)
- 3-dB Input Bandwidth = 3 GHz
- Low-Sampling Power-Saving Mode (LSPSM) Reduces Power Consumption and Improves Performance for $f_{CLK} \leq 800$ MHz
- Auto-Sync Function for Multi-Chip Systems
- Time Stamp Feature to Capture External Trigger
- Test Patterns at Output for System Debug
- 1:1 Non-Demuxed or 1:2 or 1:4 Parallel Demuxed LVDS Outputs
- Single 1.9-V Power Supply

3 Description

The ADC12D1620QML device uses a package redesign to achieve better ENOB, SNR, and X-talk compared to the ADC12D1600QML. As is its predecessor, the ADC12D1620QML is a low-power, high-performance CMOS analog-to-digital converter (ADC) that digitizes signals at a 12-bit resolution at sampling rates up to 3.2 GSPS in an interleaved mode. It can also be used as a dual-channel ADC for sampling rates up to 1.6 GSPS. For sampling rates below 800 MHz, there is a low-sampling power-saving mode (LSPSM) that reduces power consumption to less than 1.4 W per channel (typical). The ADC can support conversion rates as low as 200 MSPS.

Device Information(1)

PART NUMBER	GRADE	PACKAGE
ADC12D1620CCMLS	Flight 300 krad	CCGA (376)
ADC12D1620CCMPR	Pre-flight engineering prototype	CCGA (376)
ADC10D1000DAISY	Daisy chain, mechanical sample, no die	CCGA (376)

SYSTEM CONSIDERATIONS:

- Glue logic and data reduction in FPGA
- I/O speed of interfacing logic > ¼ Fs
- Data transmission :
  - FPGA transceivers
  - LpGBT

FPGA under study

- New effort from EU to fabricate an RadHard ITAR-free FPGA
- NanoXplore leading the effort with NG-MEDIUM (NX1H25S) as the first FPGA to come out.
- STM C65 (65nm RadHard ST process)
- Rad Hard Configuration memory (CRAM) cells and Flip Flops
- CRAM Integrity Check (CMIC)
- NX1H25S specifications:
  - 56×48kbit RAM blocks (BRAM)(ECC available)
  - 34272 LUT – 4
  - 32256 Registers (Flip Flops)
  - 8064 Carry modules
  - 112 Digital Signal Processor (DSP)
  - 24 Clocks (4 PLLs)
  - 13 I/O Banks
- Python based software
- Synthesis, place and route in house developed

NanoXplore NG medium

Conclusions and future Steps

Courtesy of Georgios Tsiligiannis

- Up to 3kGy cumulative dose -> **no degradation**
- Results showed that this FPGA has a robust behavior
- Purchase of a significant lot of devices foreseen for the next year. The requests are collected by EN-SMM-RME (contact Salvatore.Danzeca@cern.ch)
- Training from NanoXplore to be scheduled between December and January!!!
- We need your feedback!

- Searching collaboration with the equipment groups to implement an application that will be tested at PSI

Hope from Xilinx…

Family Comparisons

Table 1: **Device Resources**

	Kintex UltraScale FPGA	Kintex UltraScale+ FPGA	Virtex UltraScale FPGA	Virtex UltraScale+ FPGA	Zynq UltraScale+ MPSoC	Zynq UltraScale+ RFSoC
MPSoC Processing System					✓	✓
RF-ADC/DAC						✓
SD-FEC						✓
System Logic Cells (K)	318–1,451	356–1,143	783–5,541	862–3,780	103–1,143	678–930
Block Memory (Mb)	12.7–75.9	12.7–34.6	44.3–132.9	23.6–94.5	4.5–34.6	27.8–38.0
UltraRAM (Mb)		0–36		90–360	0–36	13.5–22.5
HBM DRAM (GB)				0–8		
DSP (Slices)	768–5,520	1,368–3,528	600–2,880	2,280–12,288	240–3,528	3,145–4,272
DSP Performance (GMAC/s)	8,180	6,287	4,268	21,897	6,287	7,613
Transceivers	12–64	16–76	36–120	32–128	0–72	8–16
Max. Transceiver Speed (Gb/s)	16.3	32.75	30.5	58.0	32.75	32.75
Max. Serial Bandwidth (full duplex) (Gb/s)	2,086	3,268	5,616	8,384	3,268	1,048
Memory Interface Performance (Mb/s)	2,400	2,666	2,400	2,666	2,666	2,666
I/O Pins	312–832	280–668	338–1,456	208–832	82–668	280–408

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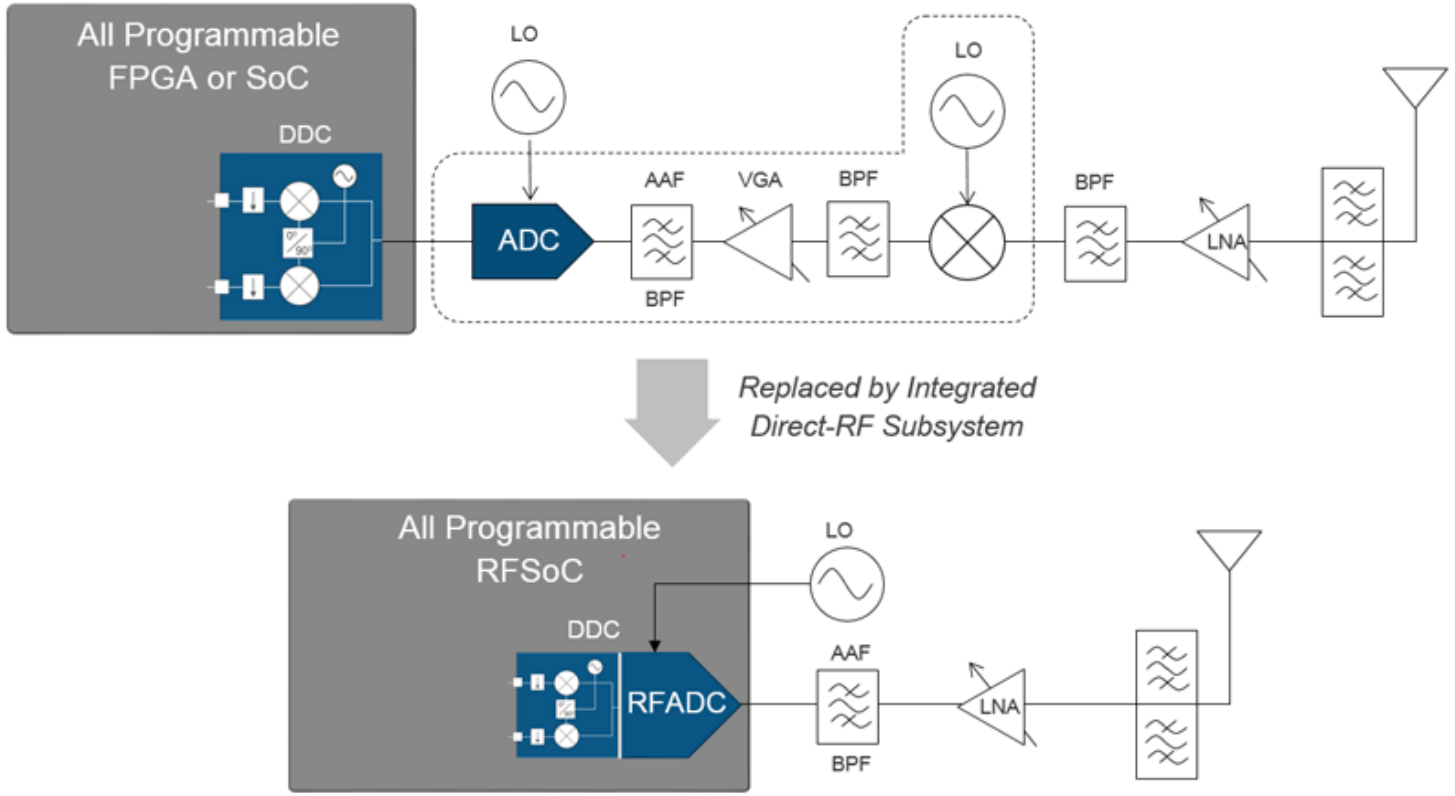

Special thanks to the absents…

- Jan Pospisil : fellow in BI
- Irene Degl’Innocenti : doctoral student in BI