Brief Introduction to the Digital BPM development for HEPS project

ShuJun-Wei, Qiang-Ye, YanFeng-Sui, HuiZhou-Ma, YaoYao-Du, Yufei-Ma, XingEr-Zhang, XiYang-Huang, YanHua-Lu, Jing-Yang, JunHui-Yue, JianShe-Cao

IHEP Beam Instrumentation Group

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Outline

1. Why we need to build the digital BPM electronics
2. The BPM requirement of HEPS project
3. Digital BPM electronics design for HEPS project
4. Digital BPM pre-research in HEPS-TF project
5. Temperature influence discussion
6. Summary and Acknowledgement

1. Why we need to build the digital BPM electronics

1，Beam orbit stability is key parameter of modern light sources, it can affect performances of accelerator and synchrotron light beam stations.

2，Beam users always hope beam orbit changes within 5% to 10% of beam size. For HEPS, its typical beam size is 3μm, so we need to control beam orbit stability within 0.3μm, so the resolution of beam position measurement is need to meet the requirement of 0.1μm.

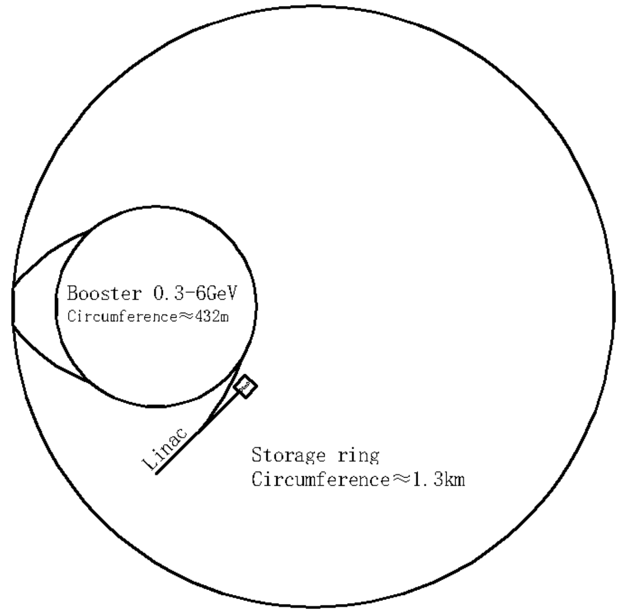
3，Commercial product is good as the beam position measurement, but the price is also “good”, and its original code is not open to users, so further development based on machine requirement and study to them is impossible.

4，Home-made electronics can develop technologies and reduce the cost.

2. The BPM requirement of HEPS project

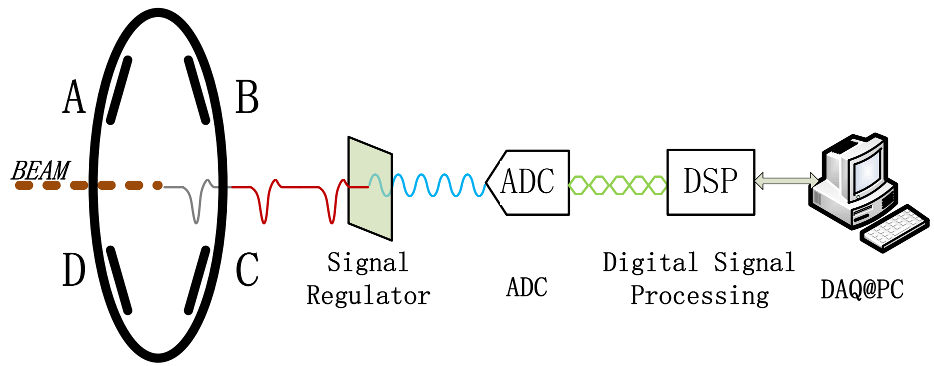
Brief introduction to the HEPS project

- The **High Energy Photon Source (HEPS)** is designed as an ultra-low emittance ring-based synchrotron radiation light ;
- About fourteen beamlines will be constructed in Phase I of the project;
  - Storage ring circumference: 1296m， 48*7BA
  - Energy: 6GeV
  - Emittance: 60pm.rad
  - Current: >200mA



Schematic of HEPS Complex

The Digital BPM requirement of HEPS project



■ HEPS BPM quantities

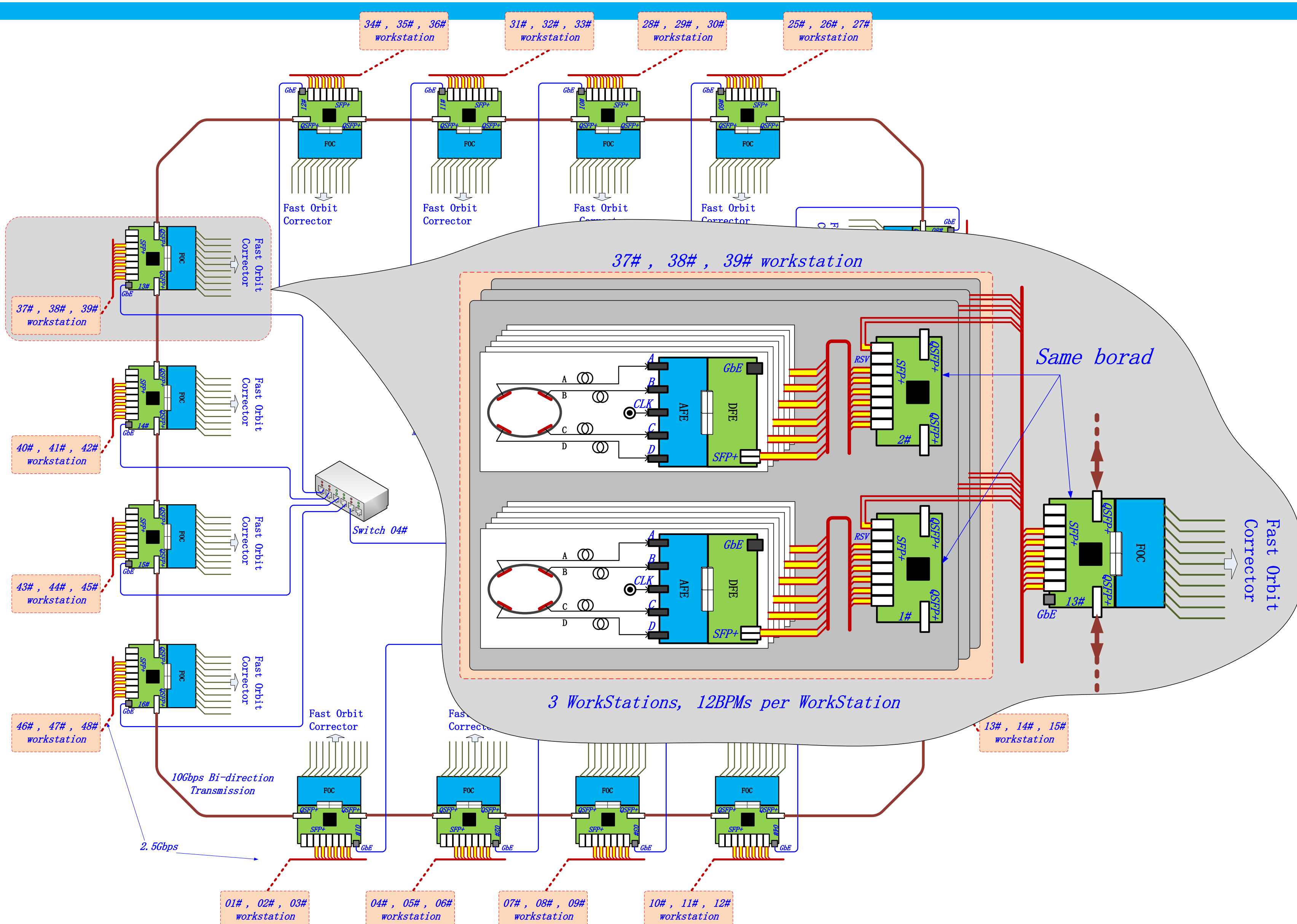
	BPM Quantities
Linac	7
Transfer Line	3*10=30
Booster	80
Storage Ring	48*12=576
SUM	693

■ Storage ring BPM Parameters

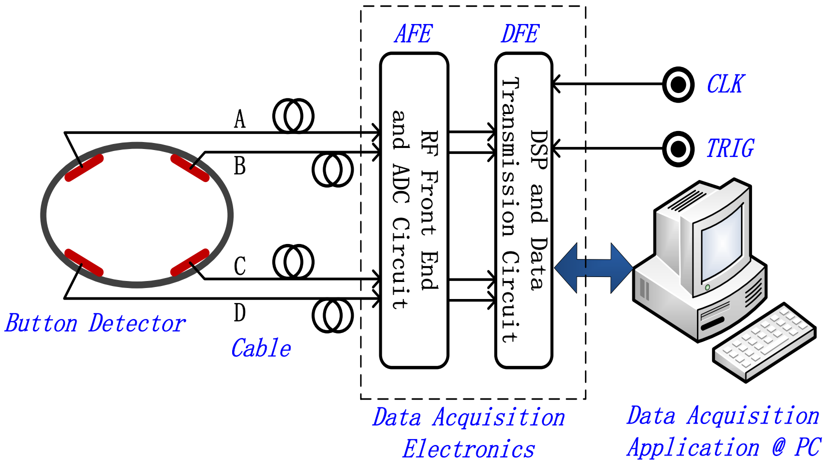
	DBPM@HEPS
Turn by Turn Data	1μm @220kHz
FA data	0.3μm @22KHz
COD data	0.1μm @10Hz

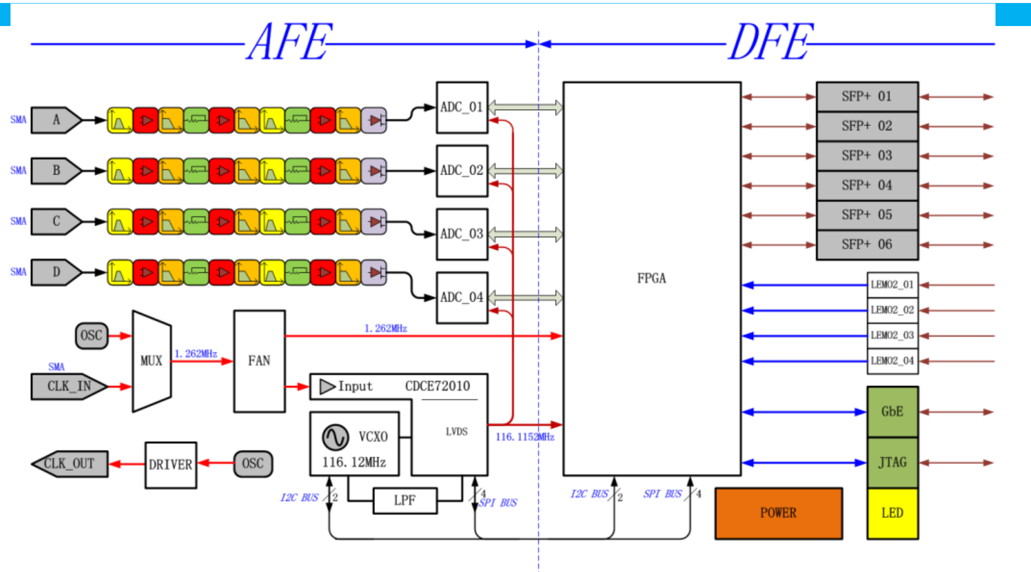
3. Digital BPM electronics design for HEPS project

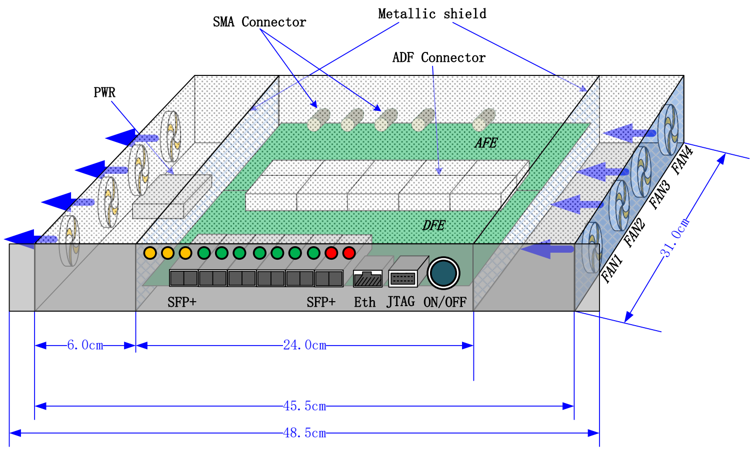
3.1 FOFB Framework and DBPM architecture



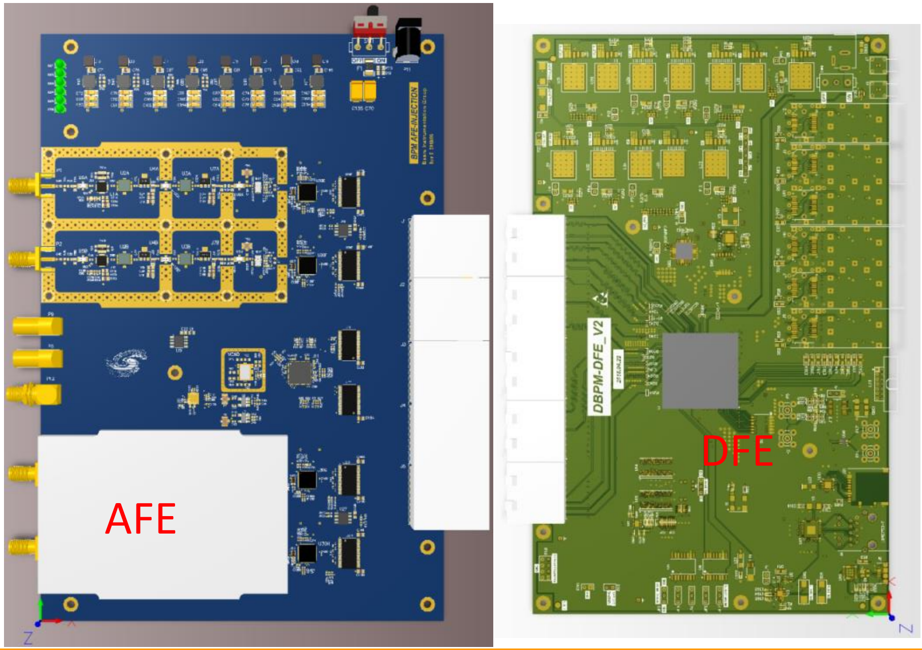
3.2 DBPM Electronics design



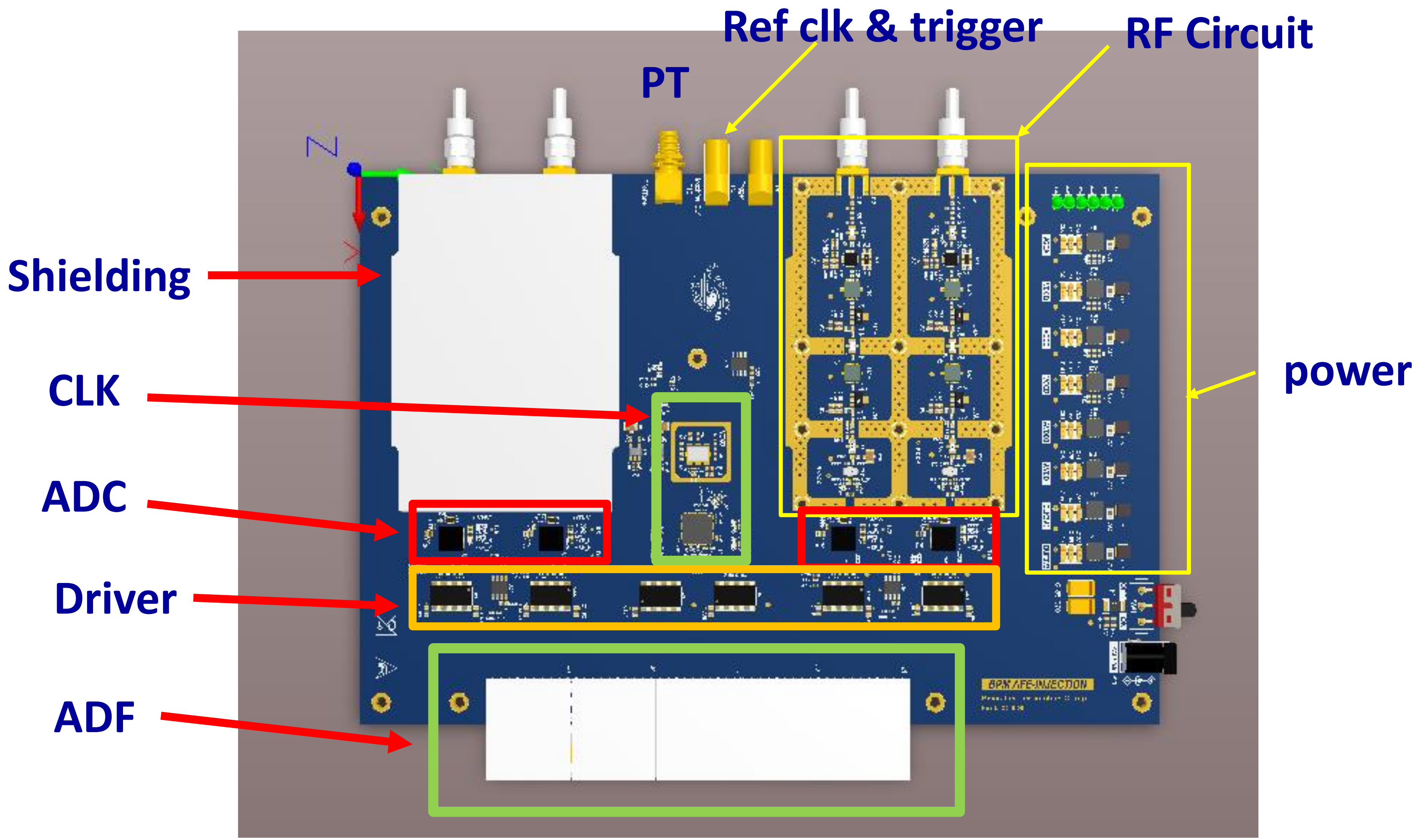




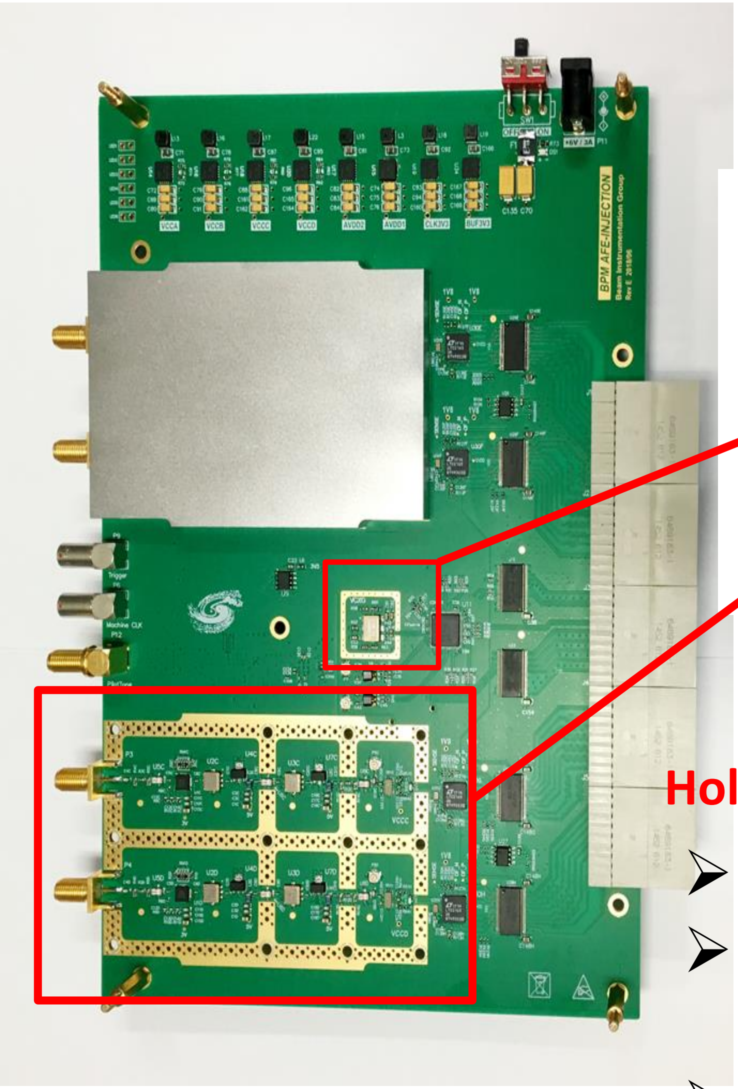
(By HuiZhou Ma)

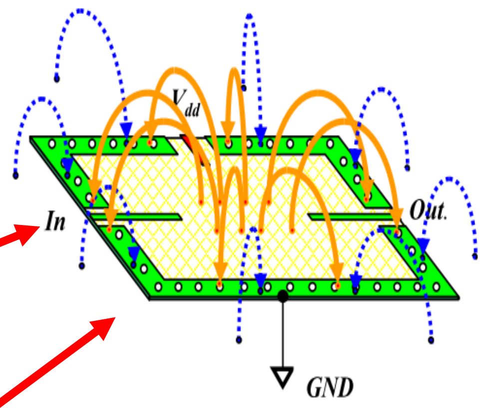


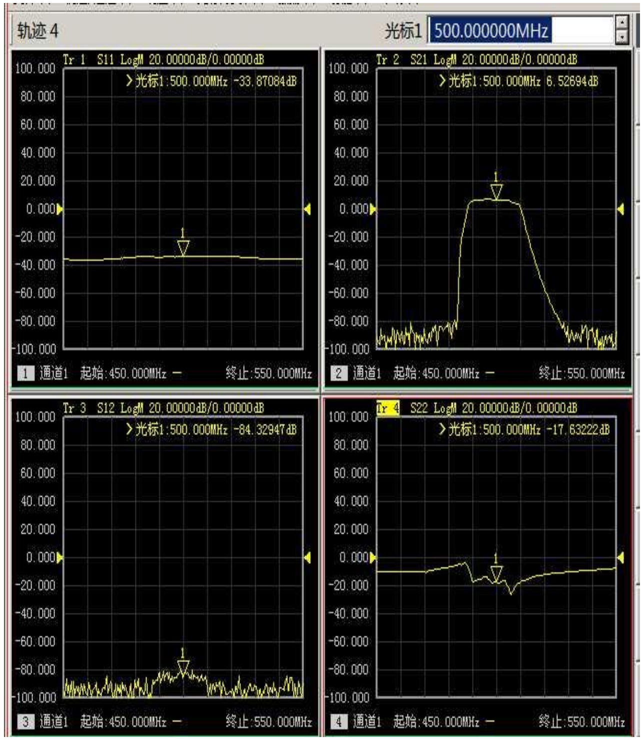
■ AFE electronic



AFE Analog logic Testing



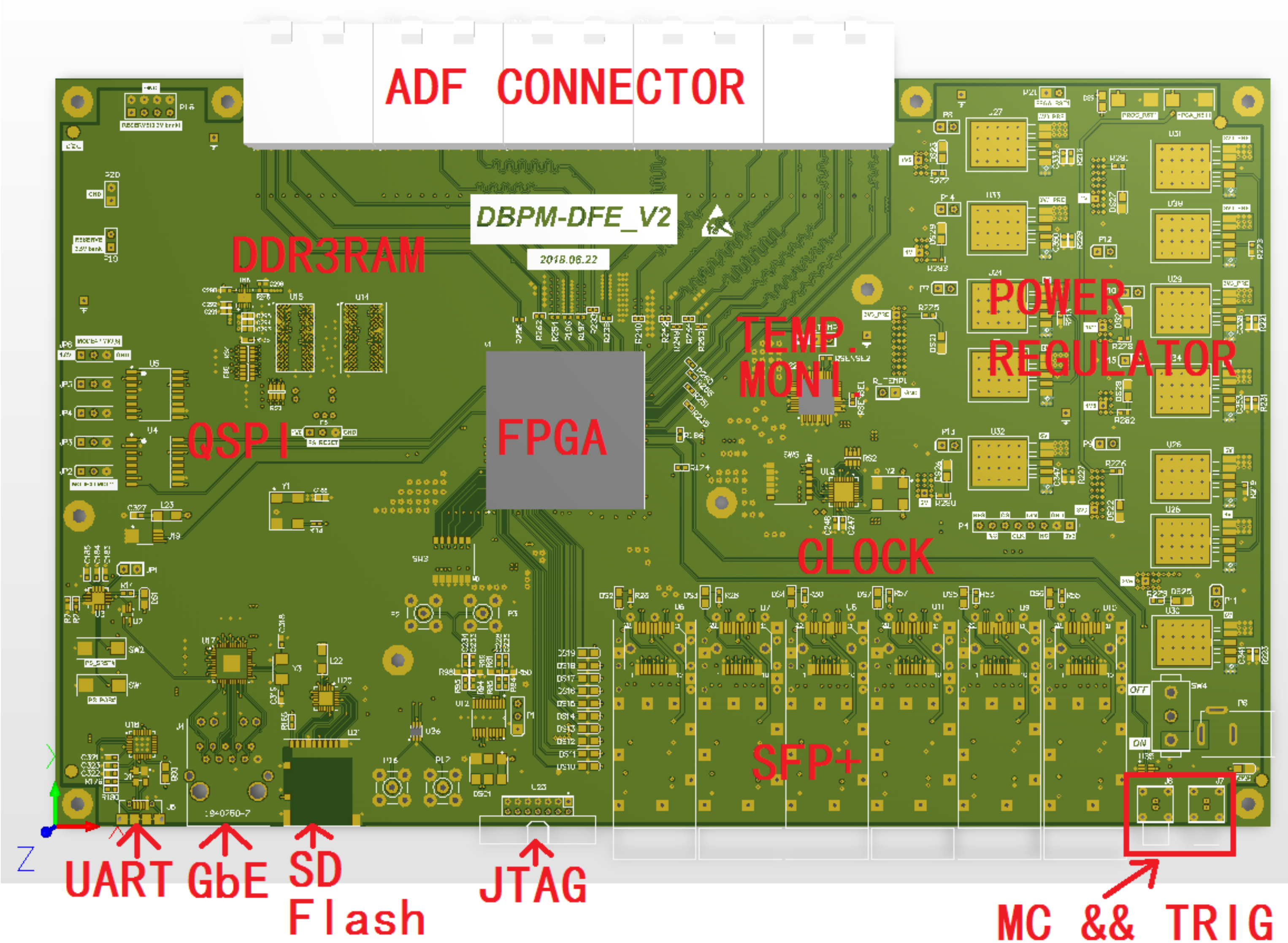




Hole space: *S ≈ 4D to 10D*

- More than 2 rows Ground Via needed;
- Vias on Adjacent rows are interlaced placed;
- Less λ /4 Via to Via space in one row.

■ DFE electronics

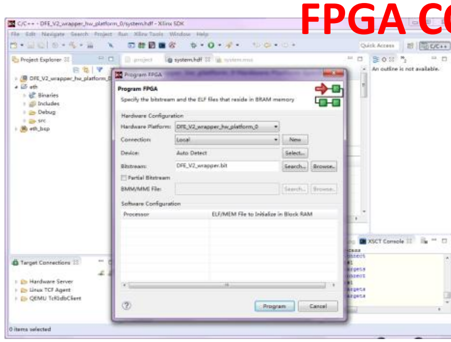


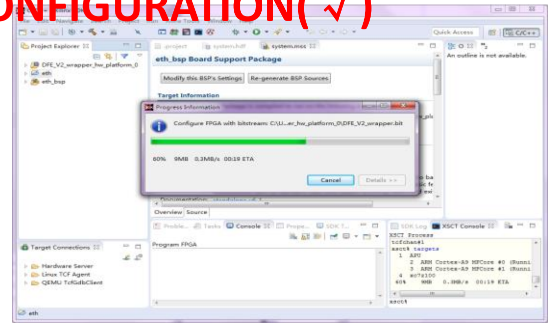
DFE Hardware Testing

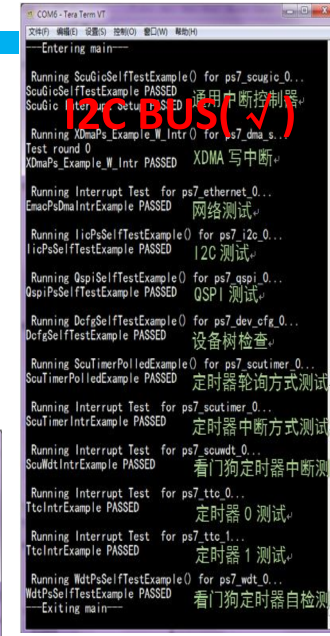
DFE POWER(√)

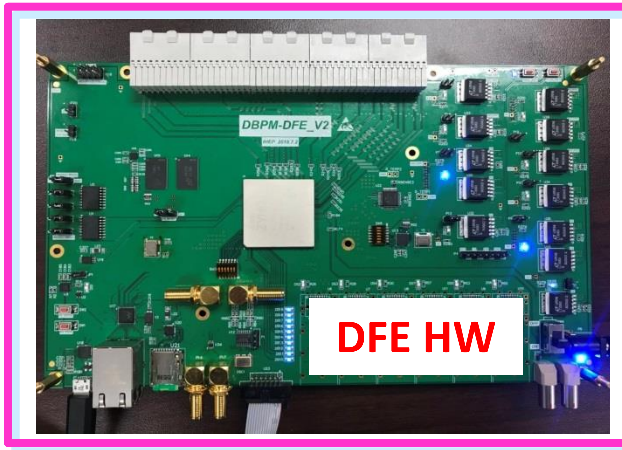
设计电压（V）	实测电压（V）	用电引脚
1	1.006	VCCINT, VCCPINT, VCCBRAM, ETH,
1	1.003	MGTAVCC
1.2	1.213	GTX_MGTAVTT
1.5	1.494	VCCO, DDR3
1.8	1.780	VCCPAUX, VCCPLL, VCCOMIO, VCCAUX, MGTAVCCAUX, UART, SD, I2C
2	1.998	VCCAUX_IO
2.5	2.513	VCCO
3.3	3.315	VCCO, ETH, JTAG, QSPI, POR,
3.3_pre	3.295	1.5V, 1.2V, 1V

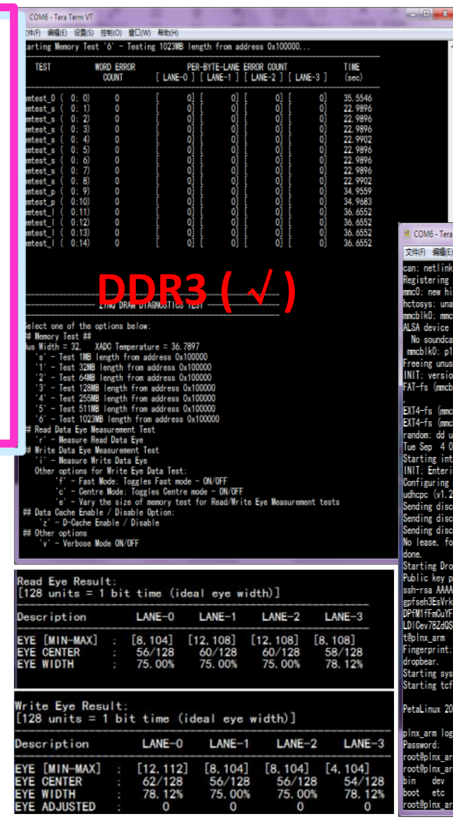
FPGA CONFIGURATION(√)

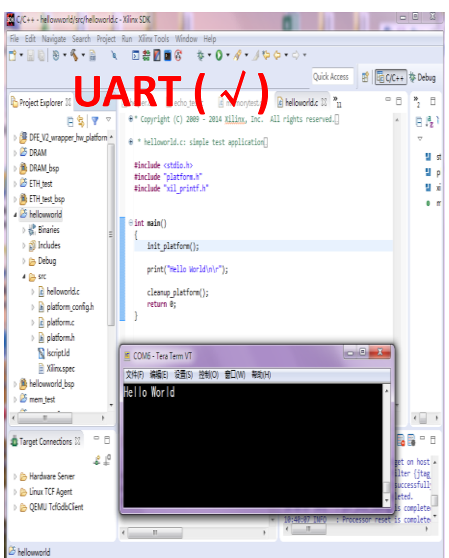


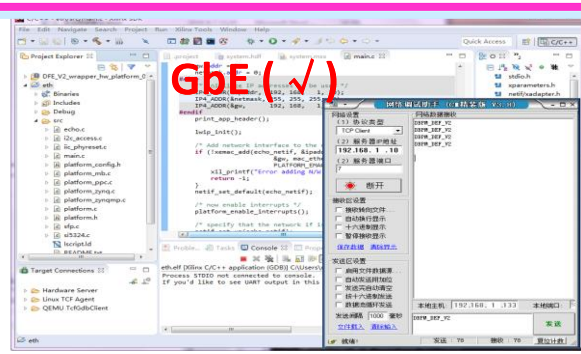






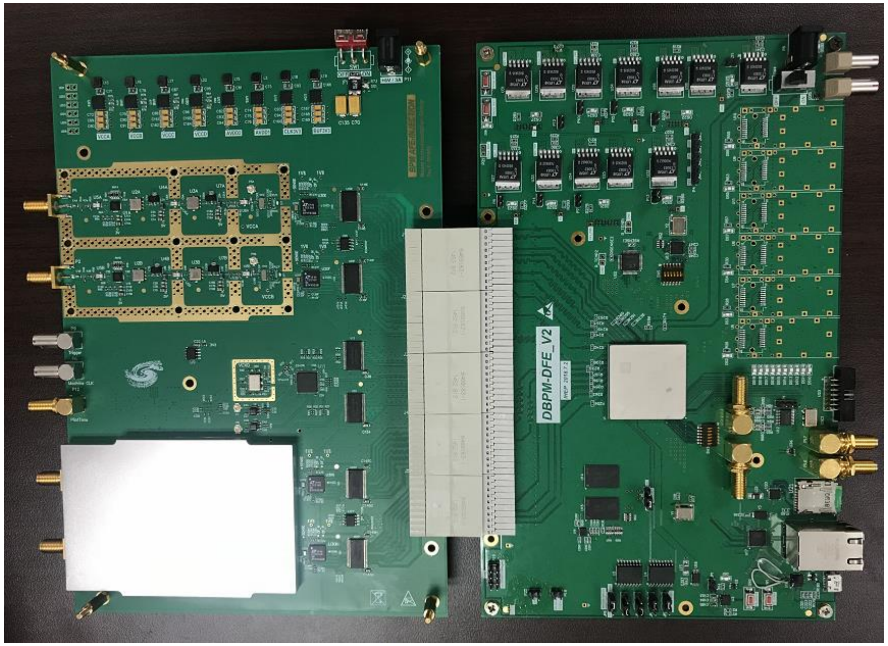






3.3 Forthcoming HW work to be done

- **AFE Board:**
  - RF Circuit(ok)
  - Clock Logic(ok)
  - ADC logic(…)
- **DFE Board: (ok)**
  - Ready for joint testing
- **Testing(…)**
  - Joint Testing(…)
  - Laboratory and On-line testing(…)

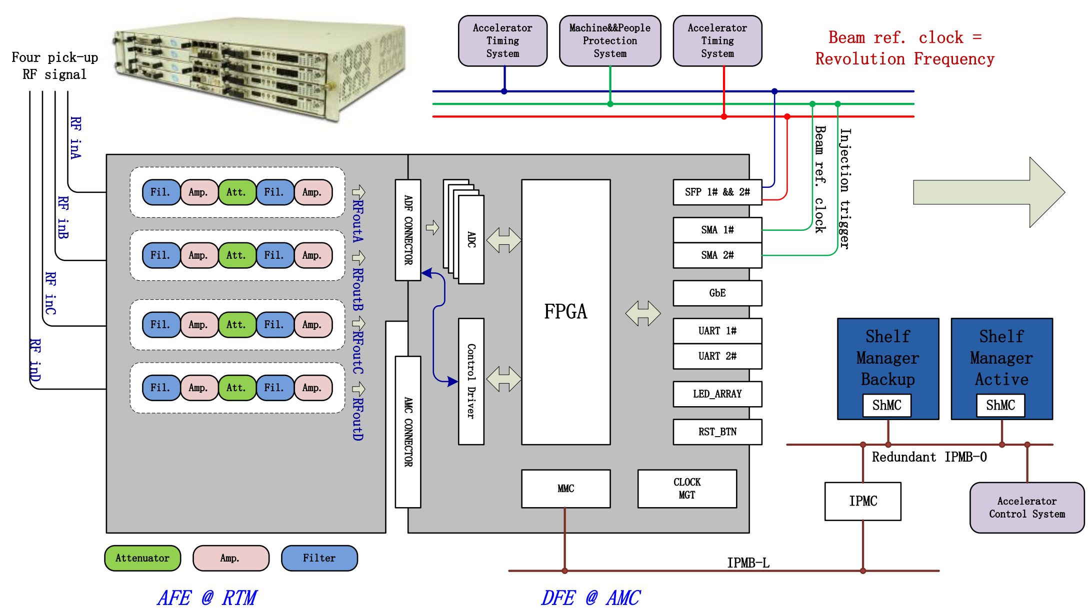


4. Digital BPM pre-research in HEPS-TF project

- System structure
- Hardware design
- Algorithm of Firmware
- Software design
- Digital BPM testing

4.1 System structure

- For the HEPS will have been built several years later, so we develop the DPBM prototype with BEPCII parameters, and DBPM system will tested in BEPCII. And main work include 3 parts:
  - HW design
  - FW design
  - SW design

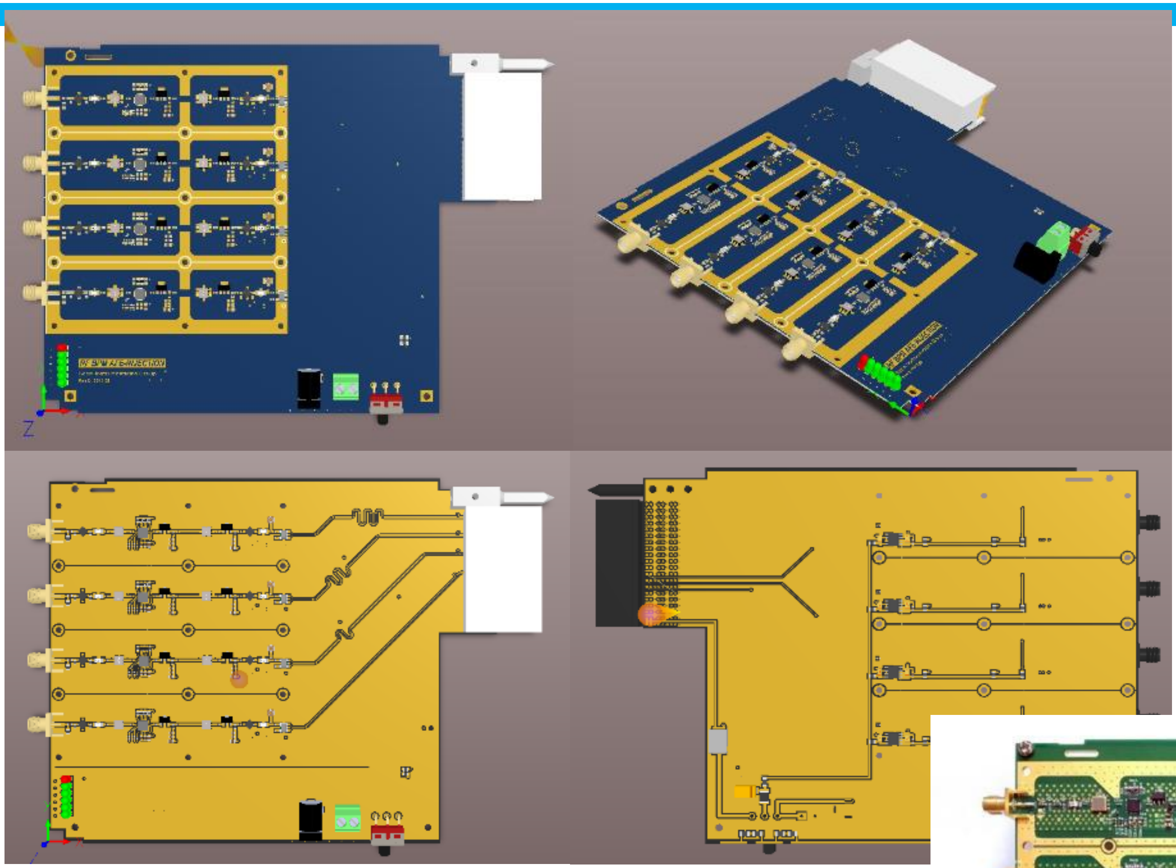


Hardware framework @ Micro TCA.4 chassis

4.2 Hardware design

- RTM Module Design(YaoYao Du)
- AMC Module Design

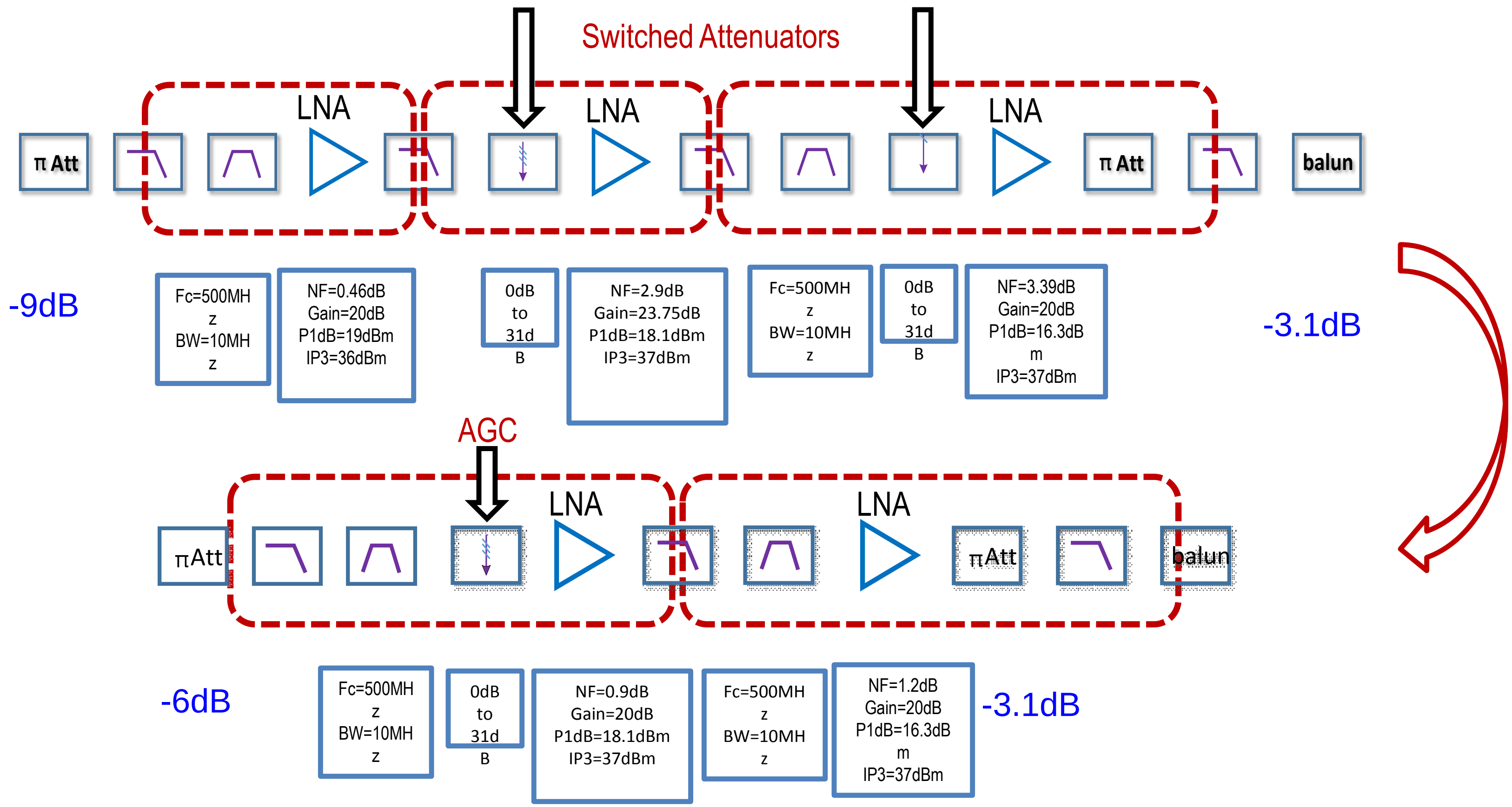
■ RTM Module design



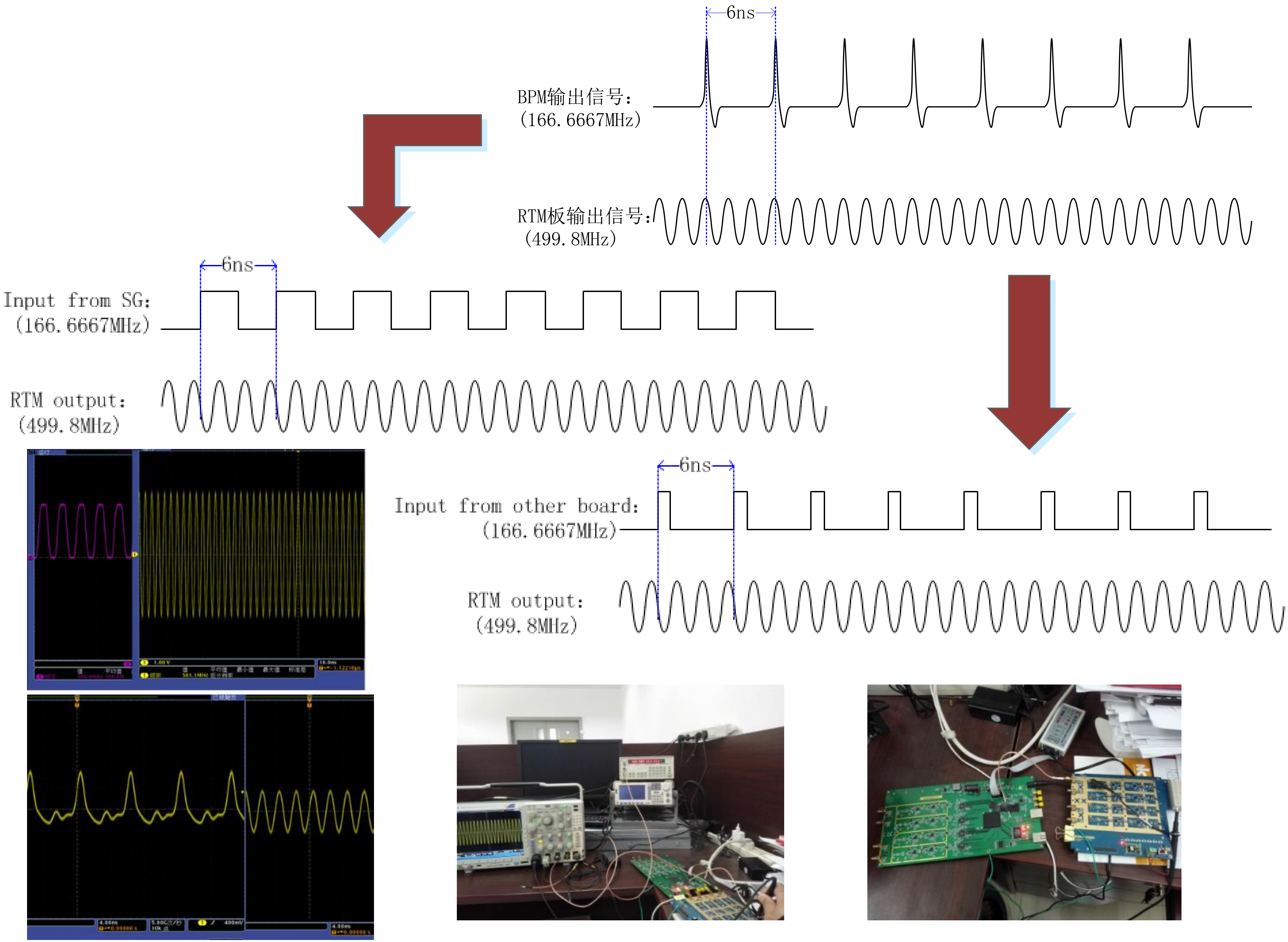
Design objective:

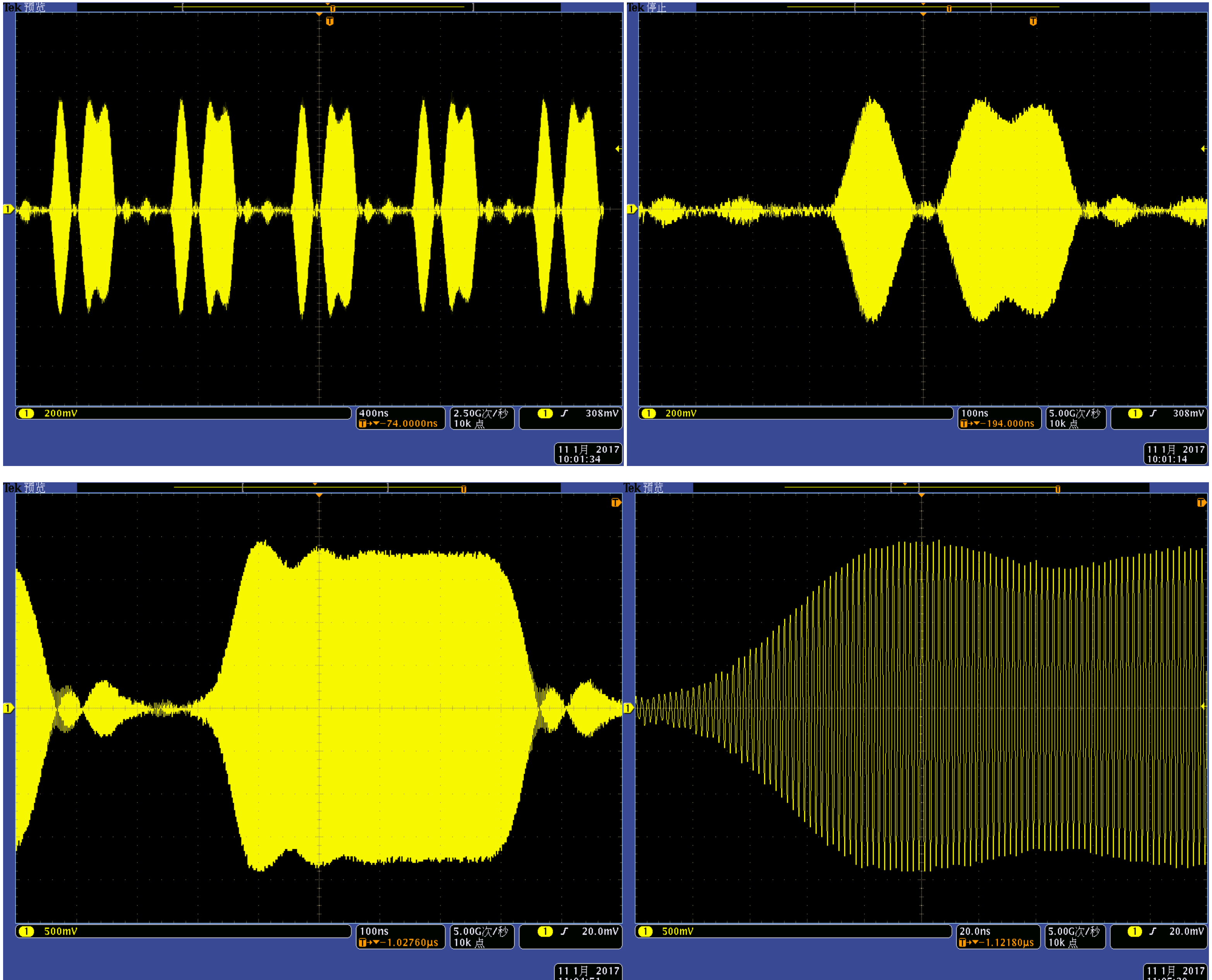
- ✓ Low Noise design
- ✓ Low power consumption

DBPM_RTM function block



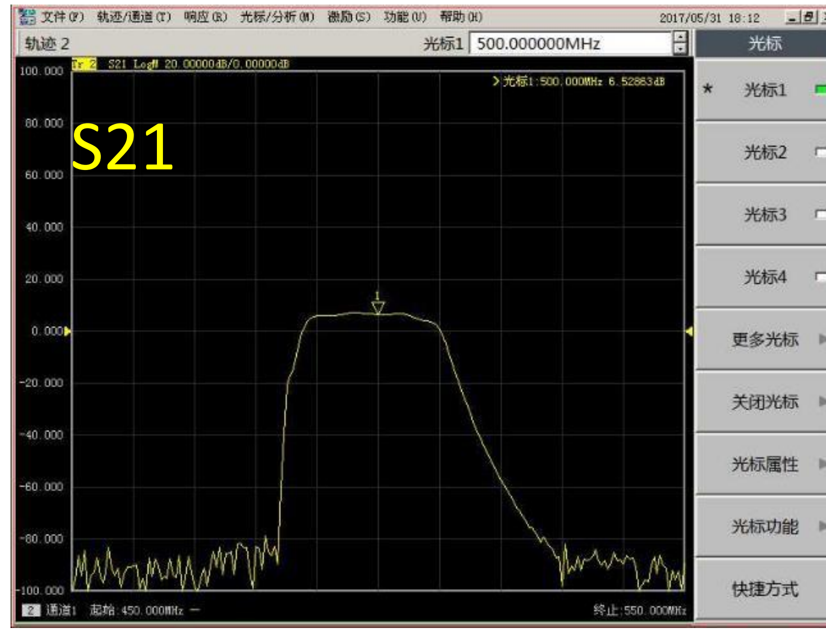
1、 Two LNAs are enough
2、 The place of Attenuator is designed carefully
3、 Attention to the Impedance matching & Noise


6ns
BPM输出信号：
(166.6667MHz)
RTM板输出信号：
(499.8MHz)
6ns
Input from SG:
(166.6667MHz)
RTM output:
(499.8MHz)
6ns
Input from other board:
(166.6667MHz)
RTM output:
(499.8MHz)


Tek 预览
200mV
400ns
−74.0000ns
2.50G次/秒
10k 点
308mV
11 1月 2017
10:01:34
Tek 停止
200mV
100ns
−194.000ns
5.00G次/秒
10k 点
308mV
11 1月 2017
10:01:14
Tek 预览
500mV
100ns
−1.02760µs
5.00G次/秒
10k 点
20.0mV
11 1月 2017
11:04:51
Tek 预览
500mV
20.0ns
−1.12180µs
5.00G次/秒
10k 点
20.0mV
11 1月 2017
11:05:20

DBPM.RTM S-Parameter Characterization

Receiver S-Parameter Characterization



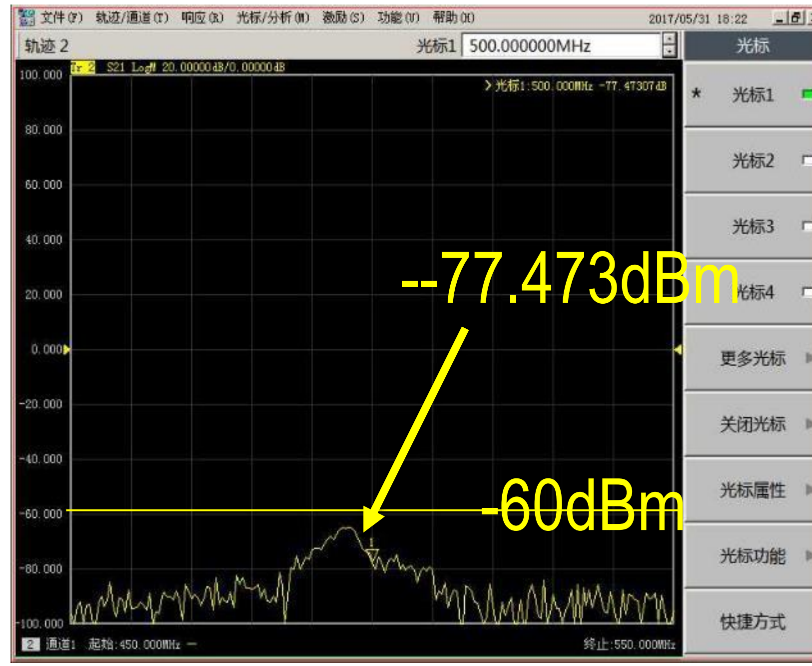
S21-Parameter Characterization

The performance of band pass filter is good!

DBPM.RTM Channel to Channel Isolation

A→B

6.5dBm→-78.8dBm

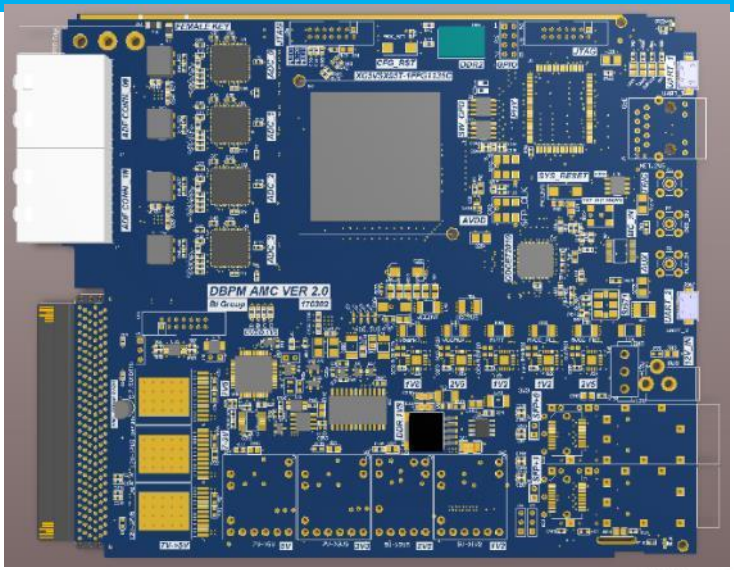


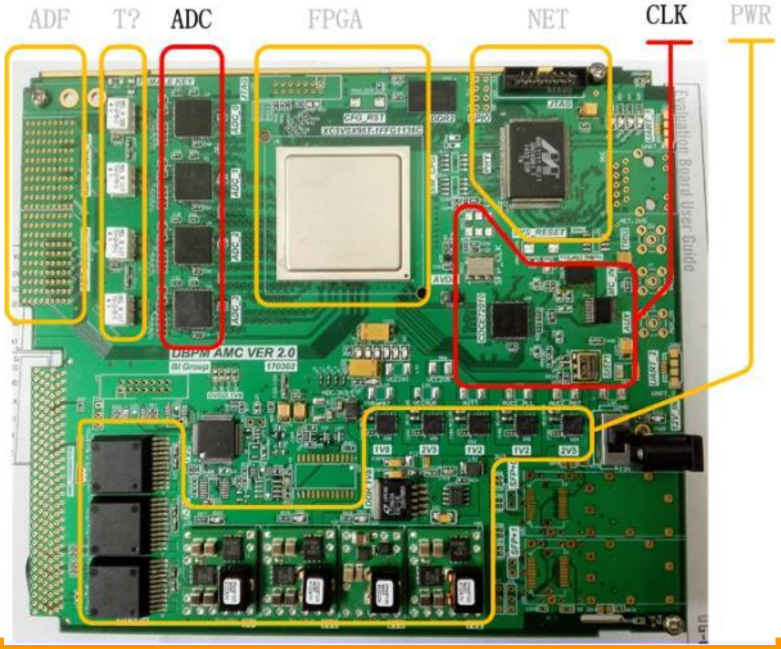
B→A

6.5dBm→-77.47dBm

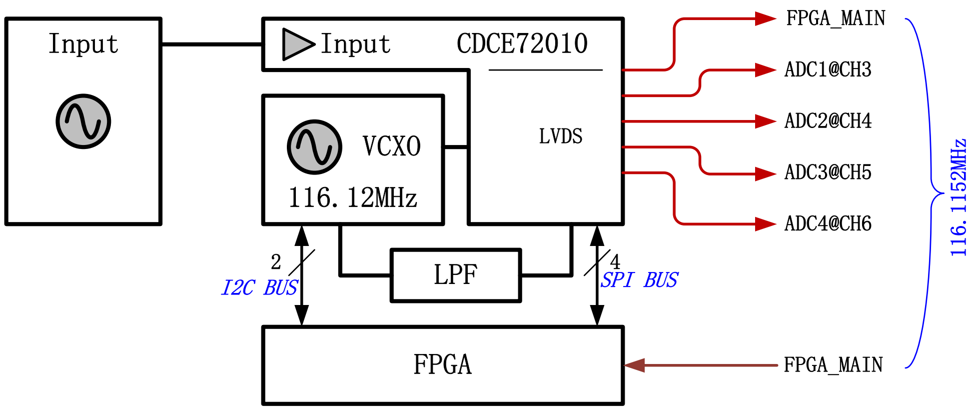
AMC Hardware design

- Power Regulator
- **Clock Logic**
- FPGA Logic
- **ADC Logic**
- NET Logic
- Other Logic…

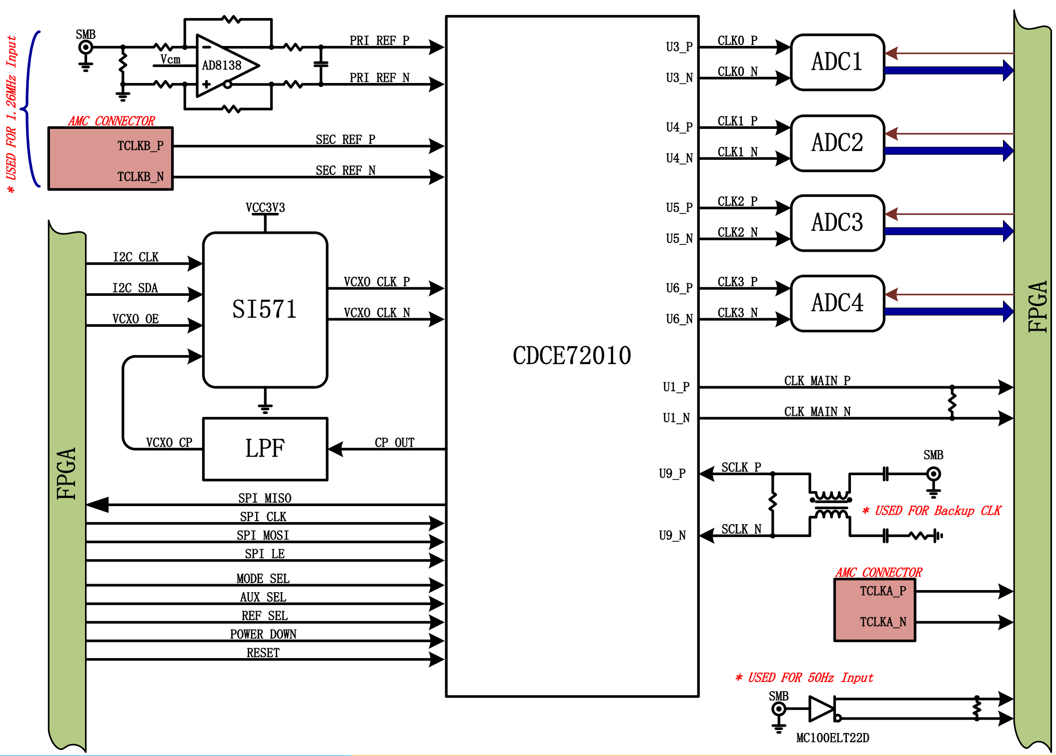


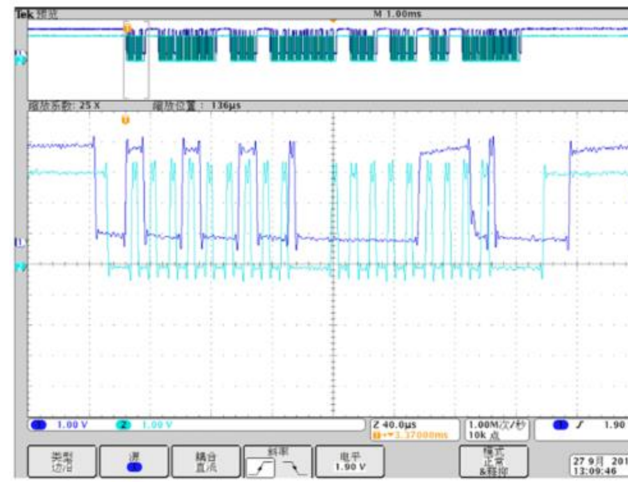


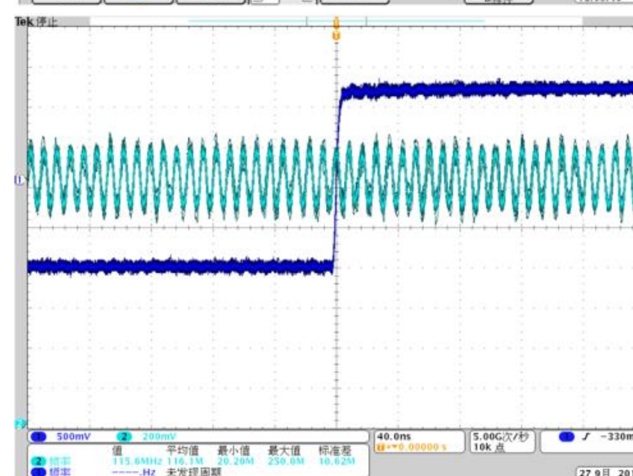
Clock logic Scheme



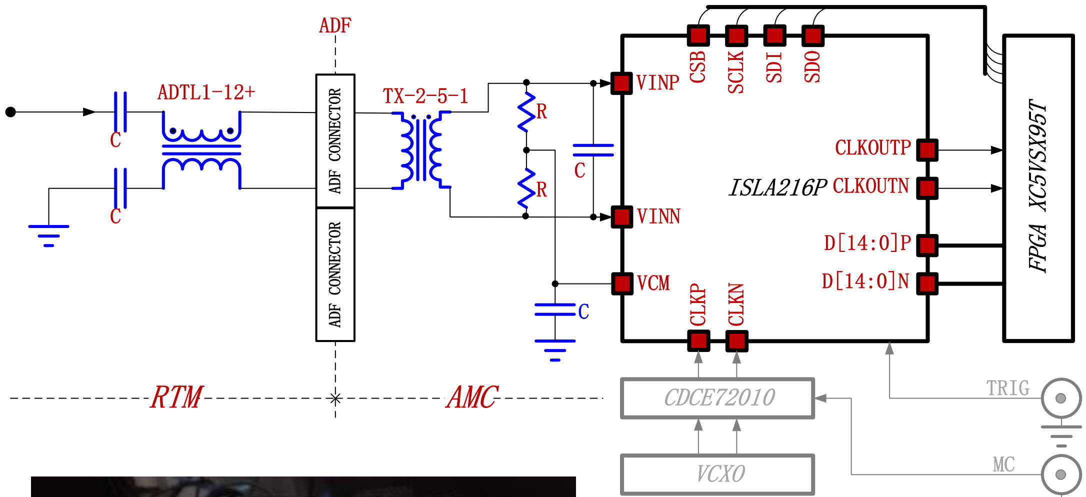
- SI571 Configuration (I2C)
- CDCE72010 Configuration （SPI ）





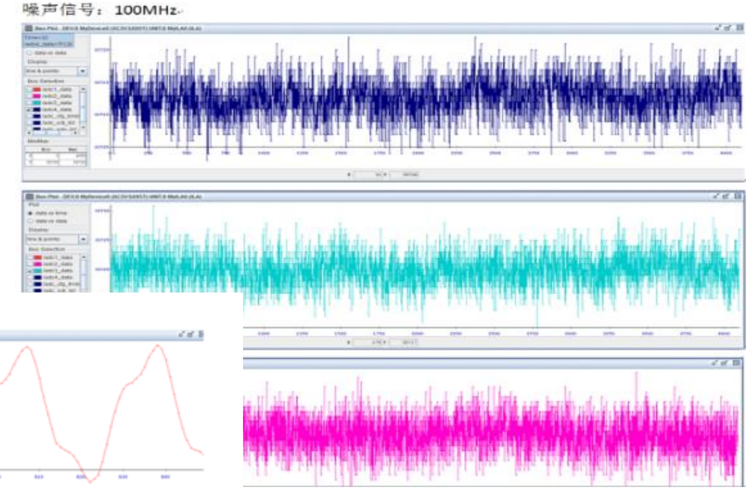


ADC Logic Scheme

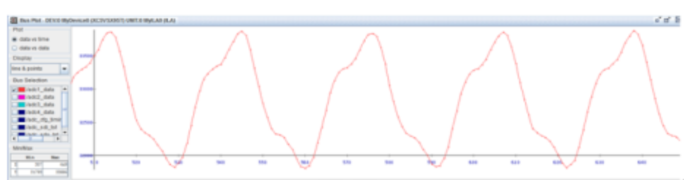


SPI总线配置时序

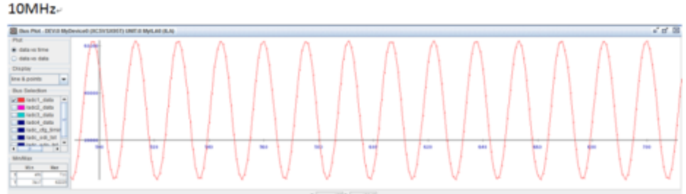
噪声信号：100MHz



5MHz

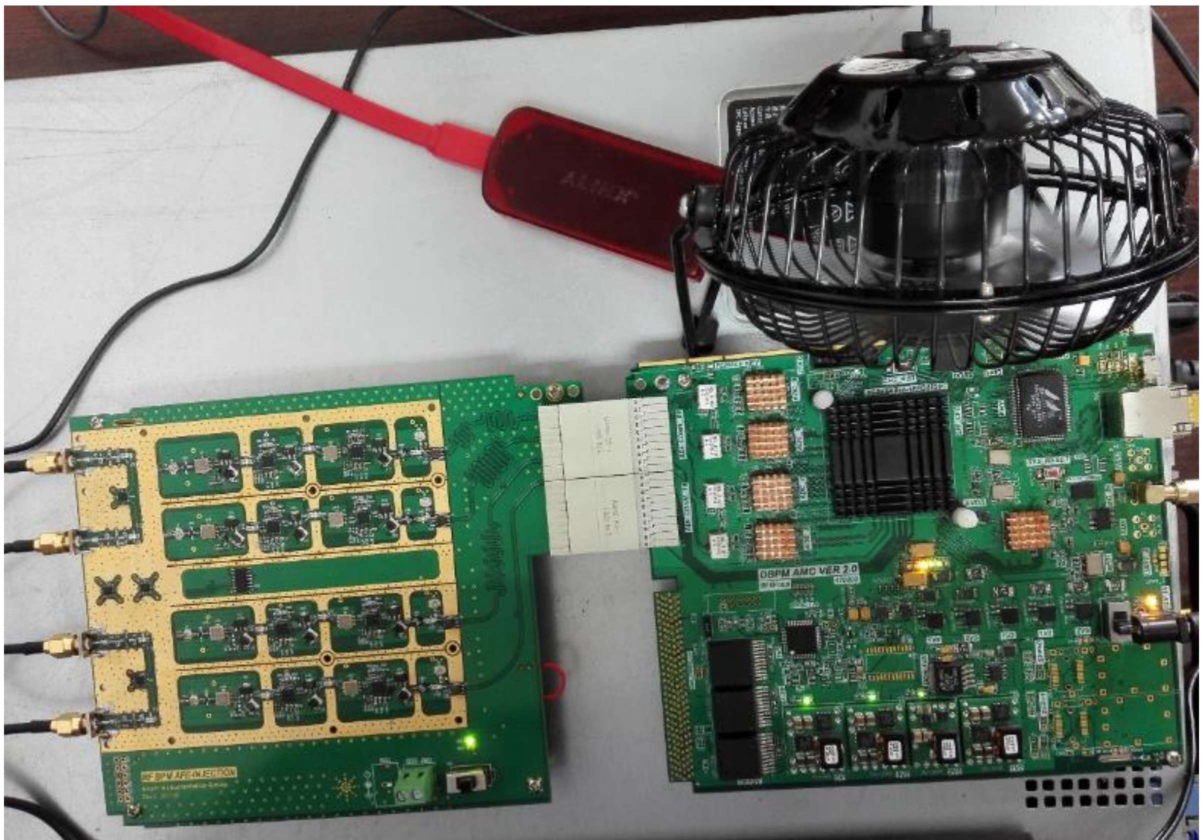


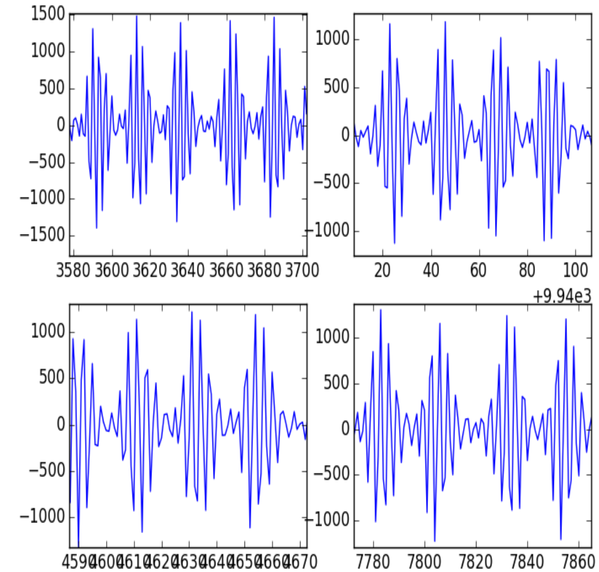
10MHz

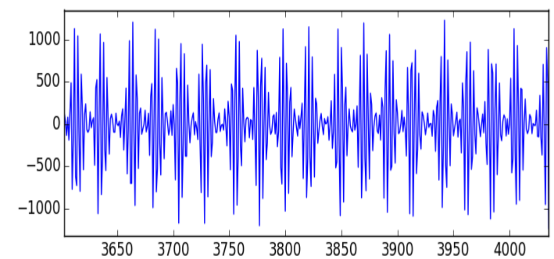


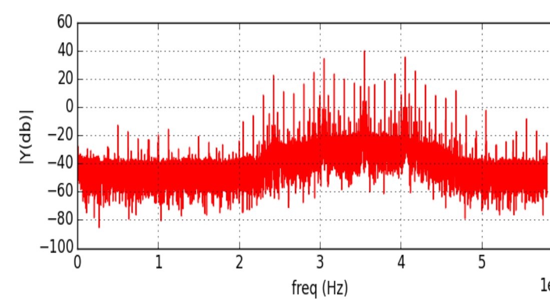
Joint Testing in Laboratory

Simulated pattern ADC read out and off-line analysis



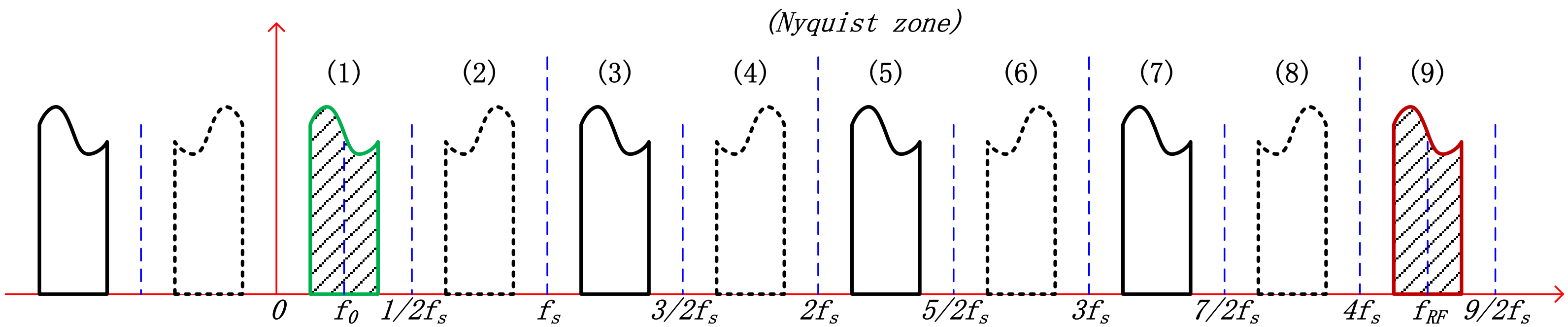


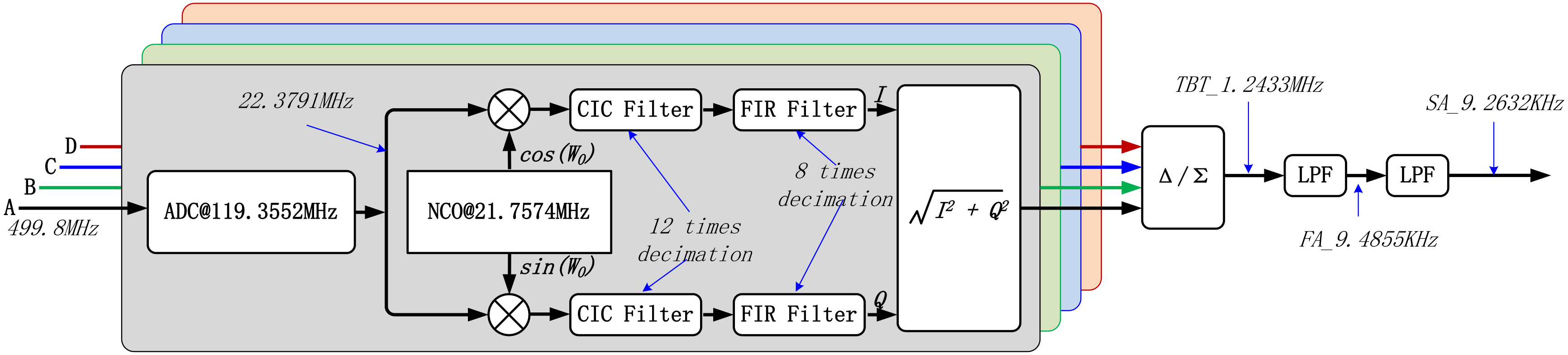




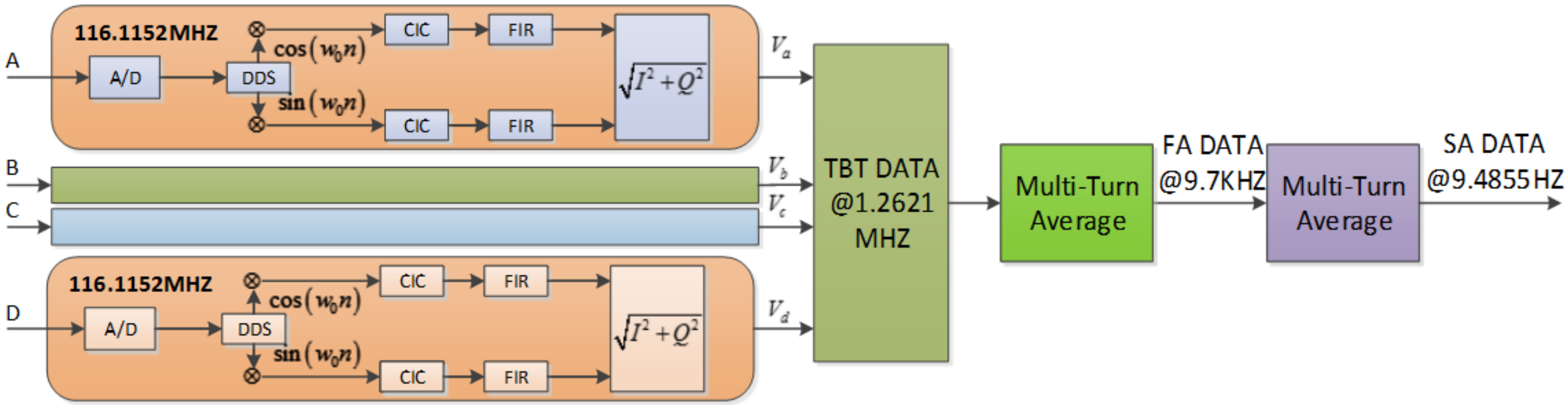
4.3 Algorithm of Firmware design

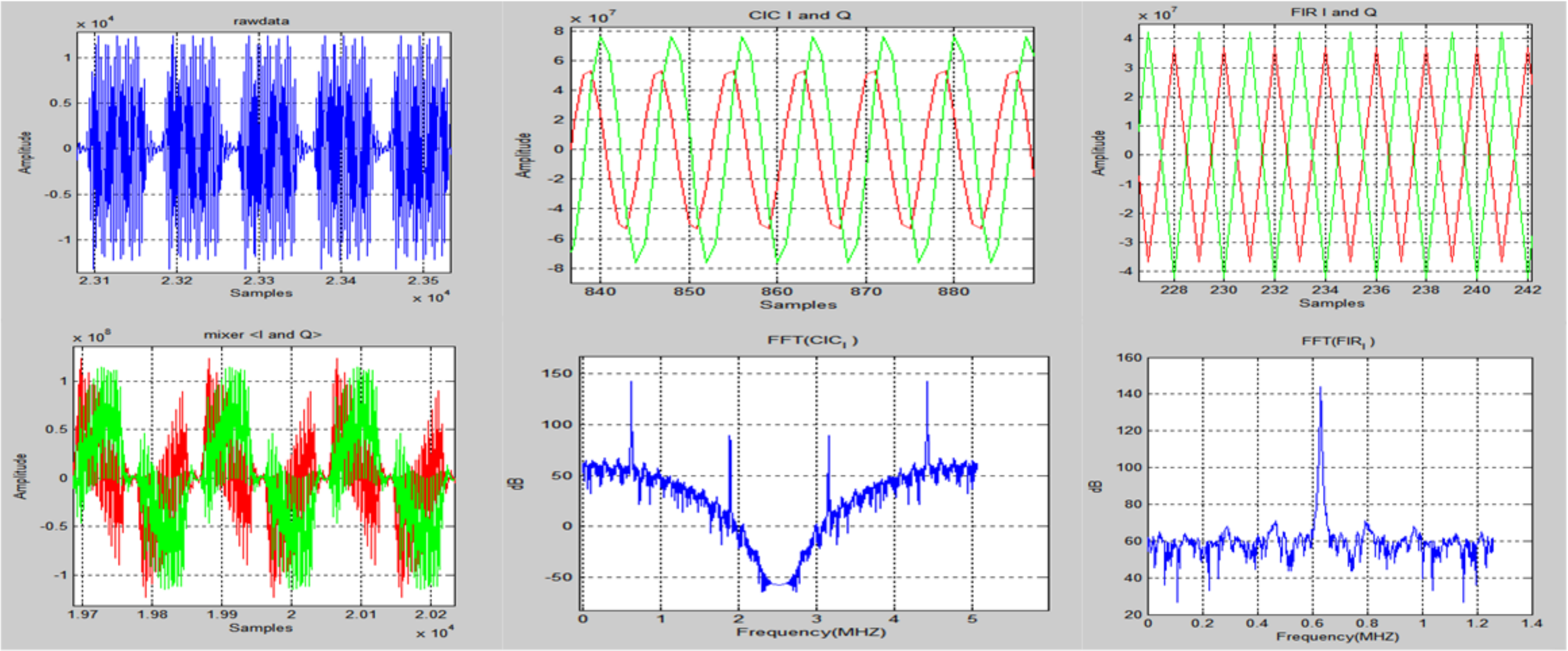
- MATLAB simulation (YuFei Ma)
- HDL Implementation



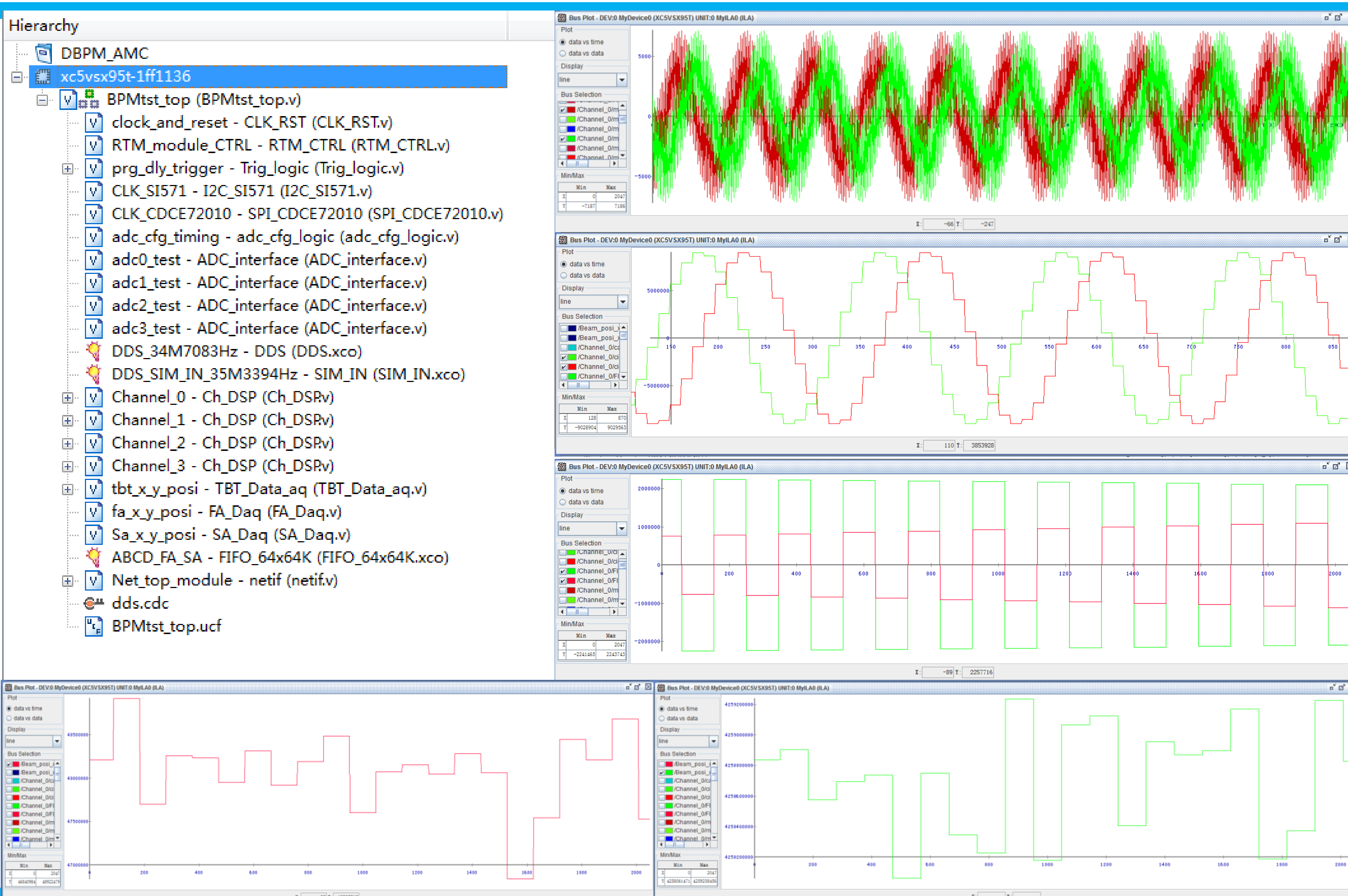


MATLAB simulation





HDL Implementation

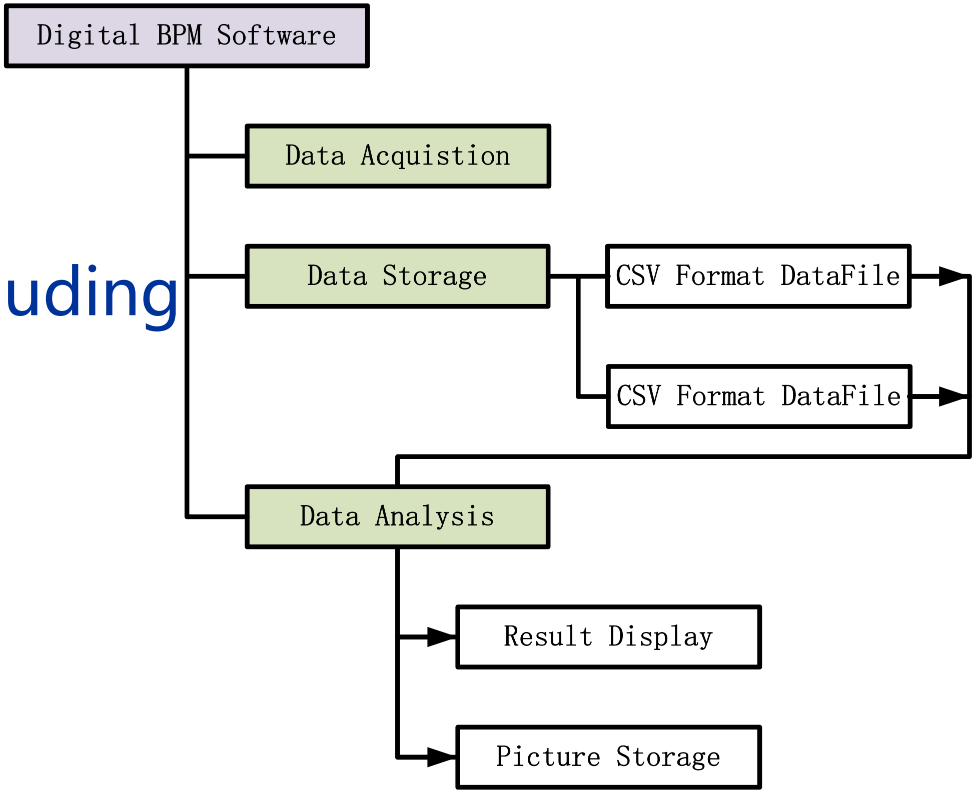


Other Algorithm study

- DFT Algorithm(Fang Liu)
- Hilbert transformer method. (Qiang Ye)
- Time domain dynamic window integrating method. (YuFei Ma)

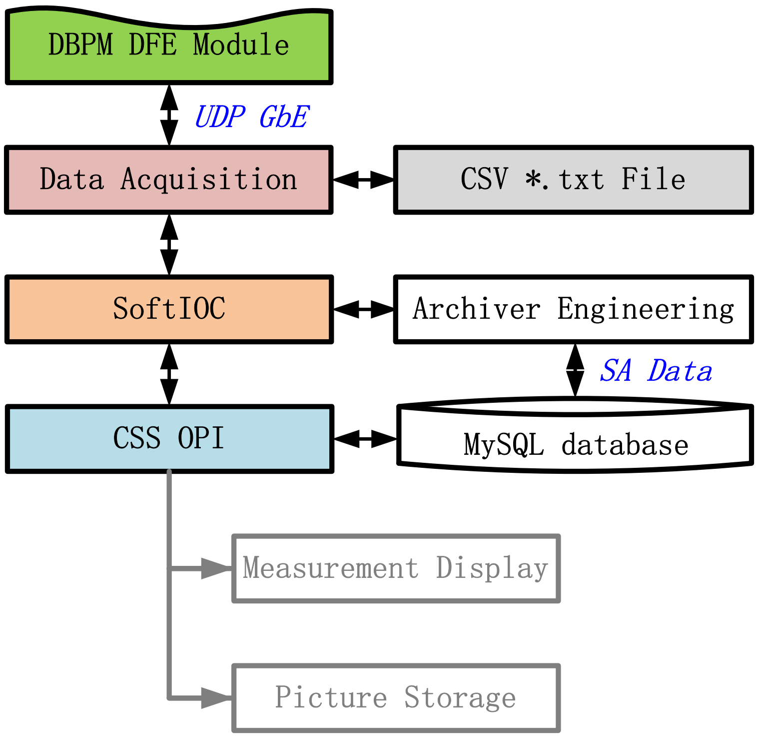
4.4 DBPM Software design

- Software framework include 3 main part:
  - Data Acquisition
  - Data Analysis
  - Data Storage
- The Software is built with **Python** (2.7.10) tools, including module:
  - Scipy1.0
  - Numpy
  - Pandas
  - Matplotlib
  - Pyepics
  - Pyqtgraph



Data Acquisition Module

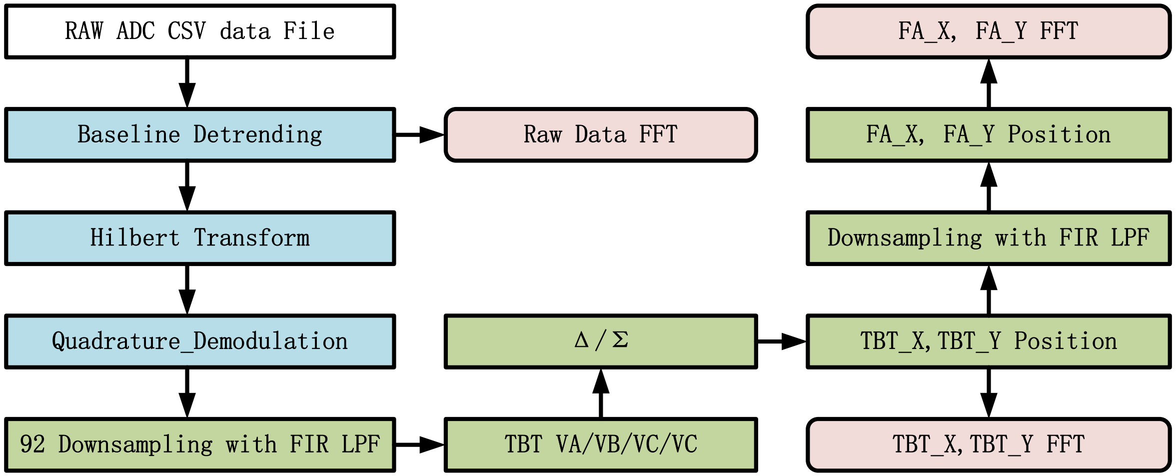
- SA Data Acquisition function block.
  - Data Acquisition control logic
  - Write/Read CSV file logic
  - EPICS IOC Logic
  - Data base logic
  - Graphical User Interface
  - …



Data Analysis Module

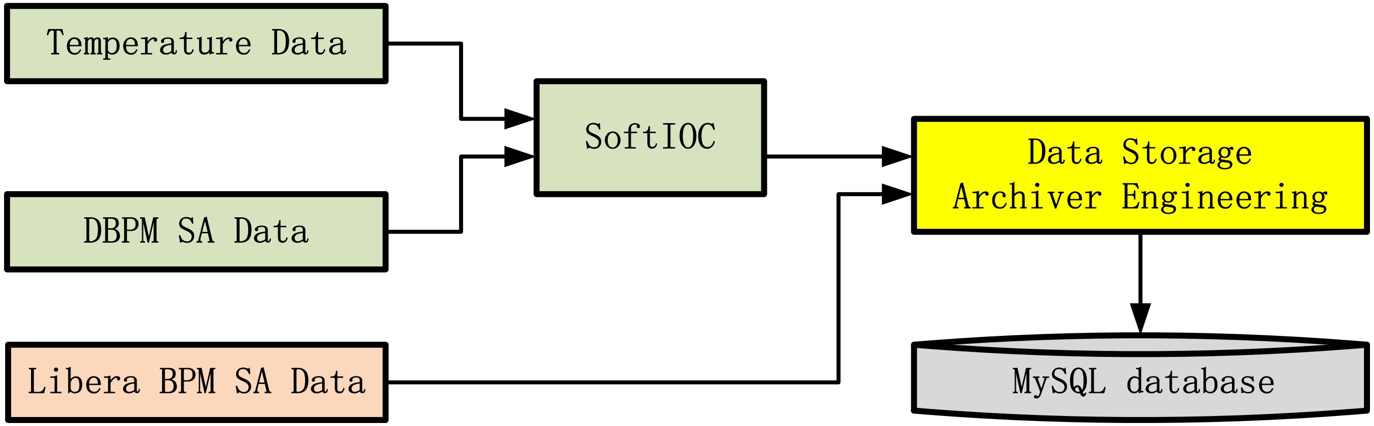
- Data Analysis function block.
  - Data Hilbert Transform and Quadrature Demodulation
  - TBT and FA Position calculation
  - FFT Analysis.

Note: The function is designed to verify the result processed in FPGA.

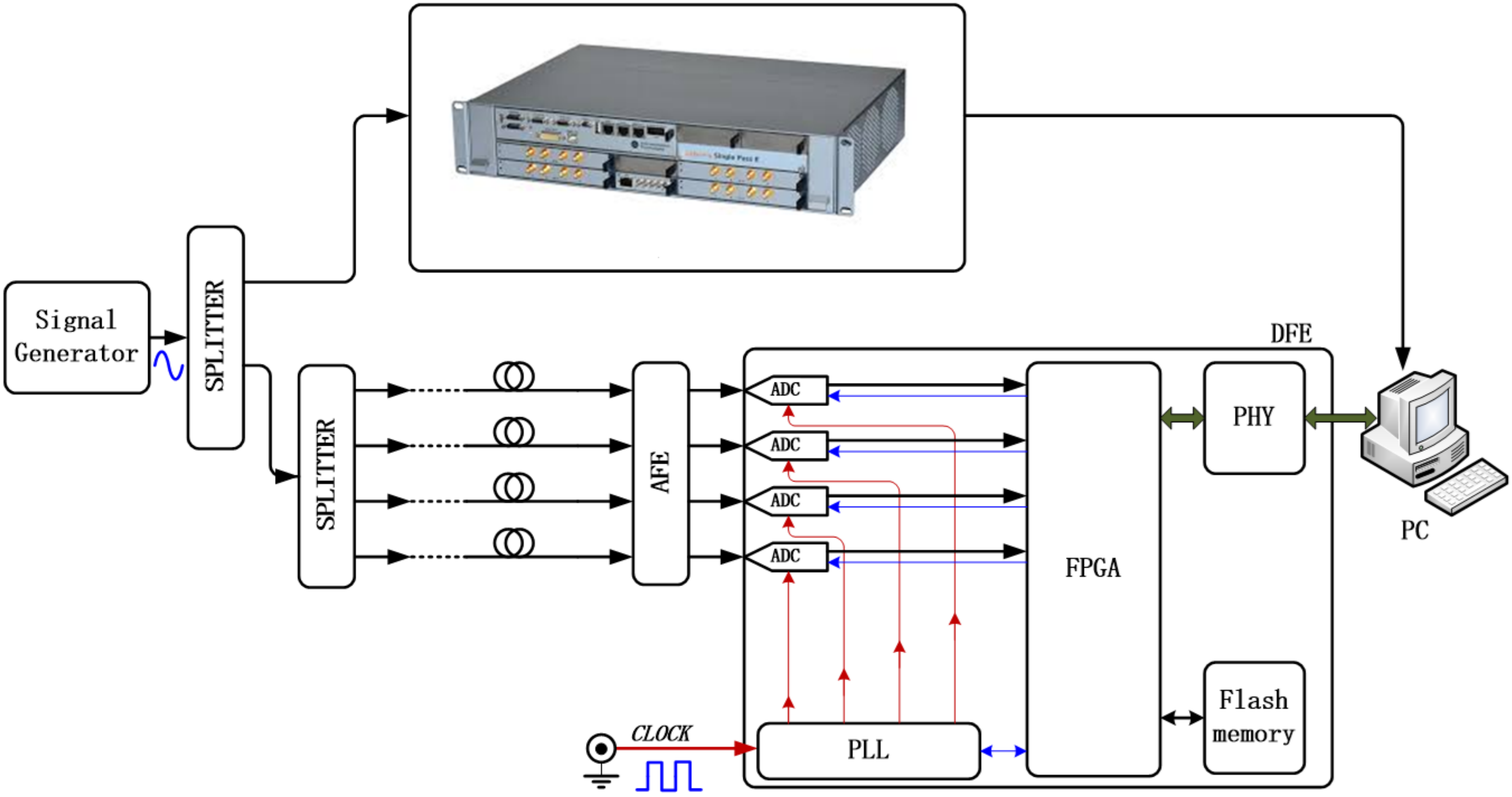


Data Storage Module

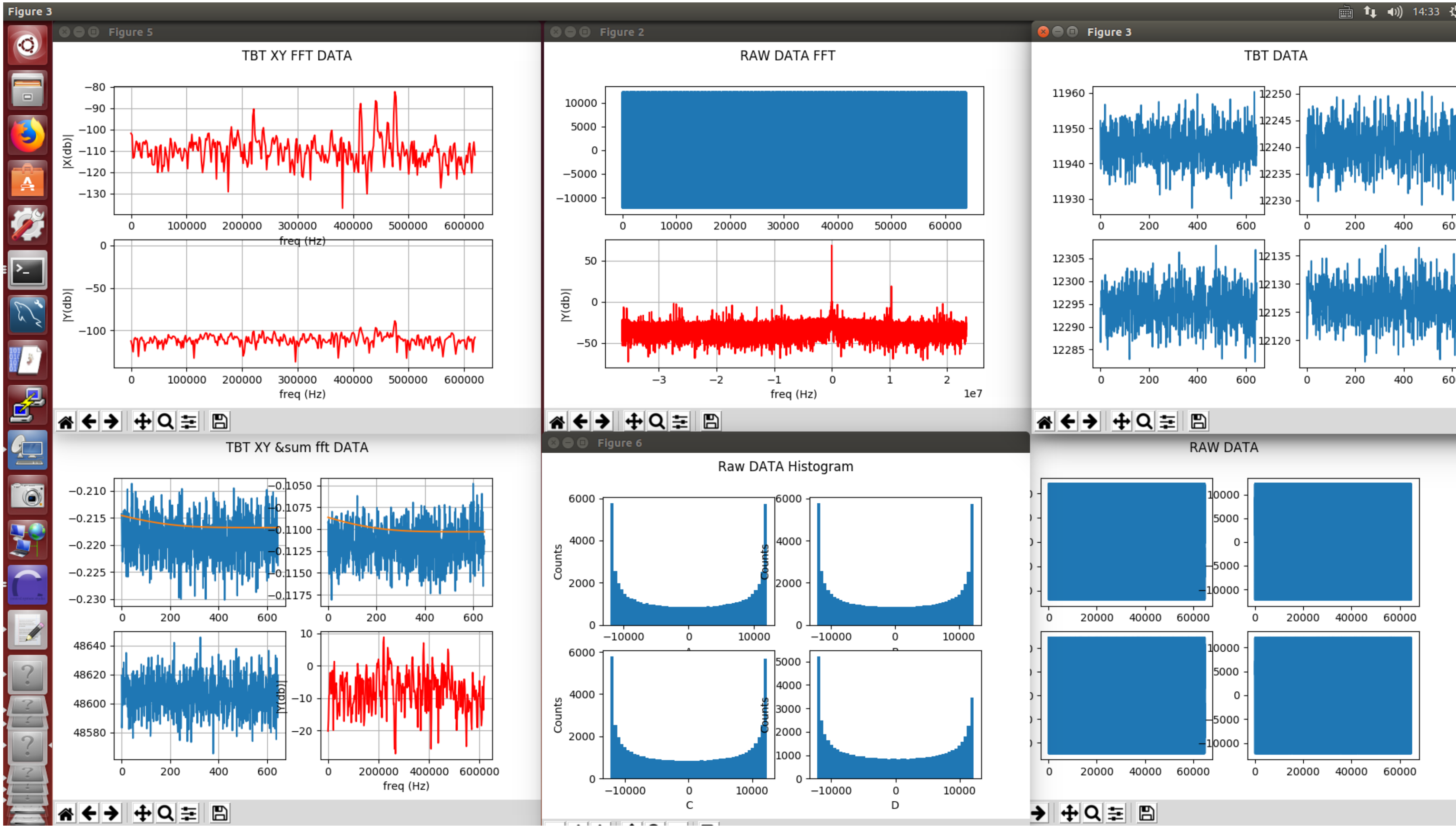
- Two Methods are used in Data Storage:
  - – CSV txt format file
  - – RDB Archiver Engineering MySQL database



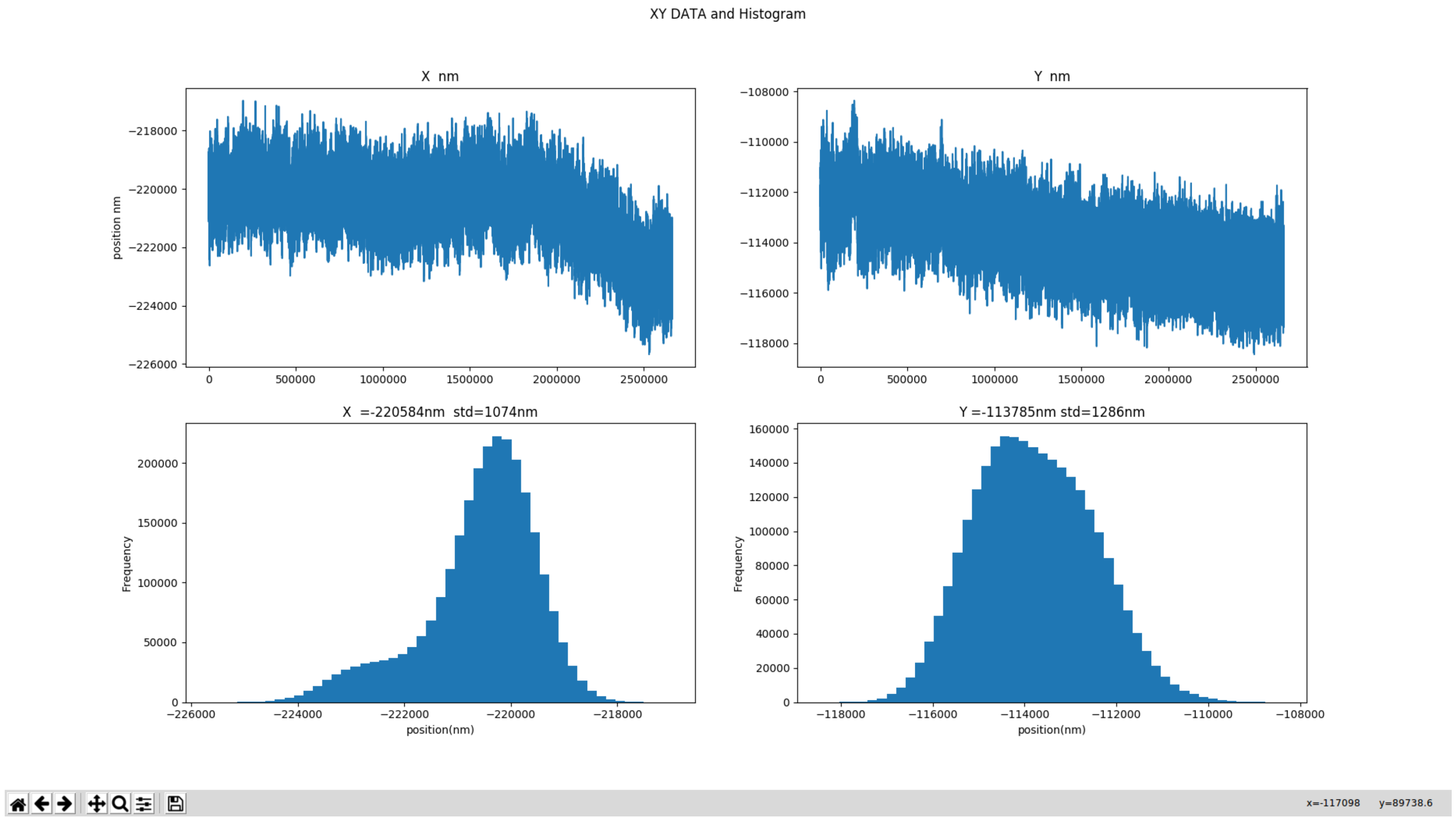
Digital BPM testing



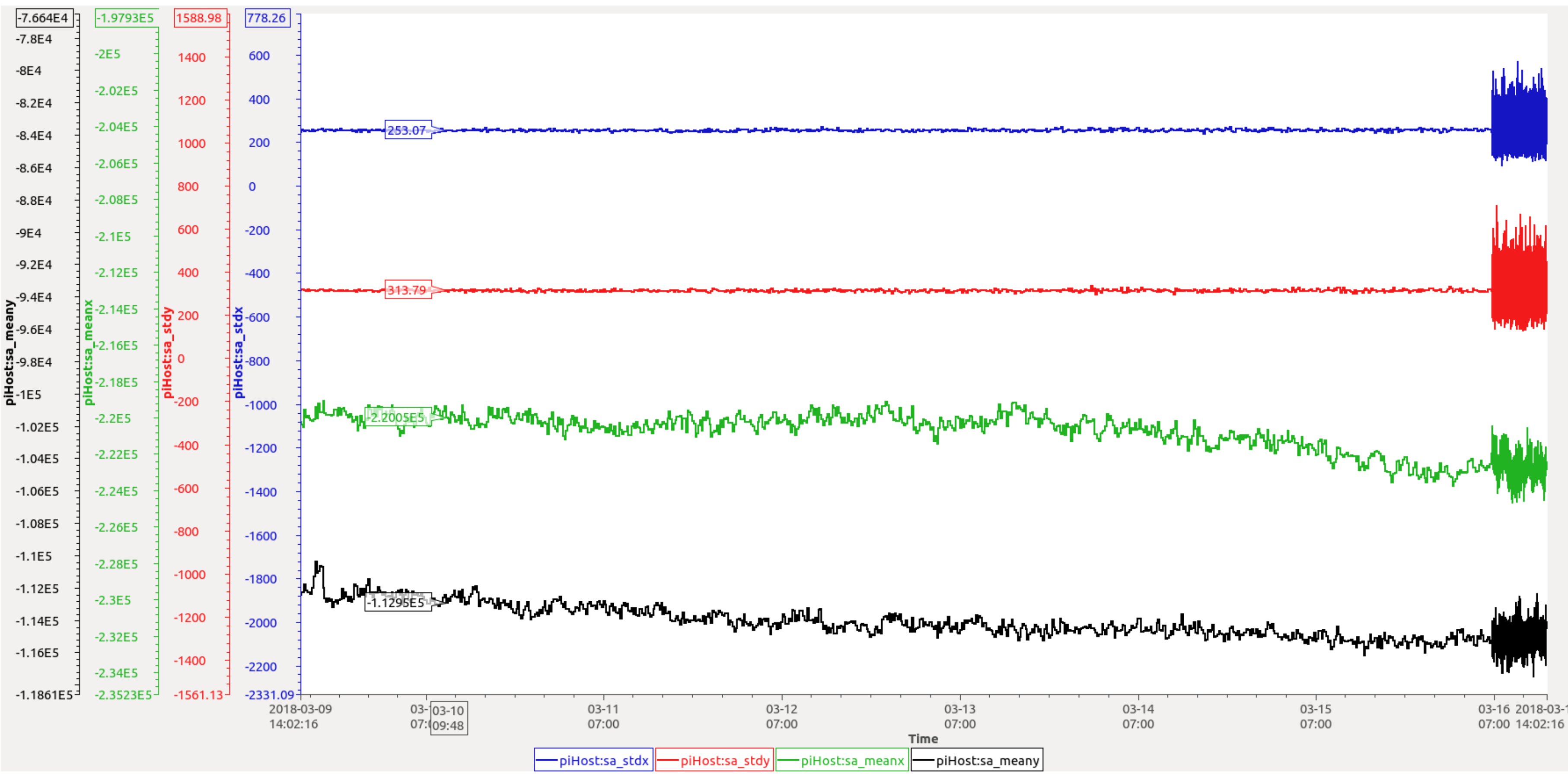
RAW ADC data and Analysis



SA Data testing



Long term testing for 7 days



Have Passed the Final acceptance tests

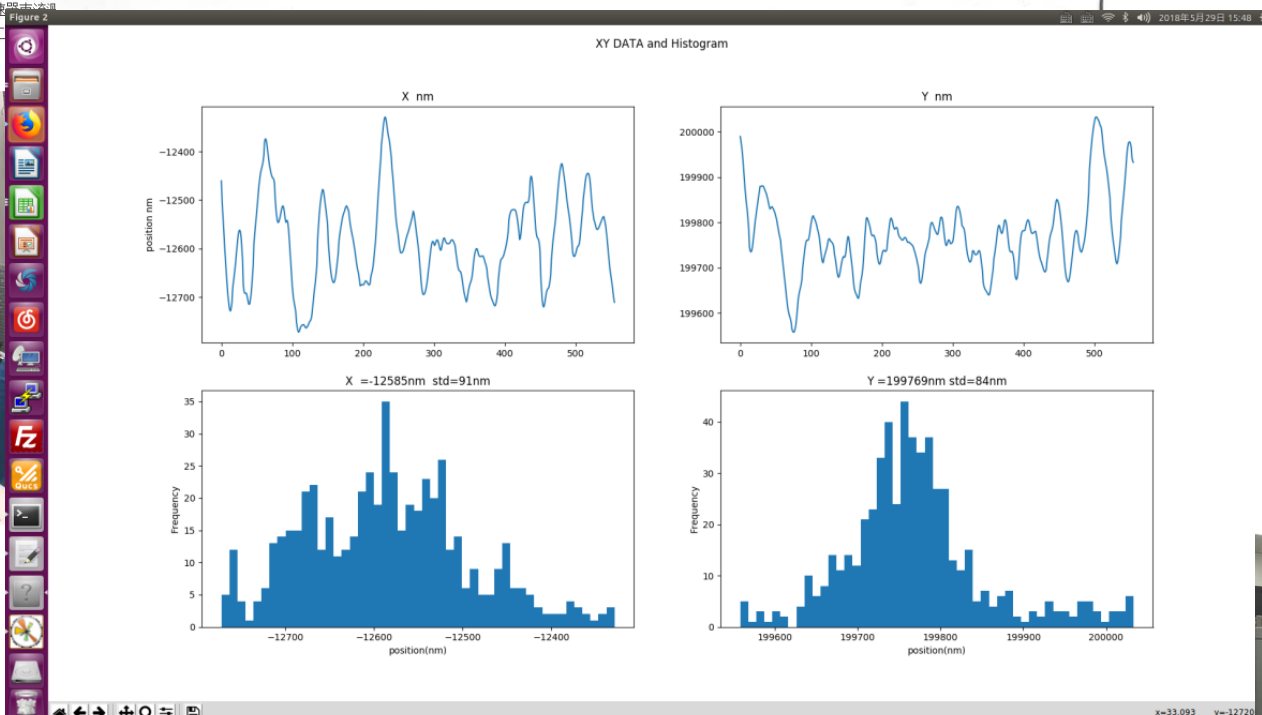
HEPS-TF束

5月15日，高能同步辐射光源验证装置
实验室、上海应用物理研究所、中国原子能
孙葆根研究员担任测试组组长。

工艺测试在A419会议室举行，HEPS-TF
审查了工艺测试大纲，然后在五号厅束测实
轨位置分辨率小于0.1μm、快轨道位置分辨
试。

数字束流位置测量系统是加速器束流
空白。其意义不仅在于降低HEPS工
极其重要的意义。

测试内容	验收指标	测试结果	测试结论
闭轨测量	0.1μm	<0.1μm	优于设计指标
快轨道分辨率	0.3μm	<0.3μm	优于设计指标
逐圈分辨率	1μm	<1μm	优于设计指标



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的验收指标

工艺测试

【大 中 小】

直和光束线站分总体的微纳聚焦等四系统通过了院

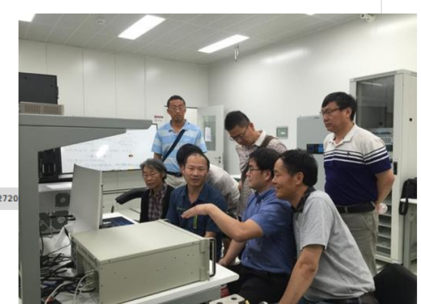
、高能所，合肥物质科学研究院等离子研究所、中

-TF不同于一般预研项目，是作为建设国家重大科
采取了“成熟一批，测试一批”，此次为工程的最
要求。

，经过努力，自测达到了验收指标，因存在在线测
审查把关，项目组将全力配合。

试结果形成一致意见：插入件、束测、机械准直和
达到或者优于设计指标。

了工艺测试，技术指标全面达到国家发展改革委批



http://www.ihep.cas.cn/xwdt/gnxw/2018/201805/t20180521_5014039.html

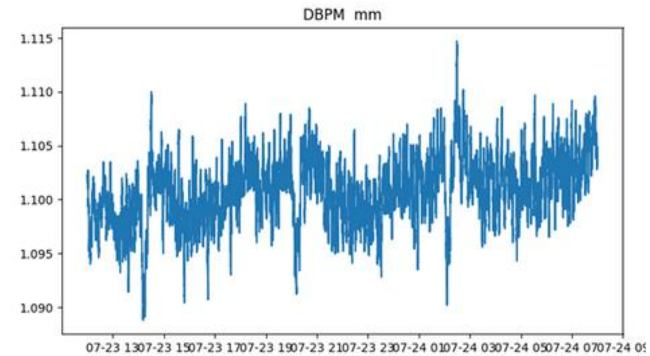
The Digital BPM have applied to BEPCII Storage ring

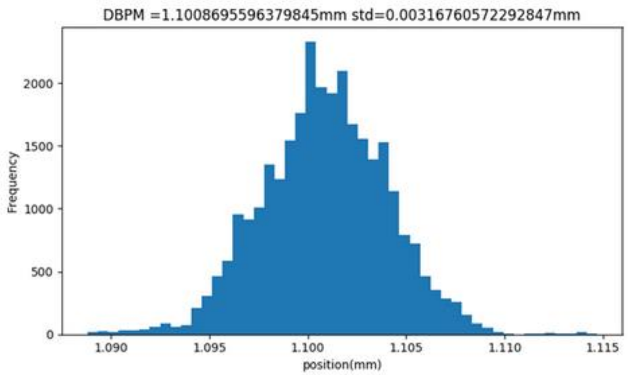
IHEP-developed DBPM First Used on BEPCII Storage Ring

2018-09-11

In the most recent run of BEPCII in dedicated synchrotron radiation mode, the Digital Beam Position Monitor (DBPM) electronics, developed by the Institute of High Energy Physics, operated successfully for the first time.

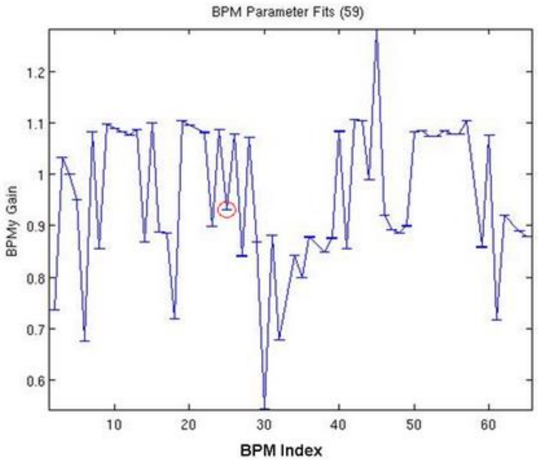
The DBPM was in stable operation for 12 days with the beam current ranging from 120mA to 250mA. The beam position resolution of closed orbit distortion (COD) in the vertical direction was about 3.17μm, with data acquisition from 12:00 a.m. on July 23 to 8:00 a.m. on July 24.





The beam position resolution results for the IHEP-developed DBPM (Image by IHEP)

Before connecting it to the Beam Position Monitor (BPM) system in BEPCII, the closed orbit response matrix of BEPCII was measured using the DBPM. The DBPM gain in the vertical direction was 0.93, with a measurement error smaller than 10%, which meets BEPCII requirements well.



Response measurement results for the domestically made DBPM (Image by IHEP)

As for the DBPM, its higher positon resolution was difficult to realize because of its complicated hardware and firmware. The DBPM group of IHEP has conquered all kinds of difficulties and made great progress in DBPM development over the past three-and-a-half years.

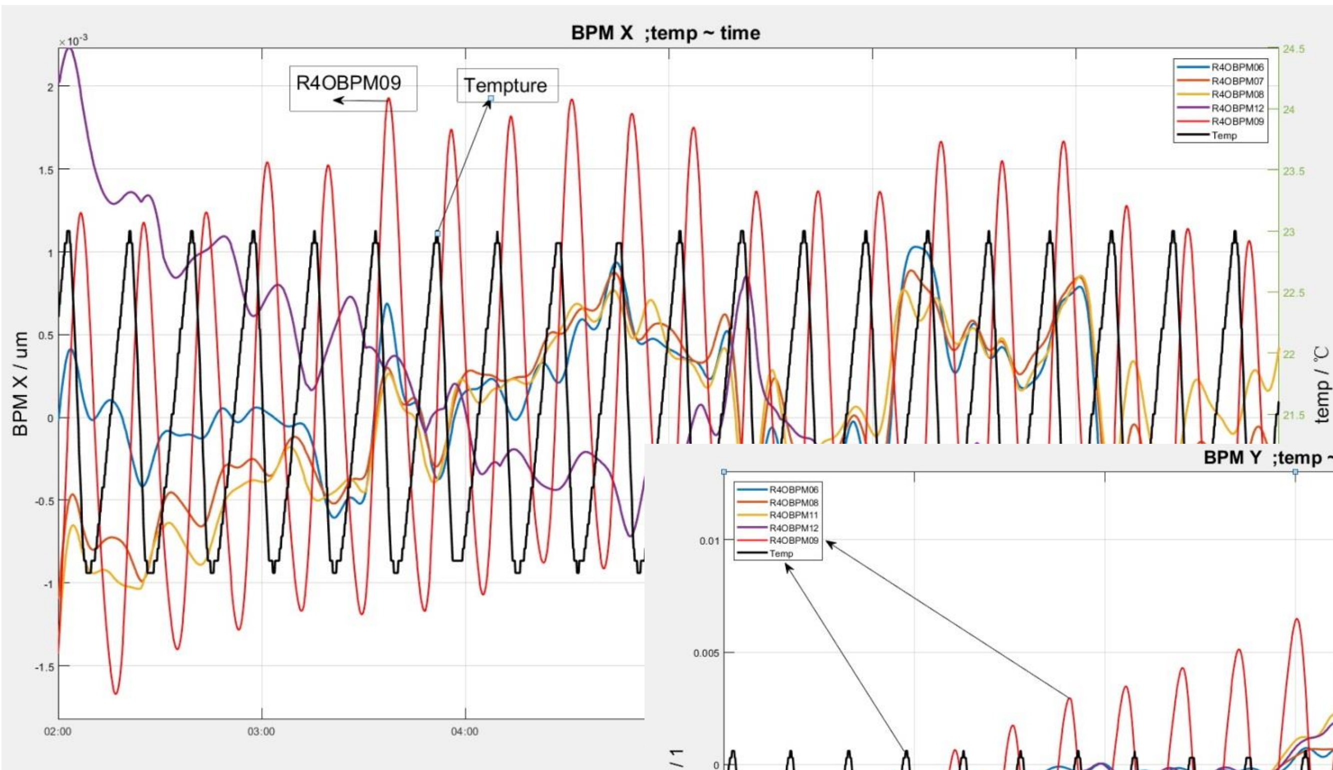
This is the first time a domestically developed DBPM has been used on an electron storage ring in China, proving that IHEP's DBPM can be put into service. It also lays a solid foundation for upgrading BEPCII's analog BPM electronics and for the upcoming High Energy Photon Source (HEPS) project.

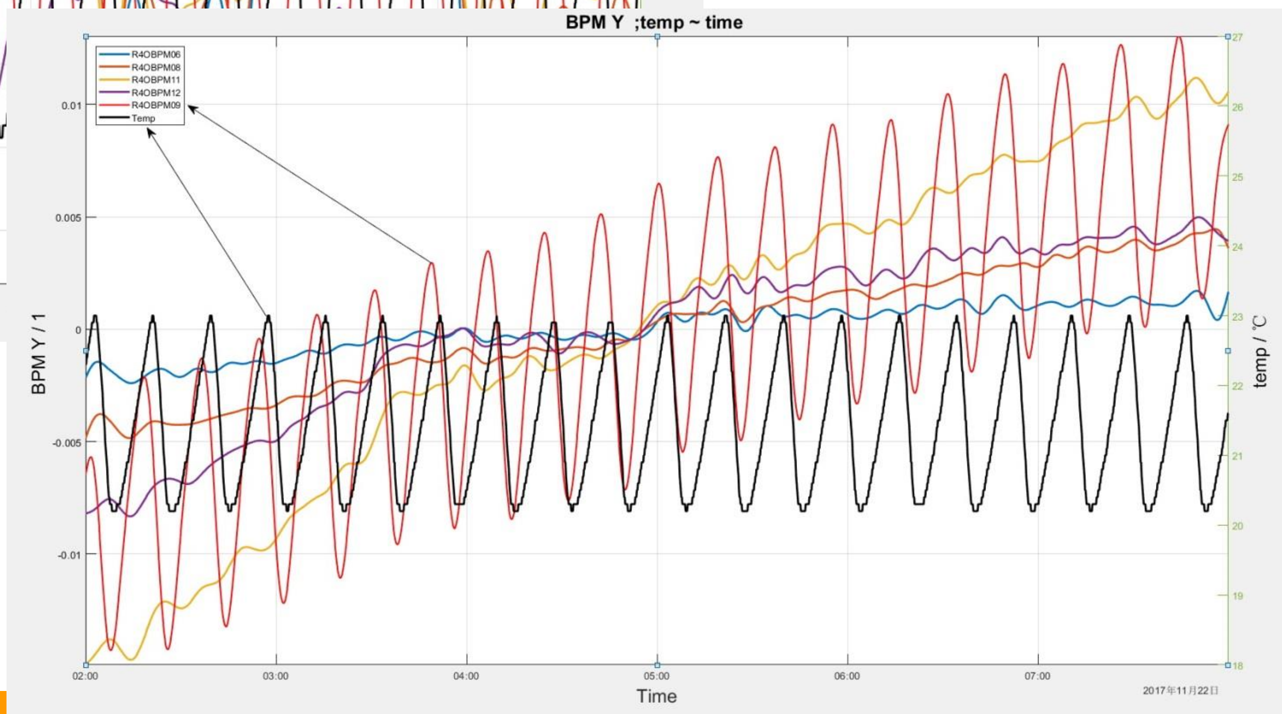
- Have got about 3.17μm resolution for 20 hours with BEPCII real beam.

http://english.ihep.cas.cn/doc/3190.html

5. Temperature influence discussion

Temperature influence in BPM measurement

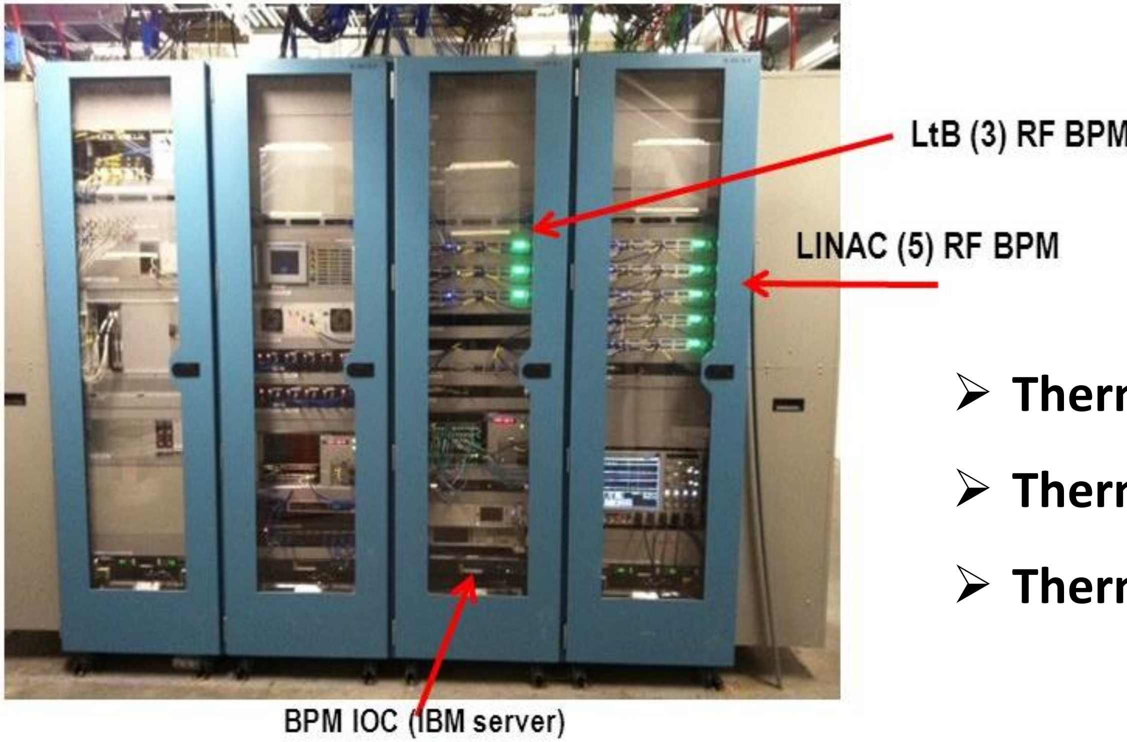




How to reduce the temperature influence ?

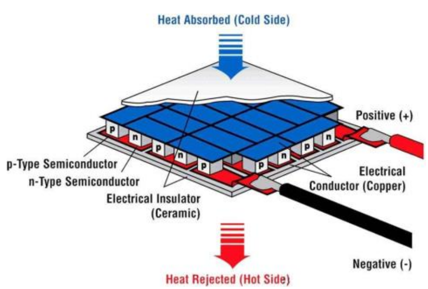
- Thermostatic control (NLS2…)
- Cross-bar Switch Method (LIBERA, Brazil-Sirius)
- Pilot Tone(NLS2 …)
- ……

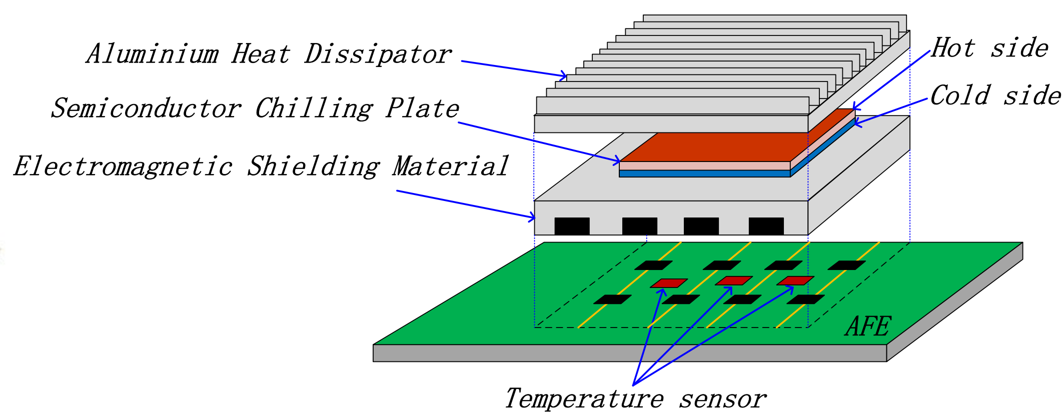
Thermostatic control technology



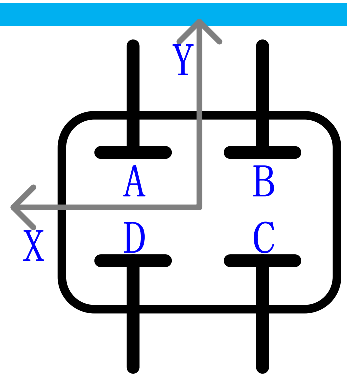
LtB (3), and LINAC (5) RF BPM Thermal Rack Installation

- Thermostatic control Cabinet
- Thermostatic control Crate
- Thermostatic control Circuit；



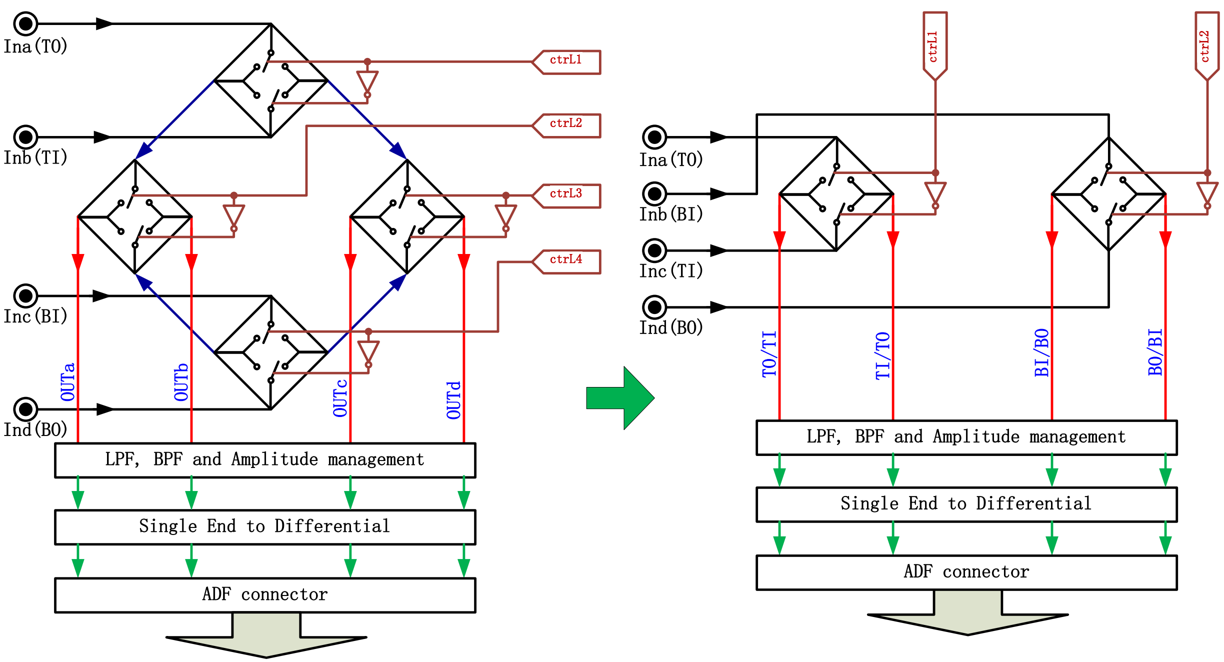


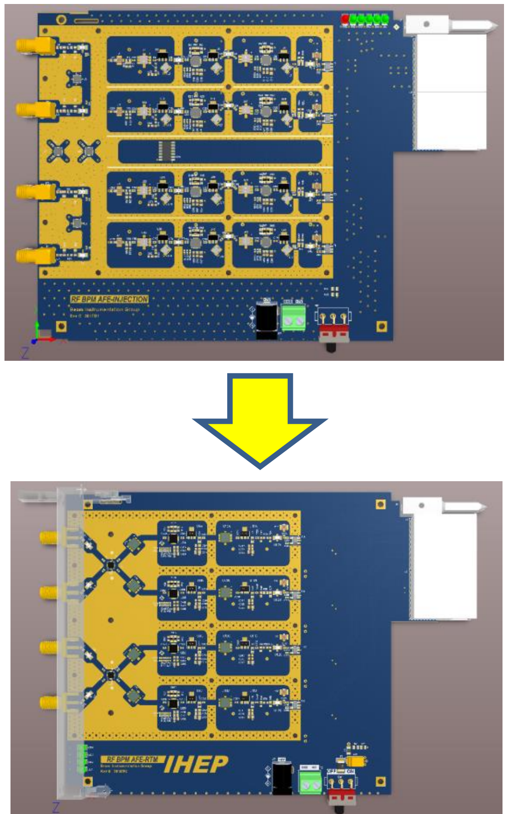
Cross-bar switching scheme



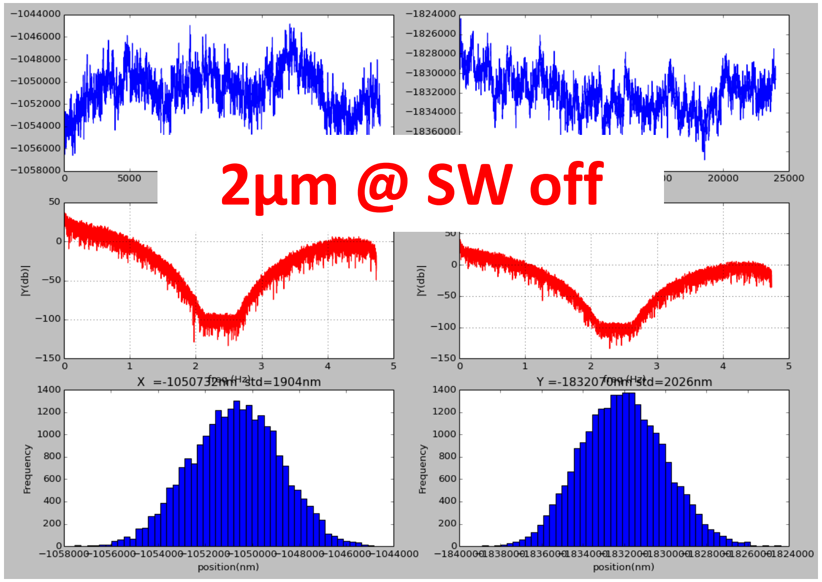
$$X = K_X \times \frac{(A+D)-(B+C)}{\sum(A,B,C,D)} = K_X \times \frac{(A-C)+(D-B)}{\sum(A,B,C,D)}$$

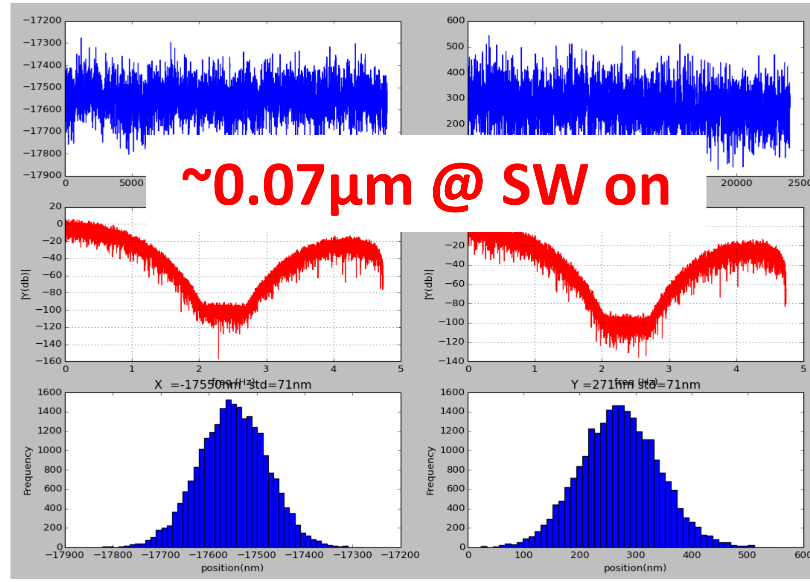
$$Y = K_Y \times \frac{(A+B)-(C+D)}{\sum(A,B,C,D)} = K_Y \times \frac{(A-C)-(D-B)}{\sum(A,B,C,D)}$$

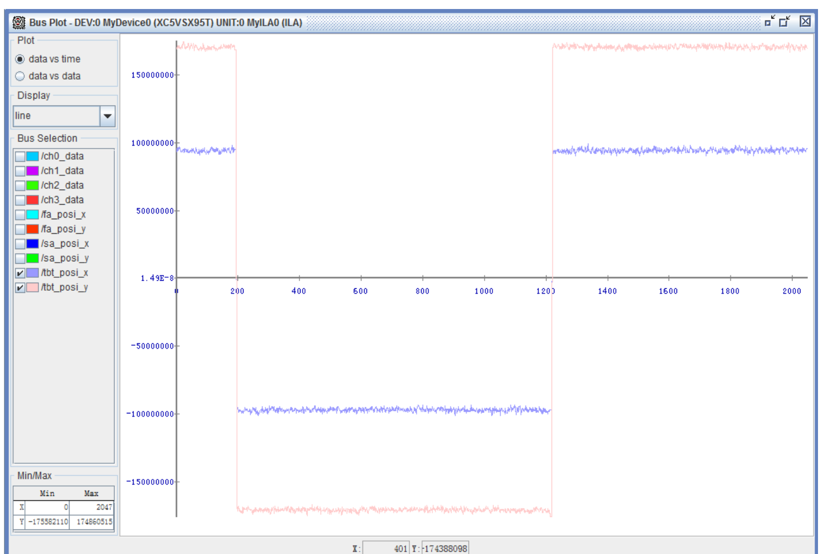


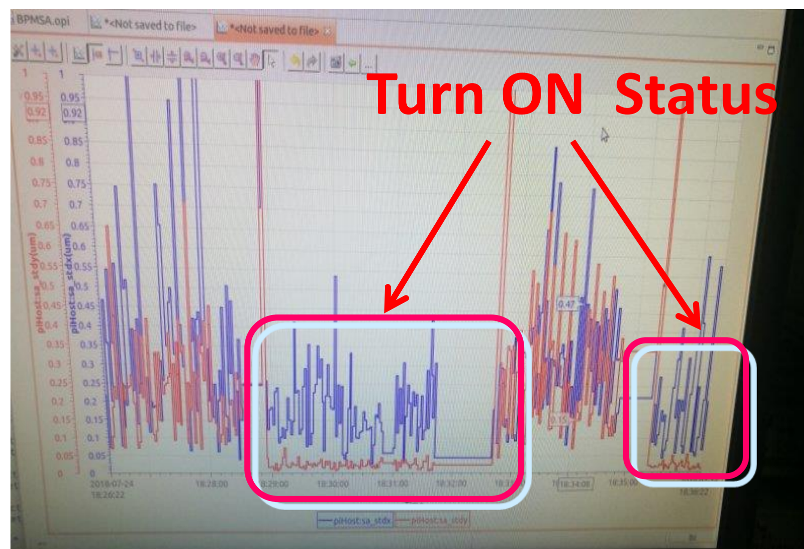


Cross-bar switching circuit testing

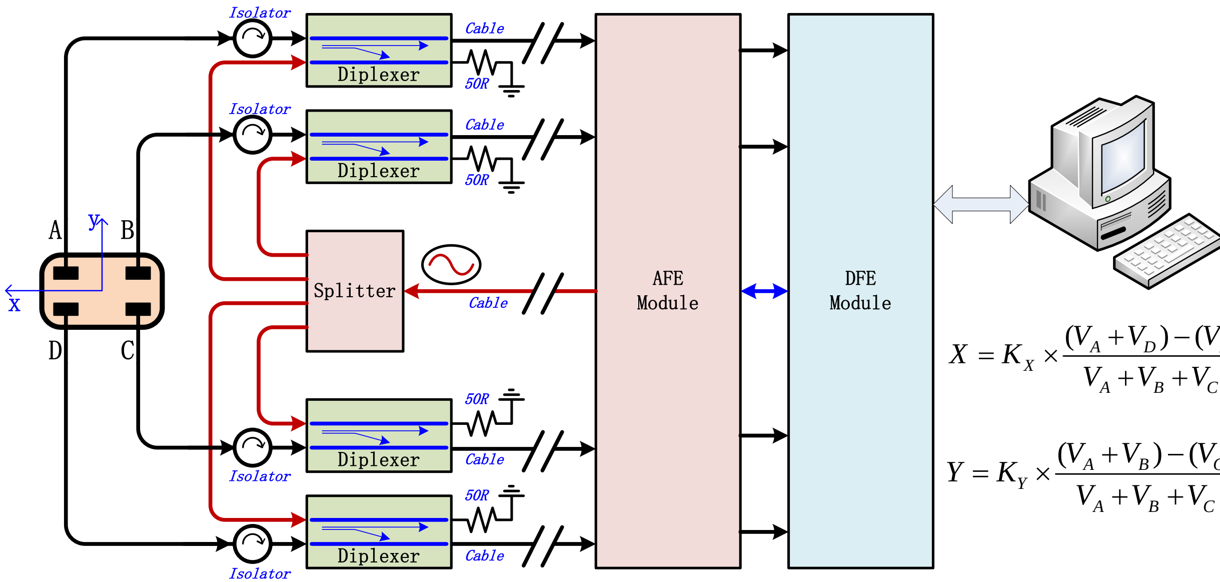








Pilot-Tone scheme



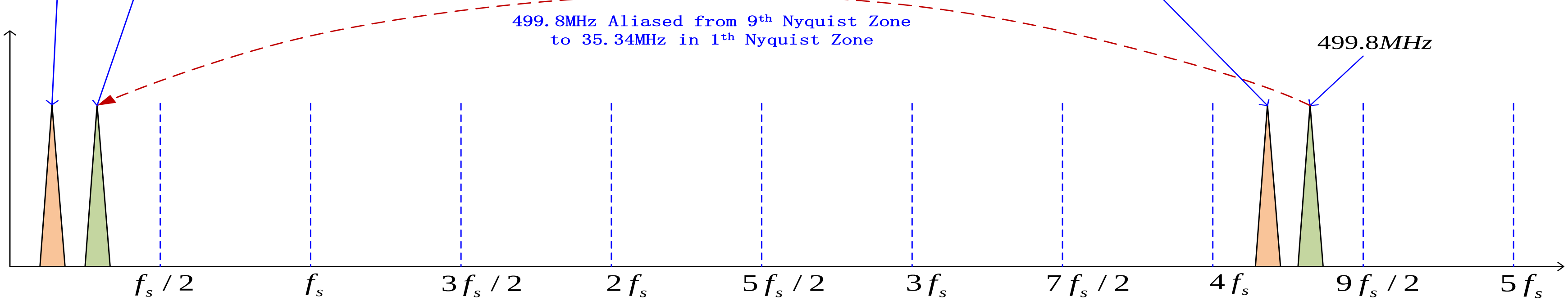
$$X = K_X \times \frac{(V_A + V_D) - (V_B + V_C)}{V_A + V_B + V_C + V_D}$$

$$Y = K_Y \times \frac{(V_A + V_B) - (V_C + V_D)}{V_A + V_B + V_C + V_D}$$

$$f_{Pilot\_Tone\_sample} = \frac{499.8MHz}{396} \times 96 \times 4 - \frac{499.8MHz}{396} \times 92 \times 4 = 20.1939394MHz$$

$$f_{Pilot\_tone} = \frac{499.8MHz}{396} \times 96 \times 4 = 484.654545MHz$$

$$f_{Data\_sample} = 499.8MHz - \frac{499.8MHz}{396} \times 92 \times 4 = 35.339495MHz$$



$$f_{Sample} = \frac{499.8MHz}{396} \times 92 = 116.11515152MHz$$

$$f_{NCO} = \frac{499.8MHz}{396} \times 27.5 = 34.7083333MHz$$

6. Summary and Acknowledgement

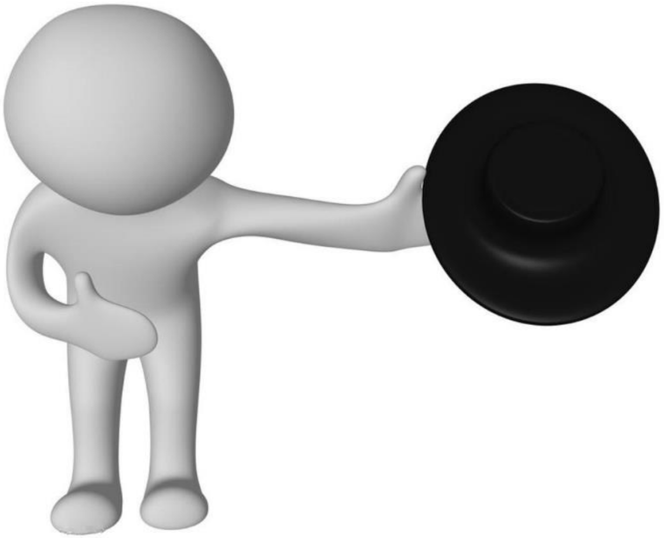
Summary

- Digital BPM Electronics hardware has been designed carefully and had been tested in laboratory;
- The algorithm of BPM based on storage-ring has been developed;
- The digital BPM electronics have been tested with the real beam on BEPCII.
- A lot of work is on the way:
  - The HW, FW are to be optimized and improved;
  - Single pass BPM, BXB BPM is on schedule;
  - BPM's Calibrating and testing system are to be developed.
  - ……

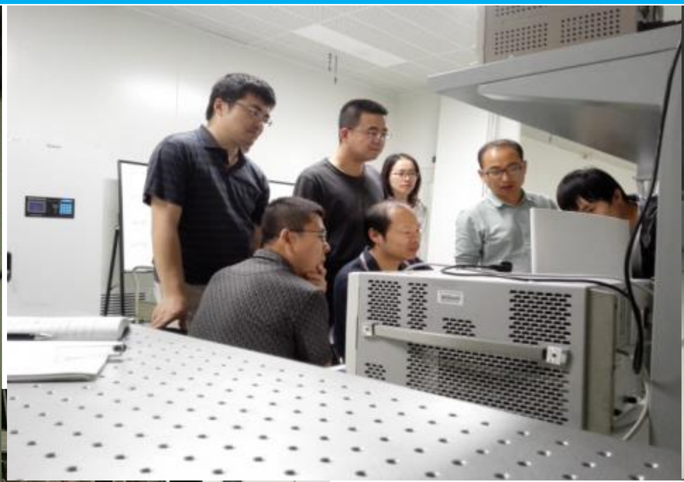
- Welcome to join us, or cooperate with us on the job, thanks you all.

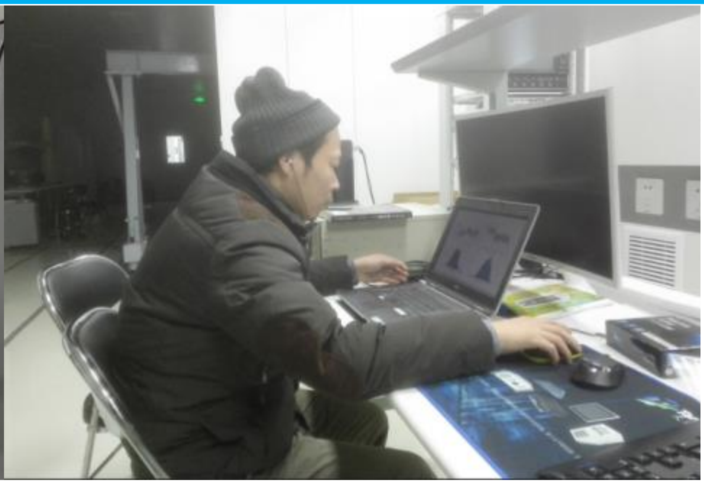
Acknowledgement

- During our Digital BPM electronic development, we got many experts help, and we would like to take this opportunity to express our sincere appreciation to them:
  - NSLSII
  - SIRIUS
  - SSRF
  - HLS
  - I-Tech
  - …



All our member's Hard-work





Thanks for your attention