Next Generation RF BPM Development at NSLS-II

Next Generation Beam Position Acquisition and Feedback Systems Workshop 2018

Nov 12-14, 2018

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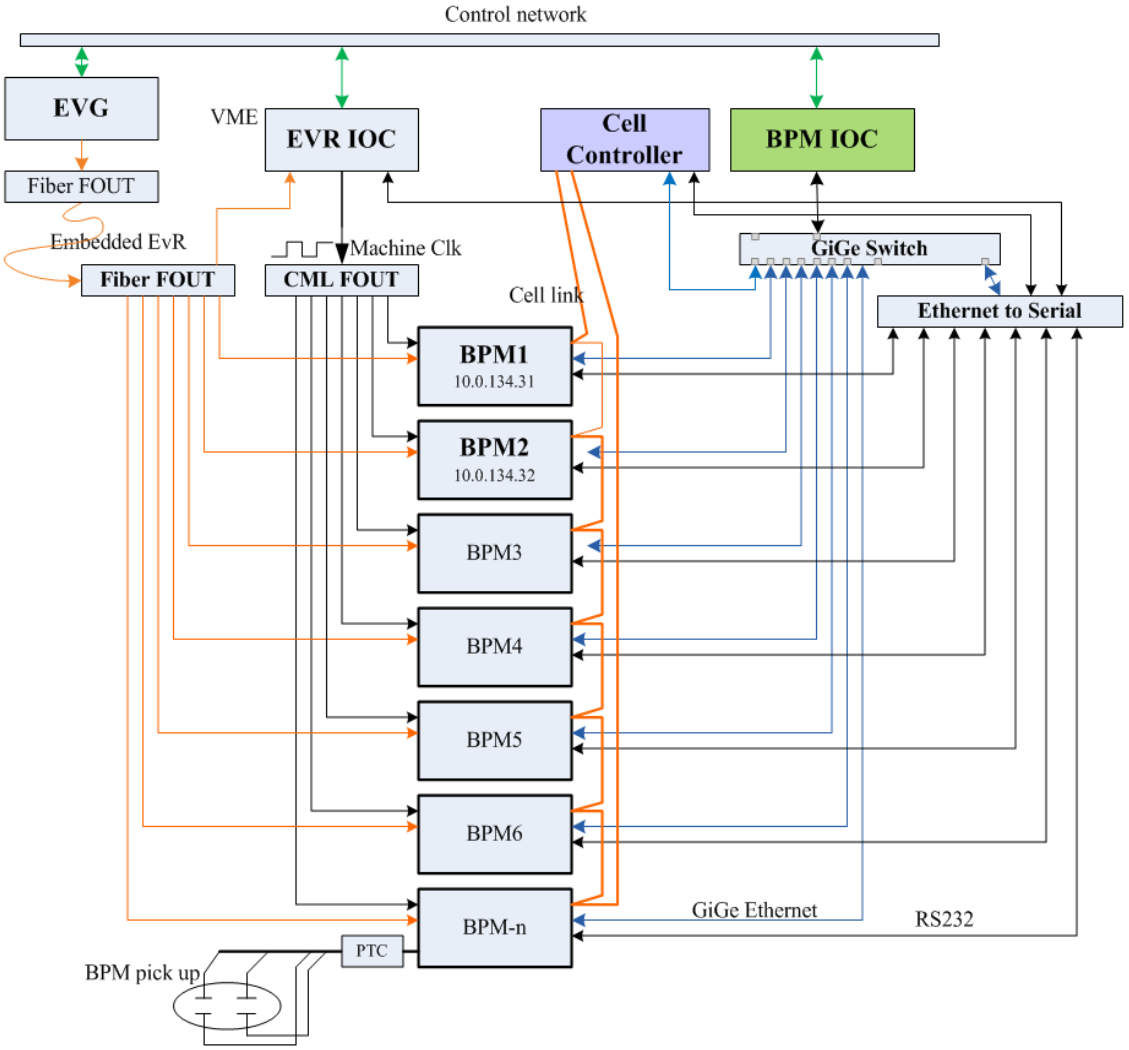
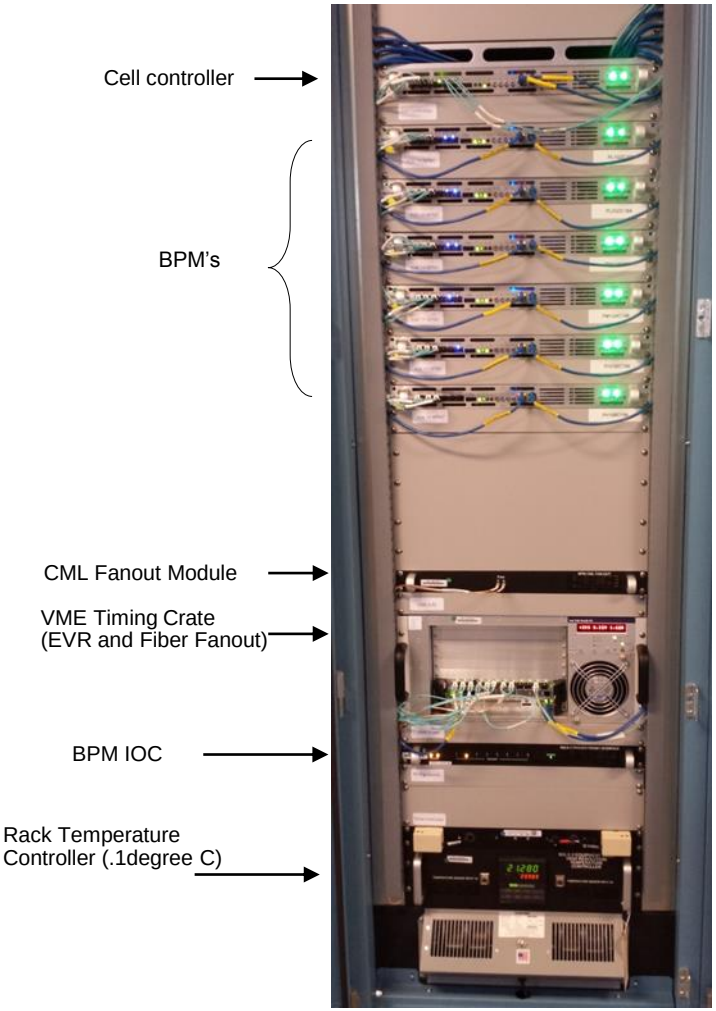
BNL, NSLS-II Diagnostics Group

Outline

1. Existing NSLS-II RFBPM overview
2. NSLS-II BPM upgrade to zDFE
3. AFE Upgrade Considerations
4. zBPM / APS-AFE Design status & Preliminary Performance Test (Collaboration w/APS)
5. BbB BPM overview/status

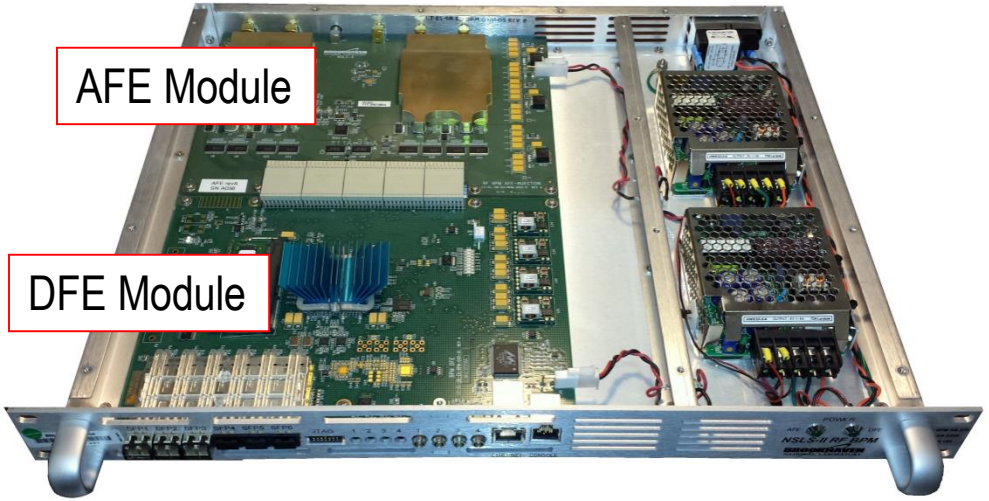
Typical BPM Cell Configuration





NSLS-II BPM Performance Specifications

- Original NSLS-II development
- Resolution specs:
  - ✓ 1 μm turn-by-turn (TbT)
  - ✓ 200 nm in 10 kHz (FA)
  - ✓ Long Term Stability 200nm/8hrs in 10Hz (SA)
  - ✓ Verified with beam
- TbT used for injection & kicked beam studies
- FA for fast orbit feedback & interlocks
- SA for orbit measurements, System Health
- No bunch-by-bunch capability (cannot resolve bunches within a turn)

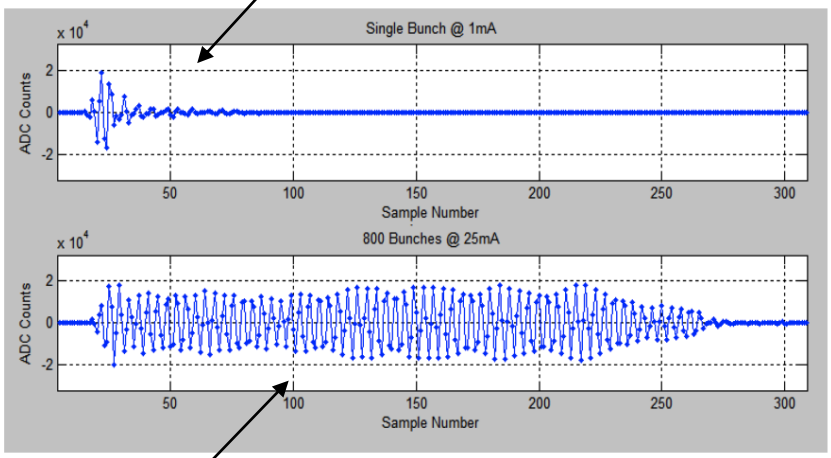


Data Type	Mode	Max Length
ADC Data	On-demand	256Mbytes or 32M samples raw ADC per channel simultaneously
TBT	On-demand	256Mbytes or 5M samples TbT (Frev=378KHz)
FOFB 10KHz	Streaming via SDI Link and On-demand	Streaming - X,Y,SUM ; For On-Demand: 256Mbytes or 5M samples FA (10KHz)
Slow Acquisition 10Hz	Streaming	DDR3 80hr Circular Buffer SA (10Hz)
System Health	Streaming 10Hz	DDR3 80hr circular buffer System Health; AFE temp, DFE temp, FPGA Die temp, PLL lock status, SDI Link status

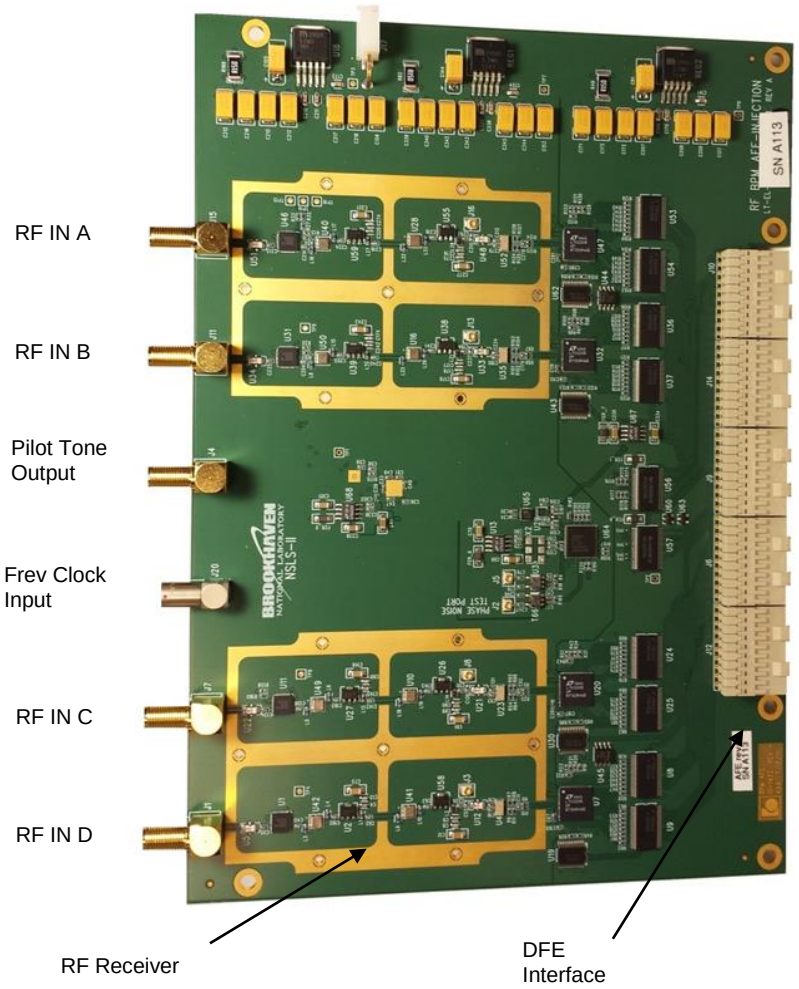
Analog Front End Board (AFE)

- Architecture is based on under-sampling the 500MHz impulse response of band-pass filter.
- Coherent signal processing – ADC clock is locked to Frev.
  - 310 ADC samples per turn

Single Bunch @ 1mA

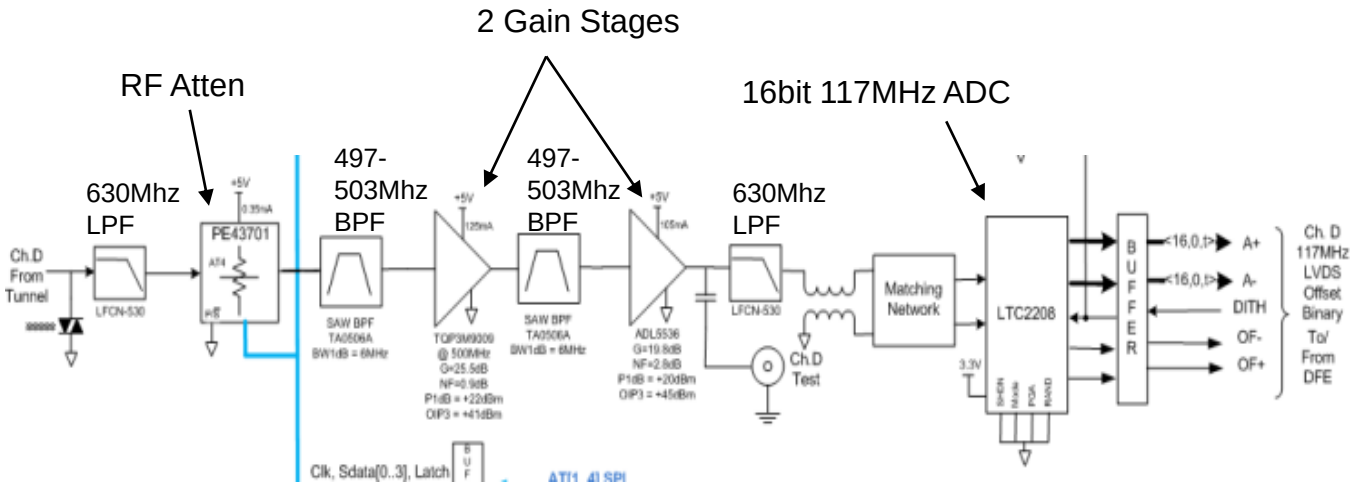


800 Bunches @ 25mA



AFE RF Channel Signal Chain

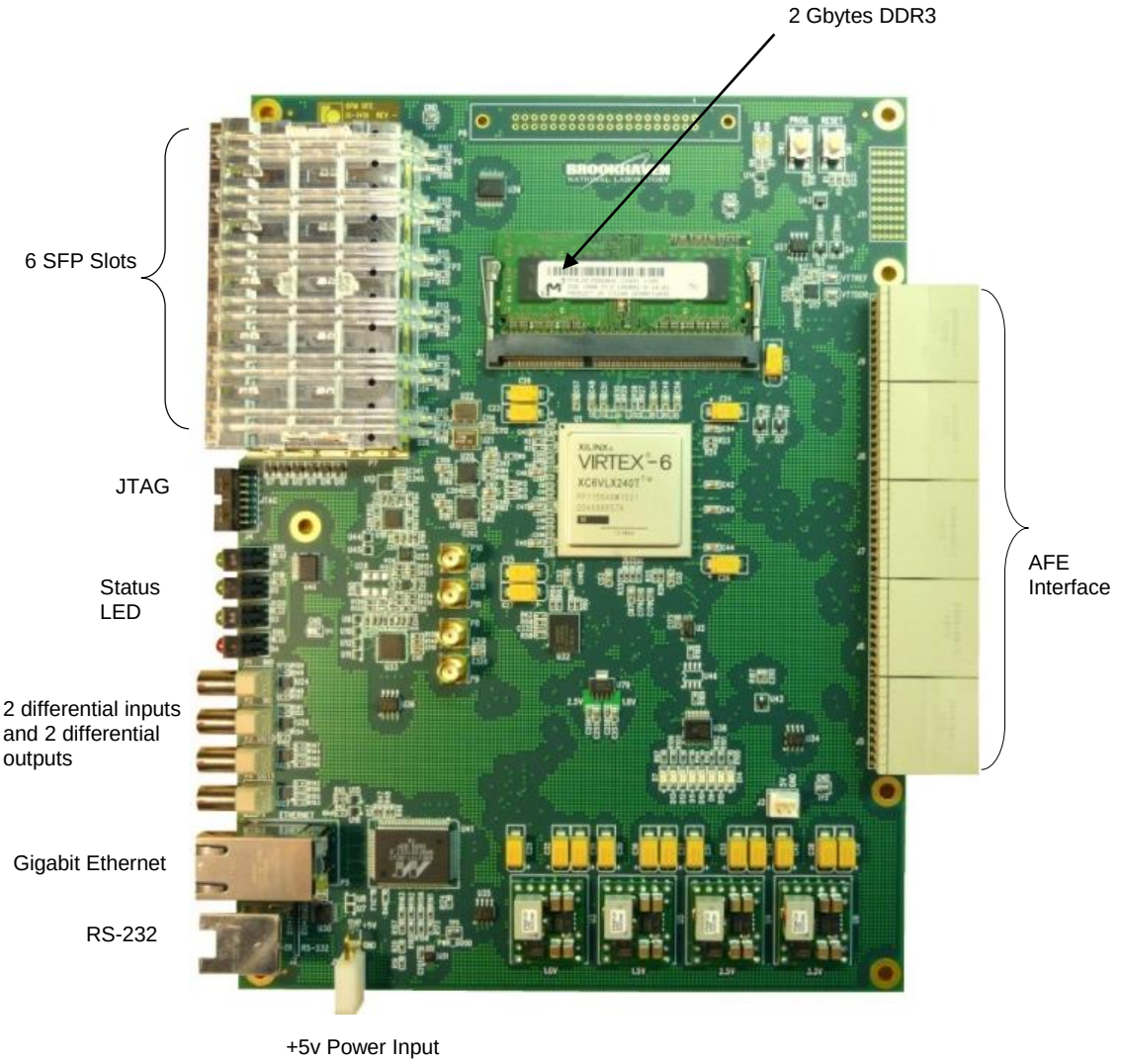
Single Channel Signal Chain



Digital Front End Board (DFE)

Features/Benefits:

- Xilinx Virtex-6 FPGA (LX240T)
- DFT algorithm for beam signal processing
- FW support for DFT, CIC, & FIR for 10kHz
- Embedded MicroBlaze soft core µP
  - Xilkernel OS and lwIP TCP/IP stack
- Gigabit Ethernet
- 2Gbyte DDR3 Memory (SO-DIMM Module)
  - Memory throughput = 6.4 GBytes/sec, which is fast enough to support streaming raw ADC data.
- Six 6.6Gbps SFP modules
  - Embedded Event Receiver
  - Fast Orbit Feedback
- 768 Hard Multipliers in FPGA fabric – Used for FIR filters, position calculations, etc.
- 1Gbit FLASH memory
- Also used as 'cell controller' processor for Fast Orbit Feedback
- Supports two(2) Gate signal processing function (Beam Operation, online lattice characterization)
- Multiple sinewave driving for fast/slow corrector excitation (0-2 kHz sinewave drive via global & SDI links)
- Post Mortem (ADC sum, TBT: X,Y,Sum, FA: X,Y,Sum)
- TBT Glitch Detection



Motivation for BPM Upgrade to zDFE

Deficiencies of existing RF BPM DFE

- The soft-core MicroBlaze processor has limited performance and poor network performance (<20Mbit/sec).
- Xilkernel OS is a non-standard, Xilinx specific, bare-metal operating system with limited support.
- LwIP TCP/IP stack has some reliability issues.
- Software development requires special knowledge of Xilinx kernel OS features and therefore steep learning curve and difficult to maintain as opposed to standard OS such as Linux.
- Hardware obsolescence, existing technology is 9+ years old

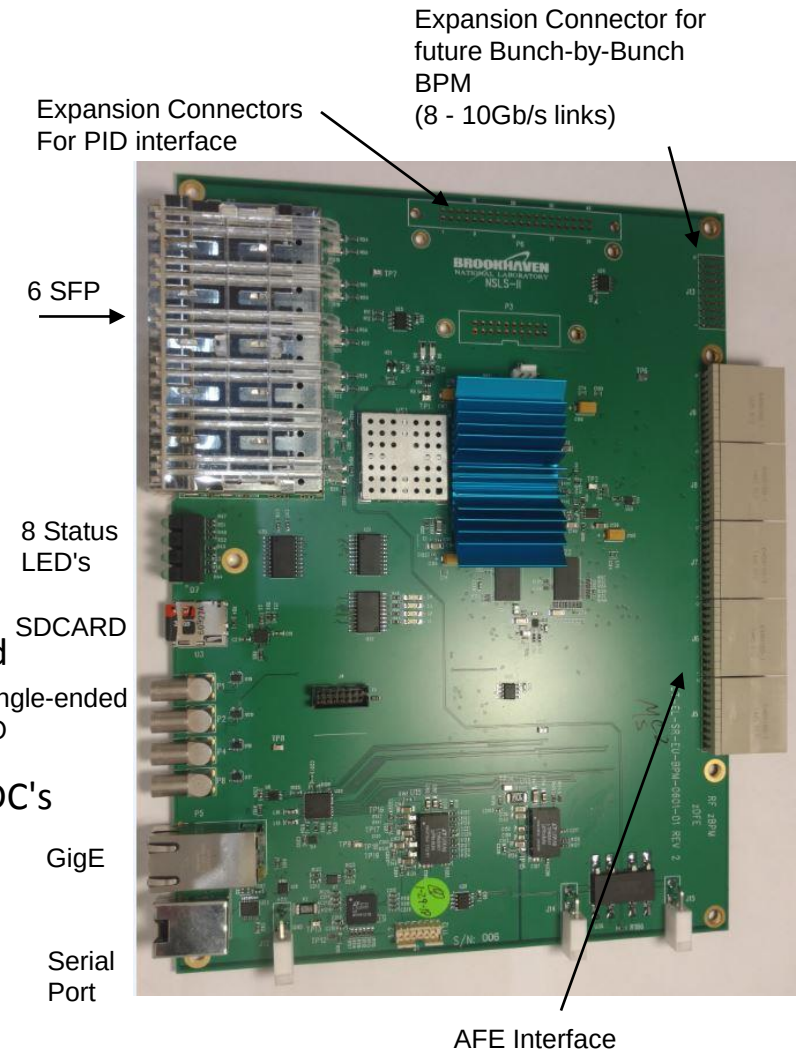
zDFE Improvements vs. Existing RFBPM DFE

- Hard dual-core ARM A9 processor provides >500Mbit/sec throughput. This is a 25x improvement over the existing RFBPM DFE performance.
- Runs standard Debian-7 based Linux Operating System.
- Embedded IOC
- Boot via 32Gbyte micro SD-Card
- DMA Kernal driver for large waveform access
  - Up to 300Mbyte
- Software development is now standard user space applications similar to software development on a standard linux server.
- Long term maintainability and standard software development provide quick learning curve and allow developers easier access to maintain and upgrade software and features.
- Added FPGA resources supporting:
  - Multi-gate signal processing
  - Digital signal processing (DFT, DDC)
  - Single bunch multi harmonic processing for improved resolution

Digital Front End Board (zDFE)

Features/Benefits:

- Faster processing and networking, 500Mbit/sec vs. 10Mbit/sec
- Hardware is backward compatible, use existing AFE and enclosure to minimize upgrade effort and cost
- Standardize to common DFE platform, supporting multiple sub-systems including: RFBPM, BbB-BPM, X-Ray BPM, Cell Controller for Fast Orbit Feed-Back
- Runs standard Debian based Linux Operating System.
- Software development is now standard user space applications similar to software development on a standard linux server.
- Support for Bunch-by-Bunch position calculation
- Integrated 10Gbps transceivers to interface to 500MSPS ADC's



zDFE BPM Performance Specifications

- zBPM Prototype
- Resolution specs:
  - ✓ 1 µm turn-by-turn (TbT)
  - ✓ 200 nm in 10 kHz (FA)
  - ✓ 200nm Long Term Stability /8hrs in 10Hz (SA)
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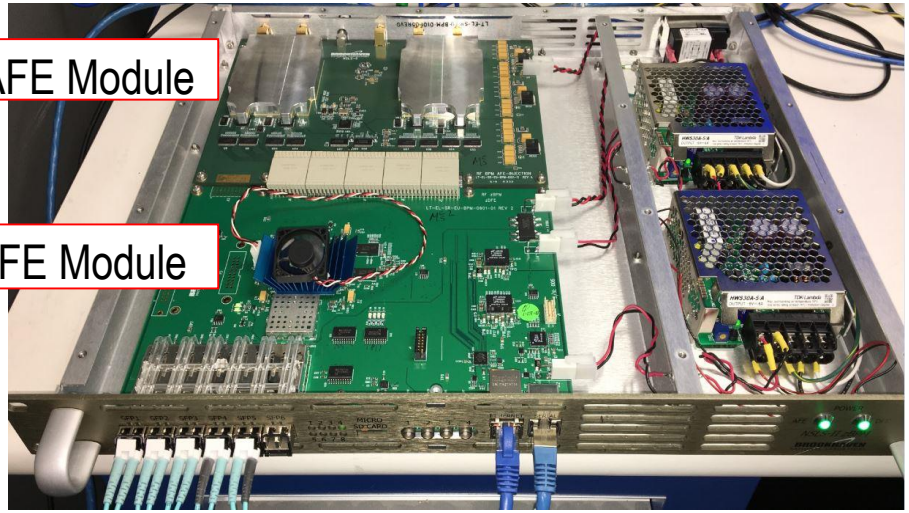


Data Type	Mode	Max Length
ADC Data	On-demand	100Mbytes or 12M samples raw ADC per channel simultaneously
TBT	On-demand	100Mbytes or 2M samples TbT (Frev=378KHz)
FOFB 10KHz	Streaming via SDI Link and On-demand	100Mbytes or 2M samples FA (10KHz)Streaming - X,Y,SUM ; On-Demand:
Slow Acquisition 10Hz	Streaming and On-demand	SD Card based 80hr circular buffer SA (10Hz)
System Health	Streaming	SD Card based 80hr circular buffer System Health; AFE temp, DFE temp, FPGA Die temp, PLL lock status, SDI Link status

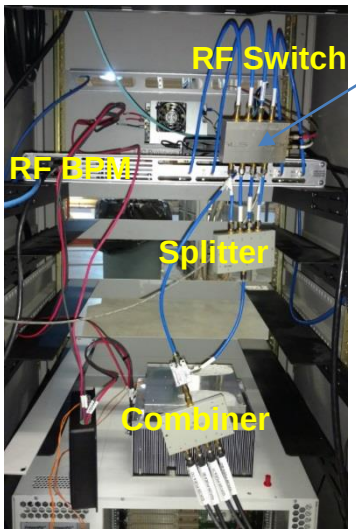
Upgrade Considerations for AFE

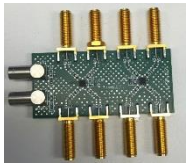
- Temperature Control
  - Present use of temp control racks (+/- .1deg C)
    - Achieve 200nm long term stability
    - 1 – 3 um/degree C
  - Investigate use of Peltier cooling for temperature regulation
    - Eliminate dependence on temp control racks
- RF Switching
  - 4-way switch presently implemented in Libera B+
    - Achieve <50nm long term stability
  - 2-Way switch presently Implemented in the Sirius BPM
    - Diagonal switch simplifies application
    - Achieve <50nm long term stability
  - NSLS-II New AFE Design implementation of 2-Way switch
    - Diagonal switch simplifies application
    - Achieve <50nm long term stability
    - Collaboration with APS, Brazilian LS
- Pilot Tone
  - Presently design custom diplexer developed by K&L Microwave for injection and combining of Out-of-Band Pilot-Tone
  - Temperature dependent band pass response of existing SAW filters on RFBPM AFE, prevented successful implementation.

zBPM System Integration Test Config

- MC28RG-G1 BPM Development Rack
  - Temperature Controlled to .1 degC
  - Standard NSLS-II Timing System
  - Dedicated PUE for testing
  - Dedicated NSLS-II Cell Controllers
- Mobile Cell RF Switch Prototype Test
  Instrument RFBPM AFE w/external RF Switch box
  Diagonal Button signals switch (A/C, B/D)

Mobile Cell

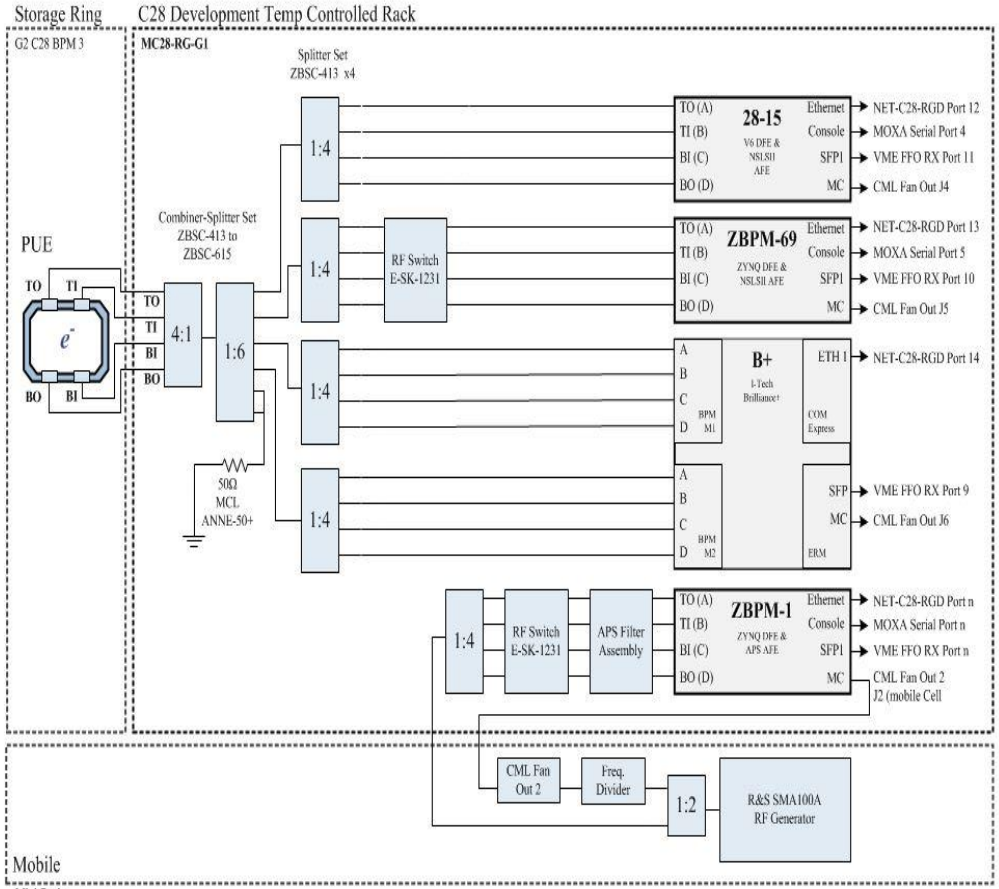




MC28RG-G1

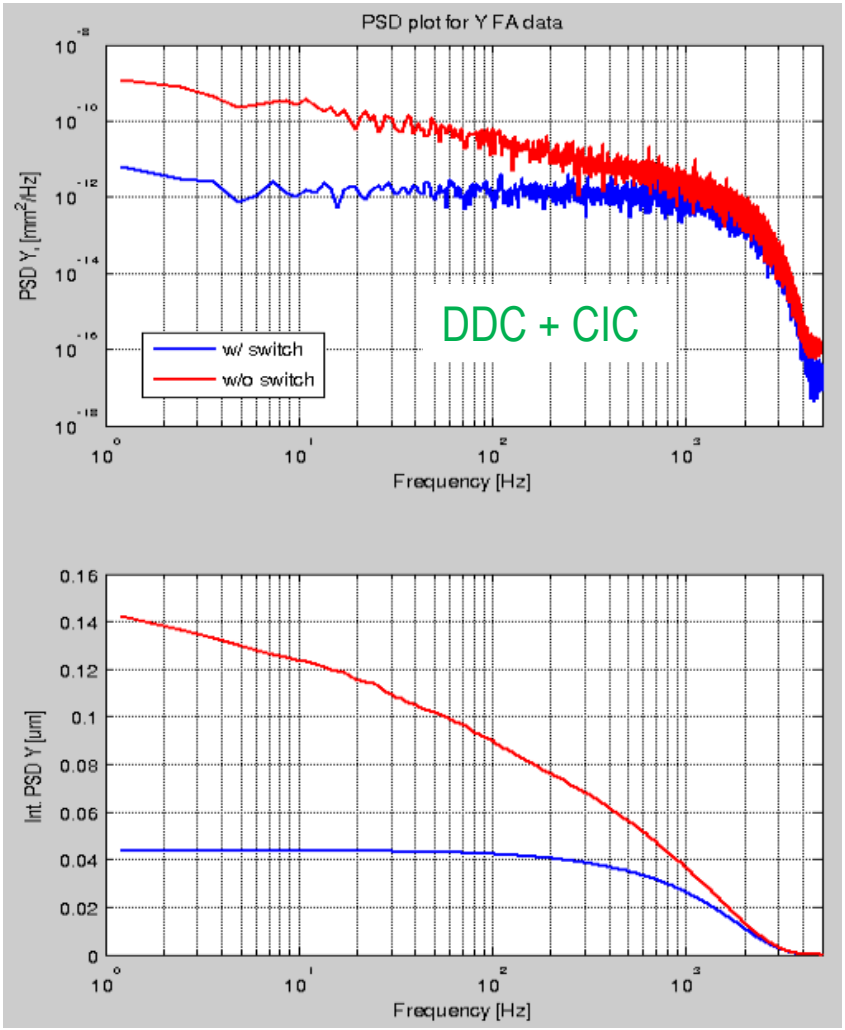
Diagnostics R&D C28
Development Setup
Version 5, M. Maggipinto
11/9/2018

LI	Device	Desciption	IP	User	Password	Moxa IP	Moxa Port
1	28-15	V6 BPM	10.0.142.233			10.0.132.42	4004
2	ZBPM-69	ZYNQ BPM	10.0.153.69			n/a	n/a
3	B+	Libera Brilliance +	10.0.143.195			n/a	n/a
4	ZBPM-1	APS BPM	10.0.153.29			n/a	n/a



FA 10 kHz PSD plot

Short-term stability



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- FA 10 kHz PSD plot
- With RFSW switching (Blue)
- Without switching(Red)
- W/O RFSW switching, FA achieve 140nm
- W RFSW switching, FA achieve 40nm

Long-term Test result (2-Days)

- V6 BPM existing BPM (red: 130/126 nm)
  - Installed temperature controlled rack (+/-0.1 degree C)
- zBPM (blue: 10.5/20.0 nm)
  - Mezanine area temperature (+/-0.5 degree C)
  - Diagonal RF switching enabled
- Both are the same pick-up signal from button->combiner->splitter)
- Beam 400 mA

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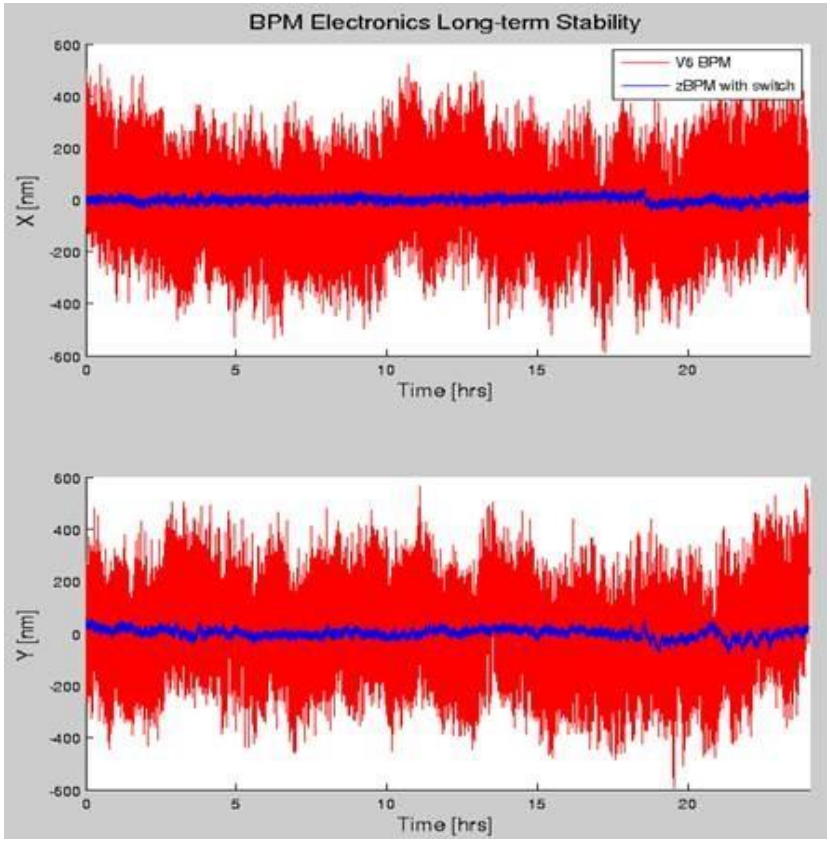
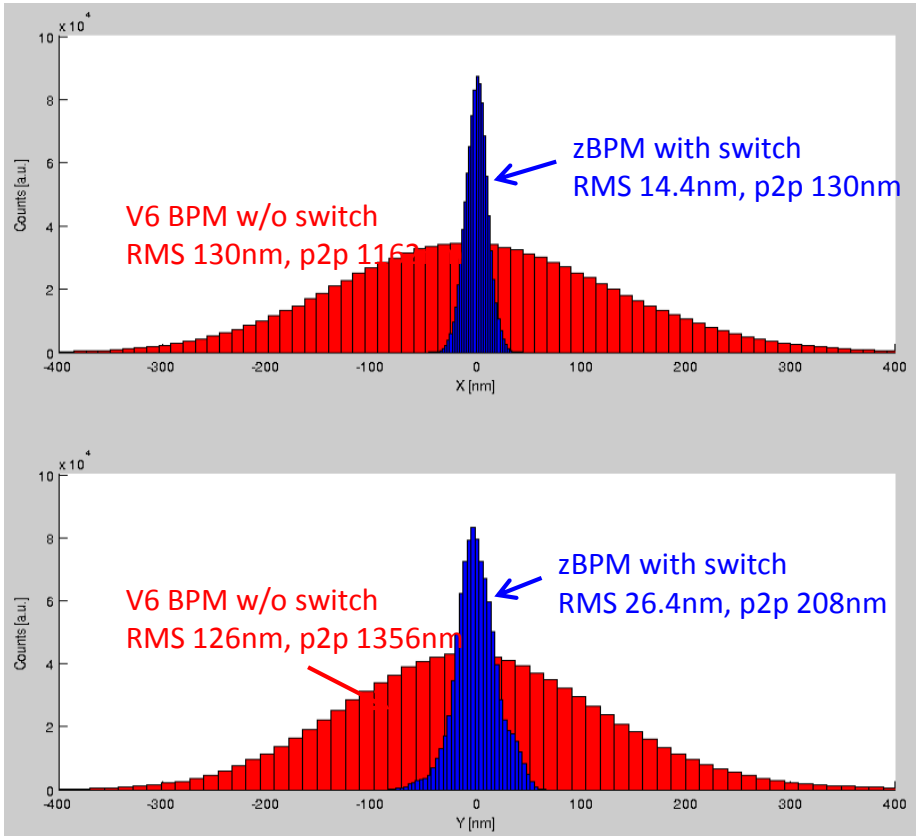
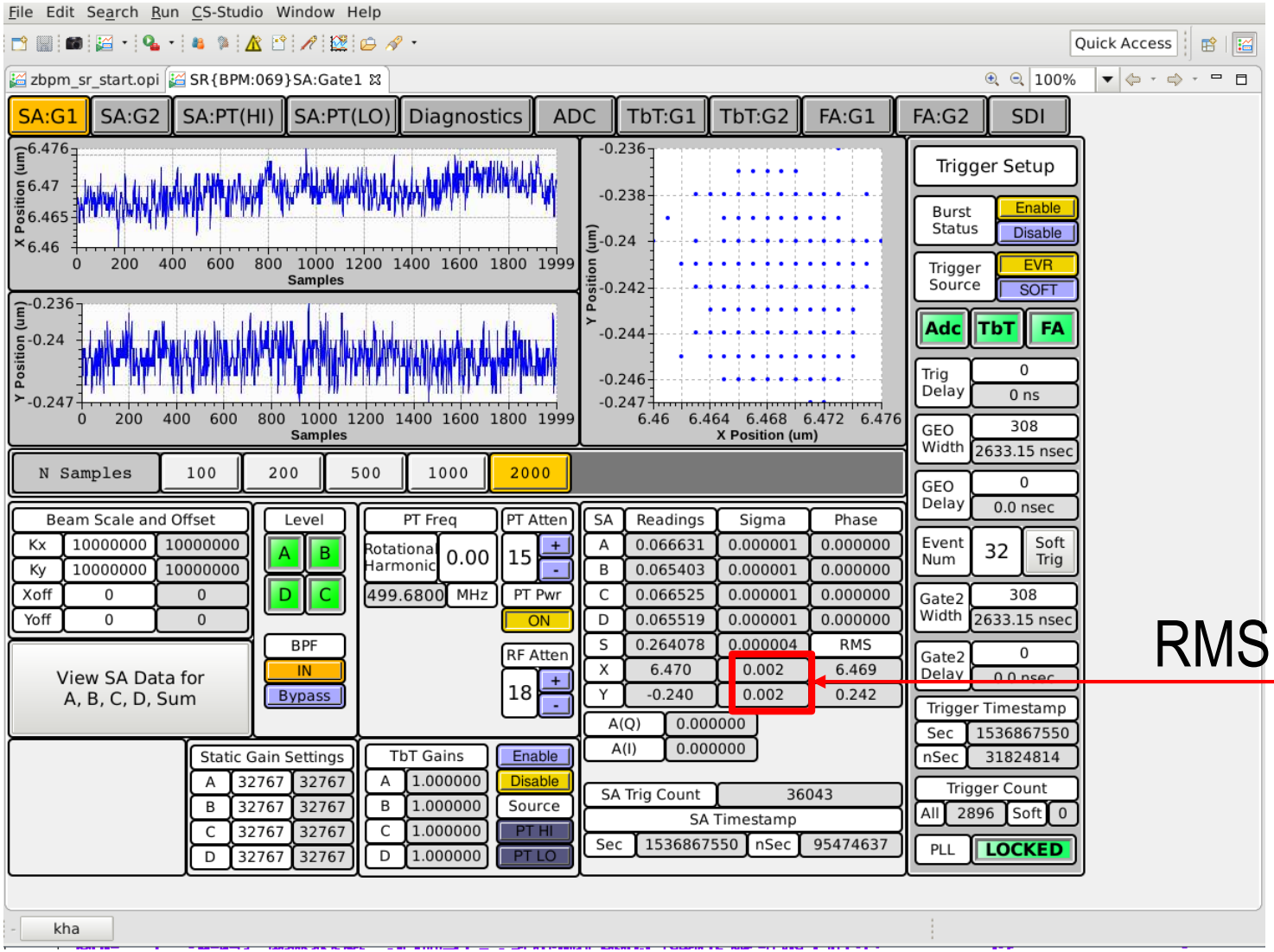




CSS Top Panel SA 2kSec (w/Switch)



RMS 2 nm

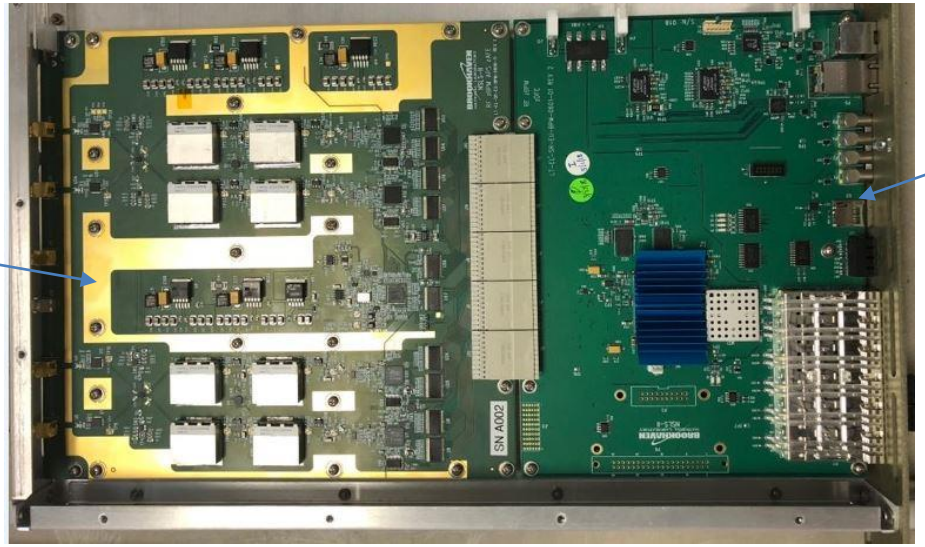
Look Ahead: Next Generation AFE

- RF BPM AFE Development
  - ✓ Support Active (PT Based) Calibration (Possible to Collaborate with ALS)
  - ✓ Implement 2-way Analog switching
  - ✓ Non-Dependence on Temperature controlled rack
  - ✓ Improve Long Term Stability
- RF BPM DFE Development
  - ✓ FPGA upgrade to Xilinx Zynq UltraScale+
- BbB zAFE Development
  - ✓ 500Msps 14/16 Bit ADC(ADS54J66,ADS54J69) resolve bunches within a turn (BbB position data)

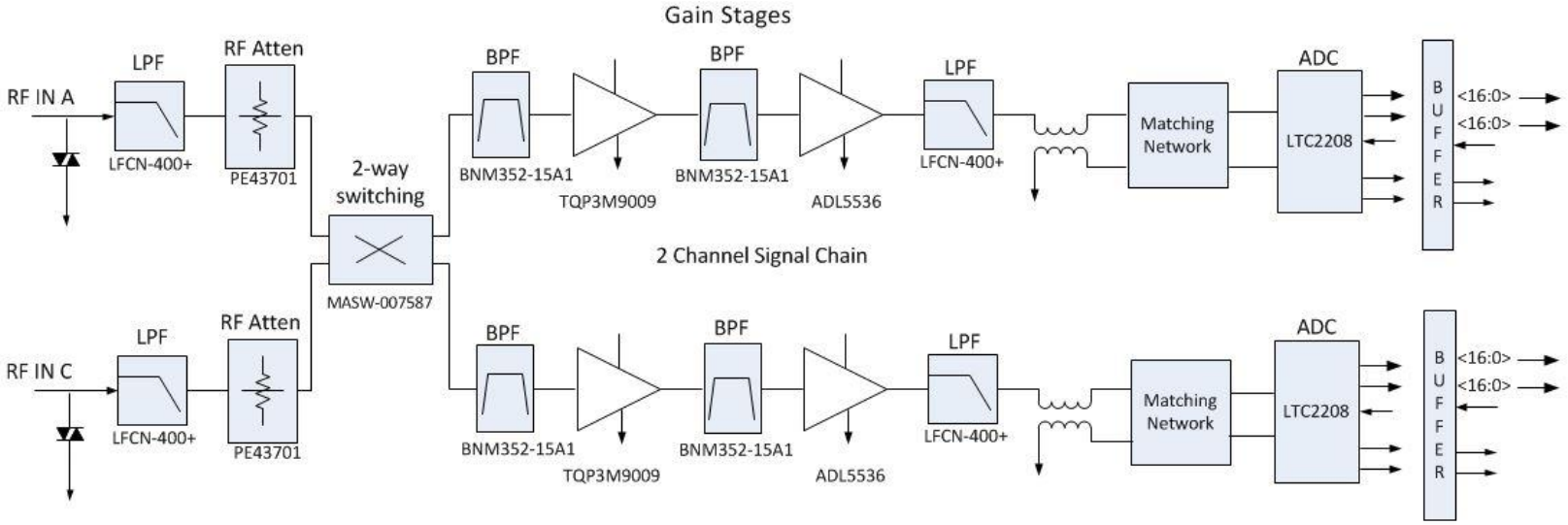
RF BPM APS AFE Prototype

zDFE/AFE BPM Chassis

AFE Prototype



APS-AFE Prototype Block Diagram



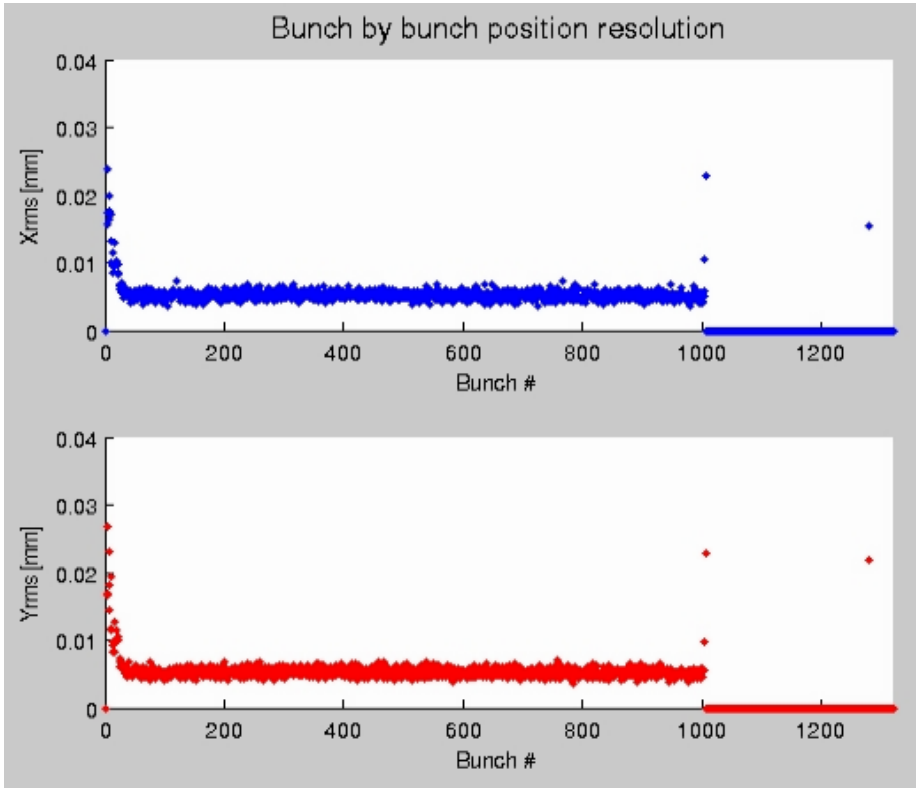
BbB BPM Electronics

- **Motivation is to design a single BPM electronics module that can simultaneously perform bunch by bunch position measurements while also improving turn by turn position results over traditional subsampling architectures.**
  - **Strong physics interest for BbB capability at multiple BPM locations.**
- **Due to advances in ADC technology in the past few years this is now possible.**
  - **TI AD54J66: Quad Channel, 14-bit, 500Msps ADC ($600)**
  - **TI ADS54J69: Dual Channel, 16-bit, 500Msps ADC ($600)**
- **Latest advances in FPGA technology could provide single chip solution**
  - **Xilinx RFSoC FPGA : 8 channel, 12-bit, 4Gsps.**
  - **Xilinx 2nd Gen RFSoC FPGA : 8 channel, 14-bit, 5Gsps**

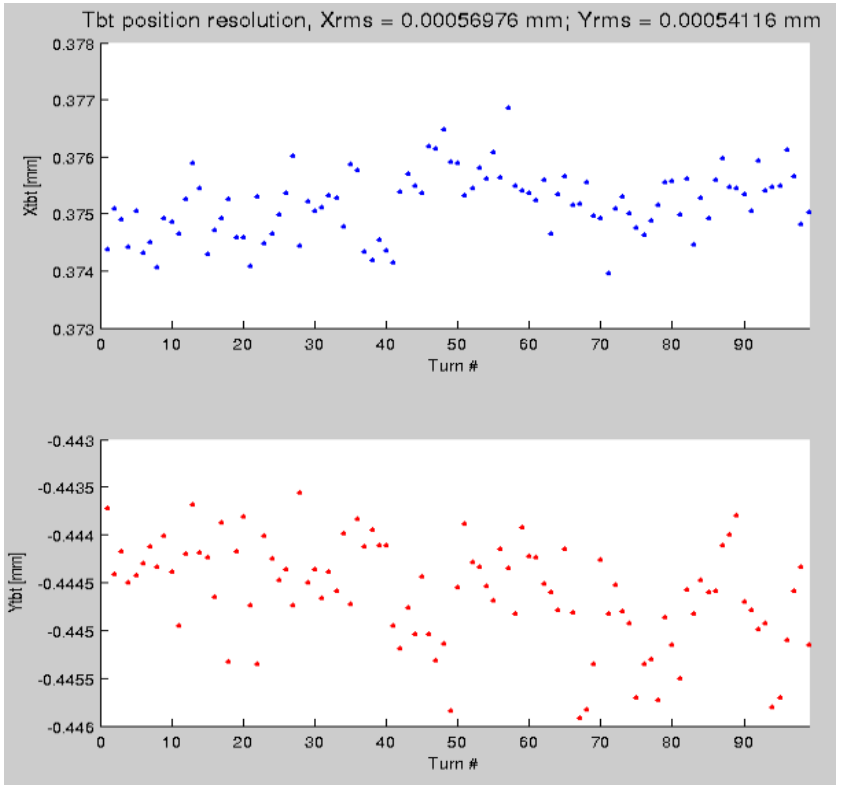
BbB Evaluation Results

- **Hardware for evaluation was TI ADS54J66 (Quad 500Msps,14-bit ADC) evaluation board connected to a Xilinx Zynq ZC706 evaluation board.**
- **Beam Test with 325mA user beam, 1000 bunches (0.3mA bunch current)**
- **Combiner / splitter setup to remove beam motion, +20dB amplifier before ADC**

~5um BxB position resolution

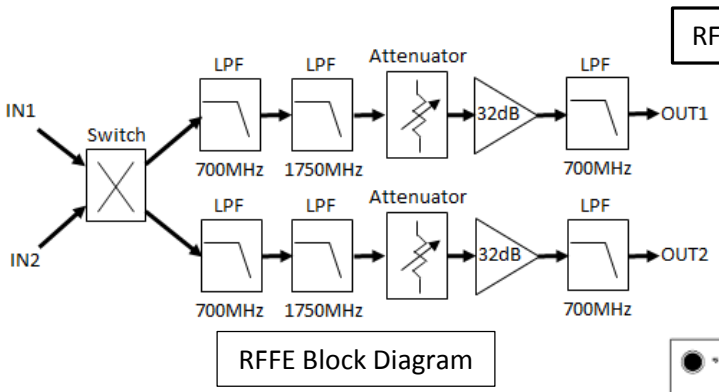


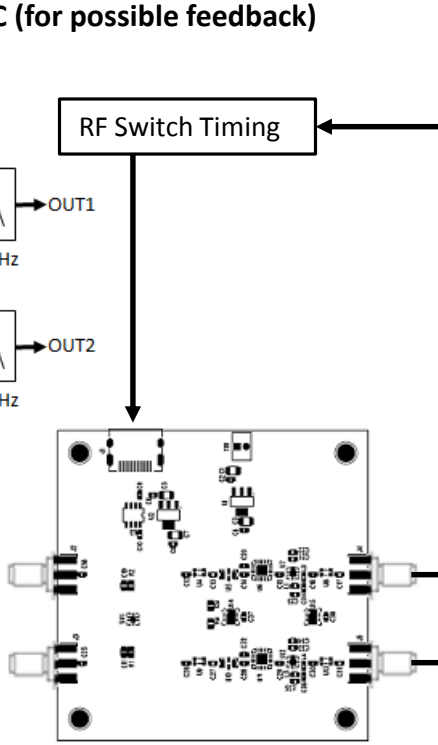
~0.6um TbT position resolution



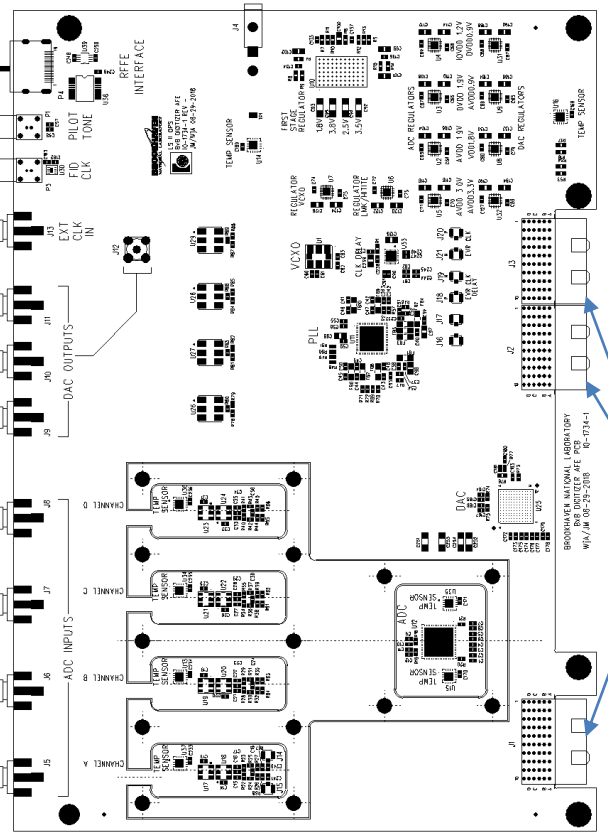
BbB Hardware

- **Based on promising preliminary results with evaluation hardware, decision to move forward with custom hardware**
  - **RFFE Front end board**
  - **Digitizer Board (pcb in fabrication)**
    - **4 channel 500Msps ADC**
    - **4 channel 500Msps DAC (for possible feedback)**





Digitizer Board



Connects to existing zDFE board

Summary

- Digital Front End (DFE) Improvements
  - RFBPM zDFE board is completed, and fully functional for NSLS-II application
  - Improved performance with new DSP signal processing algorithm
  - Use of Newer Xilinx/Vivado development environment and embedded EPICS IOC
  - Implementation of Embedded Debian Linux operating system for ARM dual core processor
  - Developed a Linux DMA driver for DDR3 memory access (ADC, TBT, FA)
  - Expanded application for the Cell controller, AI system, BbB & BPM system as well as beamline applications

- Analog Front End (AFE) Improvements
  - Improved performance using RF switching
    - Initial test results indicate >5x long term stability improvement
  - Evaluating Peltier cooling option as alternative to temperature controlled rack
  - Future support for Pilot Tone(PT) signal processing for active calibration with better BPF

BPM Development Team

Dan Padrazo (Project Manager)

Weixing Cheng (Physics)

Kiman Ha (Embedded Controls, EPICS/IOC, FPGA)

Joe Mead (FPGA, DSP, DFE Board Design)

Tony Caracappa (Embedded Controls, EPICS/IOC, AFE)

Bel Bacha (RF)

Bernard Kosciuk (Mechanical, Thermal Analysis)

Marshall Maggipinto (Technical Support)

Chris Danneil (Technical Support)

John Bohenek (DFE Board Design)

John Kuczewski (Embedded Controls, Linux Kernel)

Acknowledgements

Contributions to this presentation:

Weixing Cheng, Kiman Ha, Joe Mead, Tony Caracappa, Marshall Maggipinto

zDFE Configuration Test:

Weixing Cheng, Kiman Ha, Tony Caracappa, Joe Mead, Marshall Maggipinto, Chris Danneil, Bel Bacha

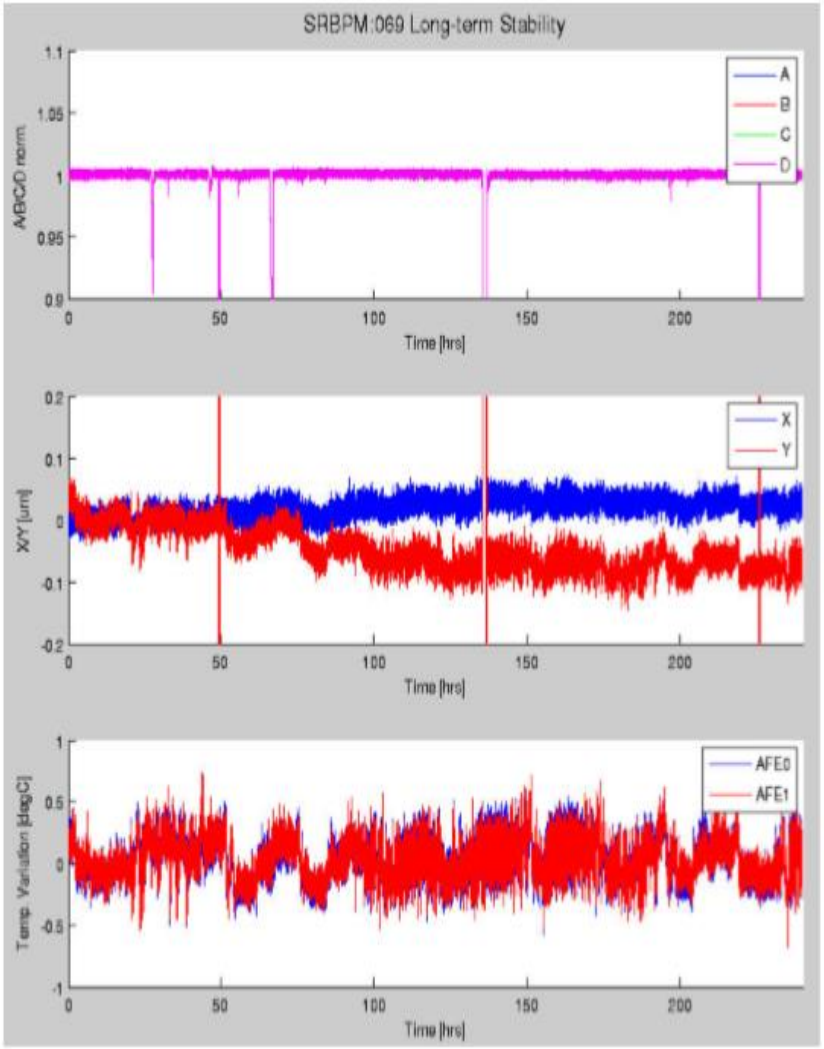
zBPM Integration Testing:

Weixing Cheng, Kiman Ha, Tony Caracappa, Joe Mead, John Kuczewski, Bel Bacha, Marshall Maggipinto, Chris Danneil

Thank You for Your Attention!

Backup Slides

RF-SW BPM Long-term (10 days)



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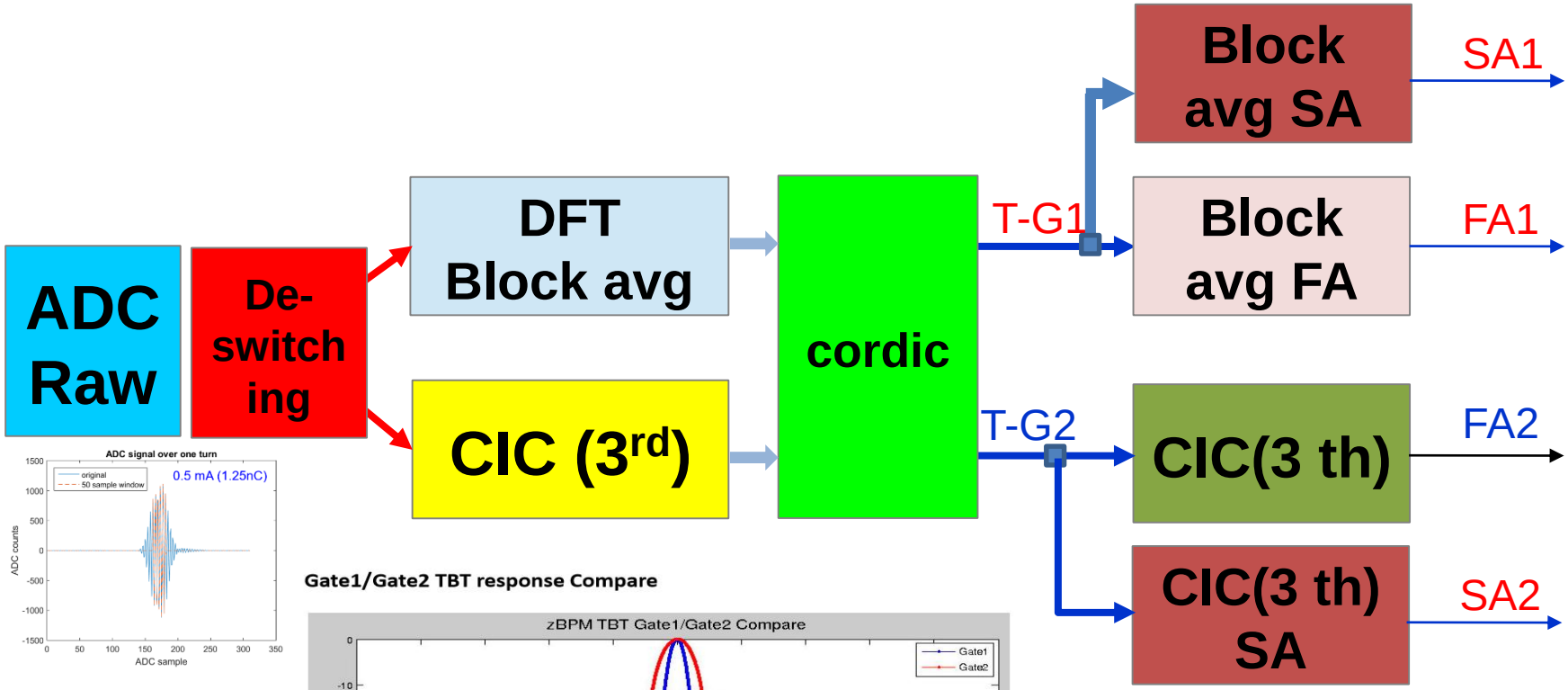
- 10 days long-term, Non temperature controlled rack
- 400 mA operation
- Gate 1: DDC
- Std(x) = 0.0146 um, p2p 0.1192um
- Std(y) = 0.0336um, p2p 0.2121um
- Std(AFE0) = 0.0363 deg, p2p 0.3267 deg
- Gate 2: DFT
- Std(x) = 0.0195 um, p2p 0.1681um
- Std(y) = 0.0440 um, p2p 0.2913um
- Std(AFE0) = 0.1741 deg, p2p 1.36 deg

Signal processing block



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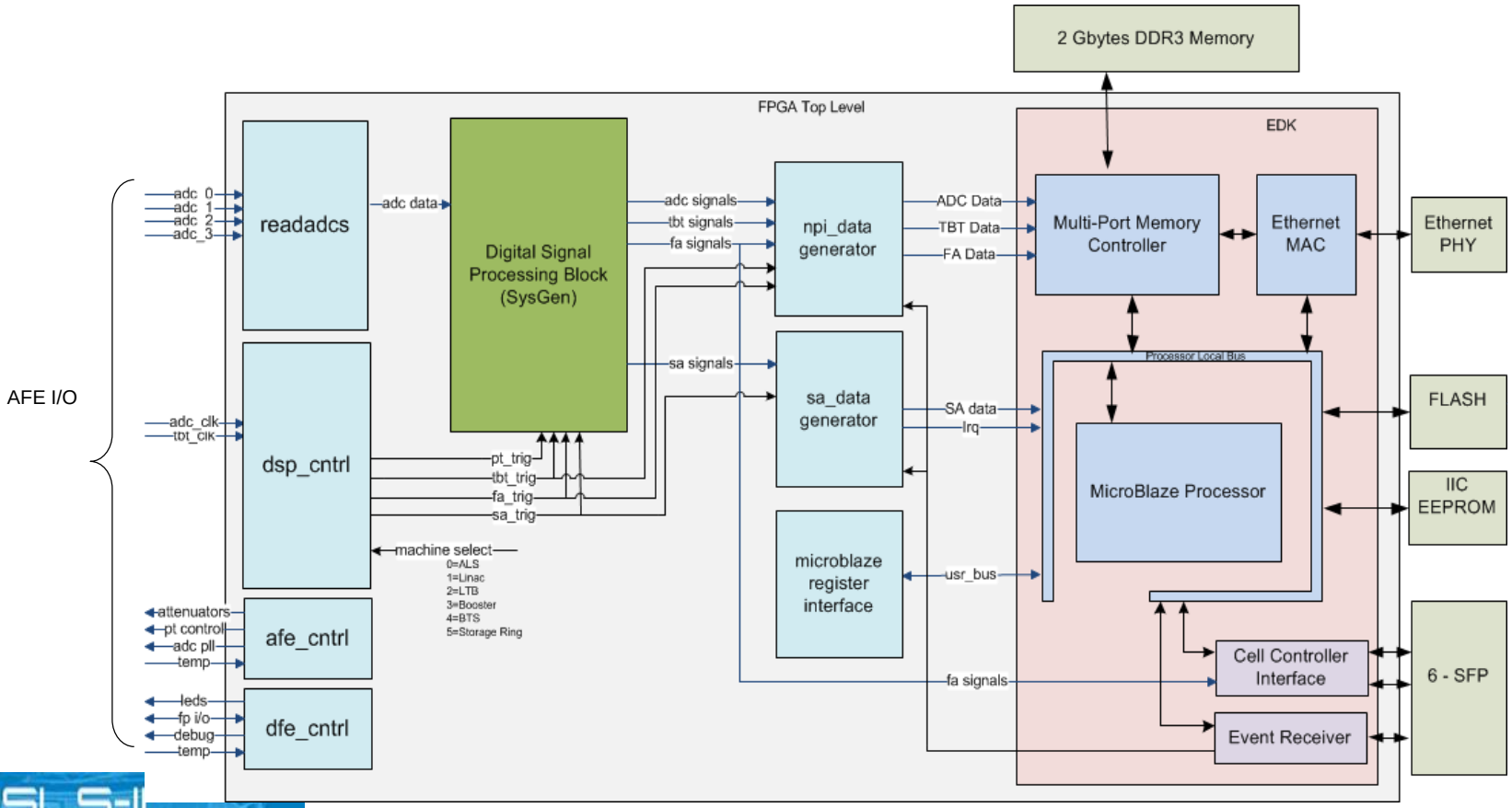
DFE FPGA Block

- FPGA implemented using a combination of VHDL, Verilog, System Generator (for DSP Block) and EDK for MicroBlaze processor
- 2 main data paths
  - Non Deterministic : ADC, TbT, FA, SA data to DDR memory and then to IOC via Microblaze ProcessorFPGA (Ethernet)
  - Deterministic : FA data to Cell Controller for FOFB and Active Interlock (Fiber Optic)



Active Calibration Options, PT

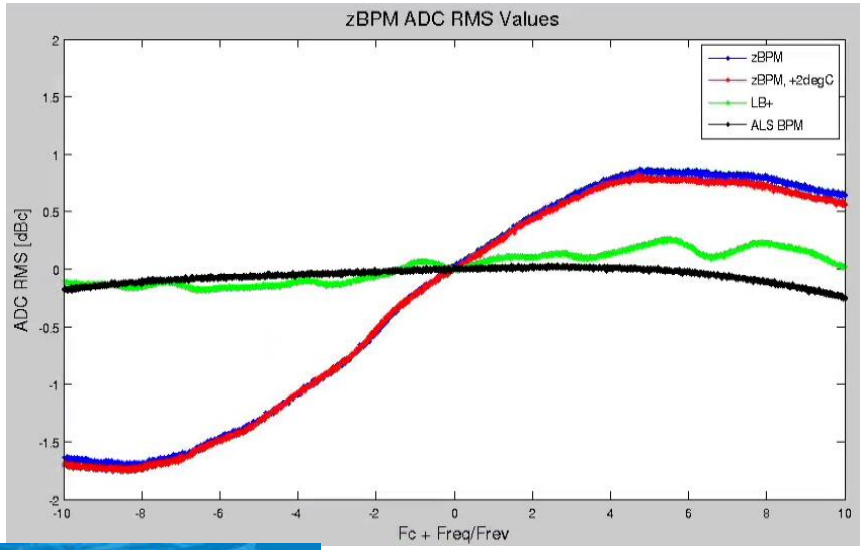
- Initial concept, use custom diplexer developed by K&L Microwave for injection and combining of Out-of-Band Pilot-Tone
  - Alternate In-Band Pilot-Tone calibration using integrated microwave Stripline coupler assembly in place of Diplexer assembly.
- Temperature dependent band pass response of existing SAW filters on RFBPM AFE, prevented successful implementation.

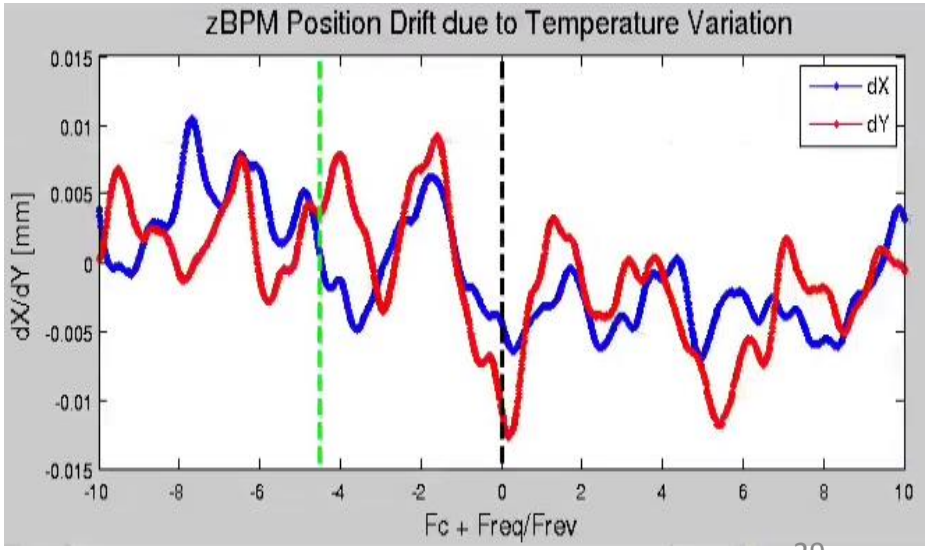
NSLS-II AFE SAW BPF has large gain variation within passband, and it's sensitive to temperature variation.

Pilot tone and beam signals see different in position changes, while temperature varies.

Ceramic BPF helps a lot (ALS) allows pilot tone calibration.

Pilot tone (@-4.5*Frev) and beam see different position drifts. Positions calculated from $g_a/g_b/g_c/g_d$.





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- FPGA implemented using a combination of VHDL, Verilog, System Generator (for DSP Block)
- 2 main data paths
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