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Boris Keil :: Paul Scherrer Institut

The SLS2 RF BPM and Fast Orbit Feedback System

ARIES Workshop, ALBA/Spain, November 12-14, 2018

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- **Introduction**
- **Present SLS BPMs & FOFB**
- **Future SLS BPMs**
- **Future SLS FOFB**
- **Summary & Outlook**

Introduction: SLS2

Parameter	SLS1	SLS2
Beam Energy	2.4 GeV	
Beam Current	400mA top-up (Δ ~ 1mA)	
# Straight Sections	12	
Circumference	288 m	290.4 m
Ɛx	5 nm rad	0.1 nm rad
Ɛy	1...10 pm rad	<10 pm rad
Integral of absolute bending angle	360°	561° (anti-bends!)
Beam pipe aperture (typical)	65mm x 32mm octagonal (+antechamber)	20mm round (+antechamber)

- New low-emittance electron storage ring. More magnets & BPMs.
- Re-using SLS1 linac, booster, building. But: Many renewals needed (most SLS1 systems, infrastructure, building nearly 20 years old ...).

Introduction: SLS2 BPM Specification

Parameter	Value	Beam Current / Filling Pattern
Position Noise (1 kHz BW)	<50 nm RMS	nominal
Position Noise (0.5 MHz BW)	<1000 nm RMS	nominal
	<50 um RMS	1mA single bunch
Position Drift (for constant beam current and filling pattern), electronics only	<100 nm / hour	nominal
	<400 nm / week	nominal
	<1000 nm / year	nominal
Position Drift (mechanics only, for top-up operation mode and standard tunnel temperature stability)	<100 nm / hour	nominal
	<400 nm / week	nominal
	<1000 nm / year	nominal
Beam current dependence for constant filling pattern	<100 nm / 1%	nominal

See SLS2 CDR
http://ados.web.psi.ch/SLS2/CDR/Doc/cdr.pdf

Introduction: SLS2 Status & Schedule

SLS2 project status:

- Conceptual design report done. TDR due 2019.
- Funding (~100 MCHF) likely but not yet approved.
- Main funding phase 2021-2024
- So far: Moderate funding for preparatory R&D.
- Most systems still in early concept/design phase, including new BPMs & fast orbit feedback (FOFB)

SLS2 schedule:

- Last SLS1 beam 3/2023
- Start of SLS2 beam commissioning Q2/2024
- SLS2 pilot experiments Q4/2024
- Rather short time for SLS2 accelerator commissioning -> aiming to test & commission critical SLS2 systems already at SLS1 where possible (e.g. new BPM & FOFB components).

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Present (Old) SLS BPM & FOFB System

- BPM and Fast Orbit Feedback (FOFB) ~20 years old. BPMs: 500 MHz -> 36 MHz IF, undersampled by 12-bit ADCs @ 32MSPS. Intersil Digital Downconverters. DSPs from 1990s. All VME64x.
- BPM & FOFB spare part situation & MTBF still O.K., not reason for urgent upgrade.
- Until 2017: Busy with FEL projects (SwissFEL, E-XFEL in-kind contribution) for a decade -> only minimal maintenance of SLS.
- Performance (noise etc.) still acceptable for experiments, but they started seeing limitations of present system. Countermeasures:
  - Filling pattern feedback -> counteract filling pattern dependence of BPM electronics.
  - Better BPM electronics spare test, sort out electronics with higher noise (larger variations due to component tolerances).
  - Slow photon BPM feedback (on top of FOFB).

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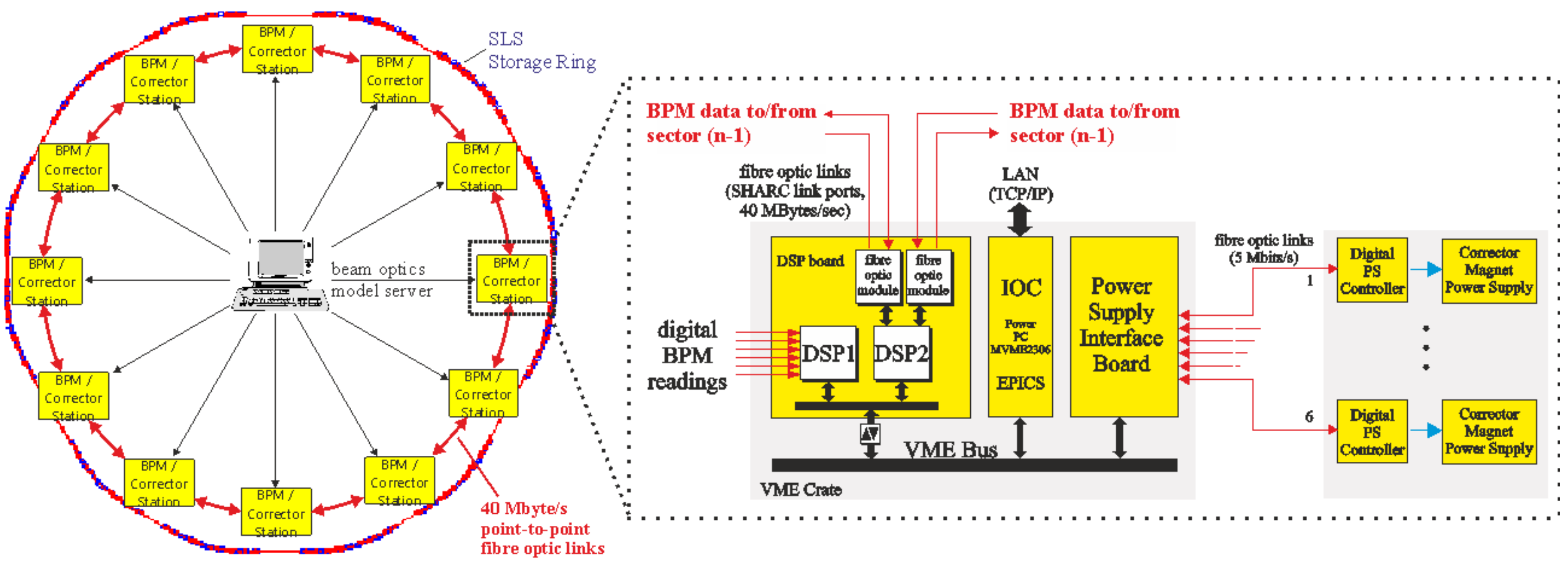
Present (Old) SLS BPM & FOFB System

SLS1 storage ring: 12 "BPM/FOFB" VME crates, each with:

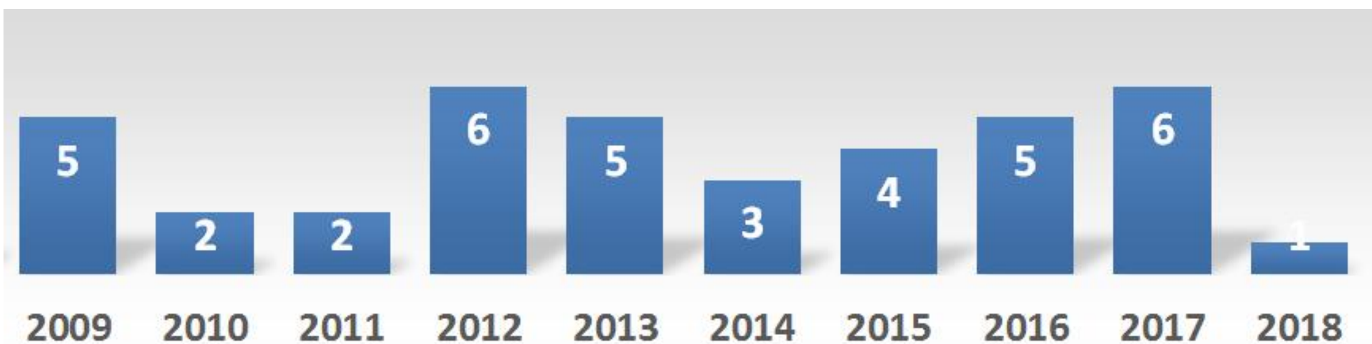
- 2 VMEbus EPICS IOCs (1 BPM, 1 Magnet) + Event Receiver
- 1 DSP Board (BPM position calculation, FOFB algorithm, ...)
- 6-7 BPM digitizer cards ("QDRs")
- 2 Hytech boards for corrector PS interface

BPM RF Front-Ends (RFFEs) put into 2nd VME crate (no IOC, control via slow serial interface).



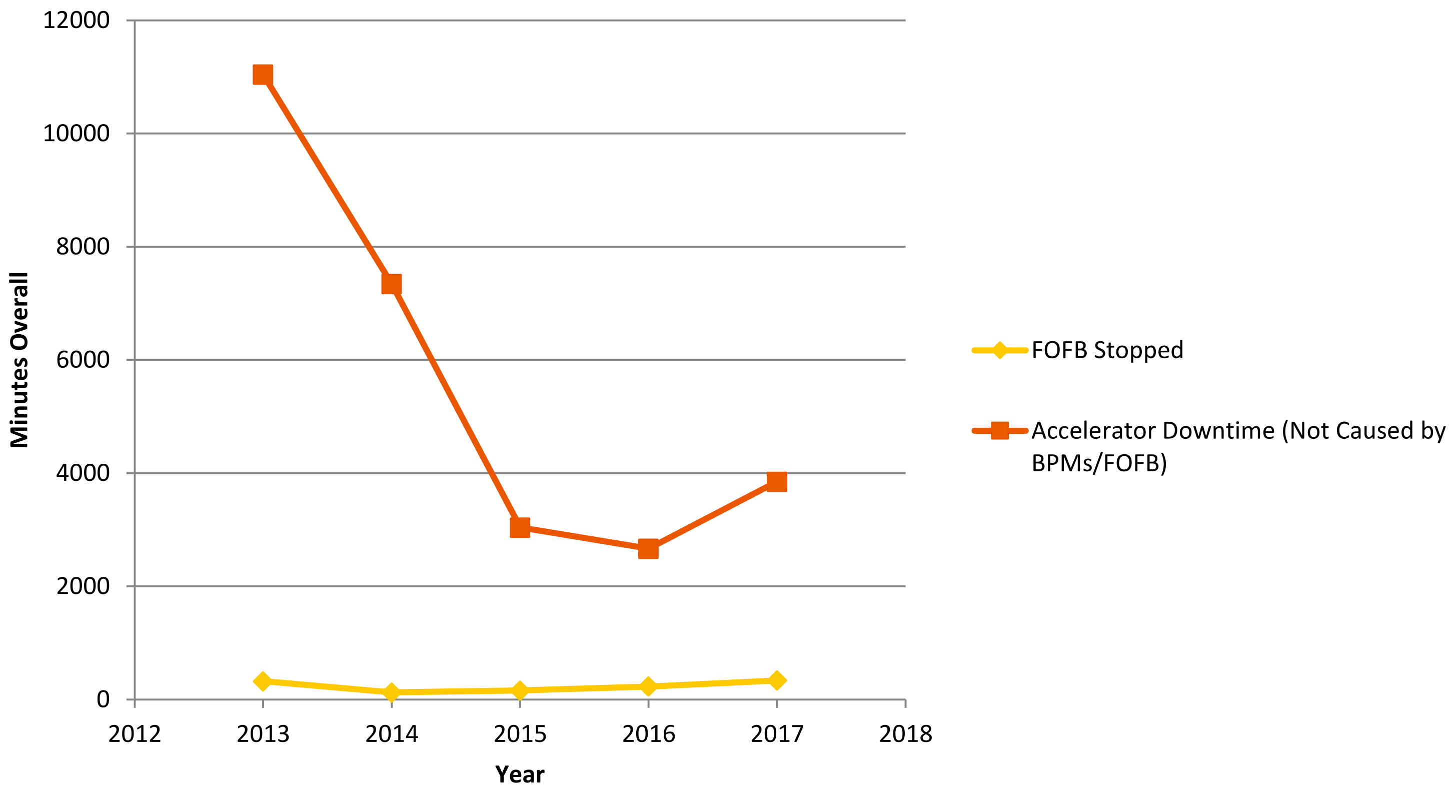
SLS1 BPM Failure Statistics

Number of annual BPM hardware failures/replacements (last update 3/2018 ...) -> comparatively stable (for a nearly 20 year old system ...).



SLS1 FOFB Failure Statistics

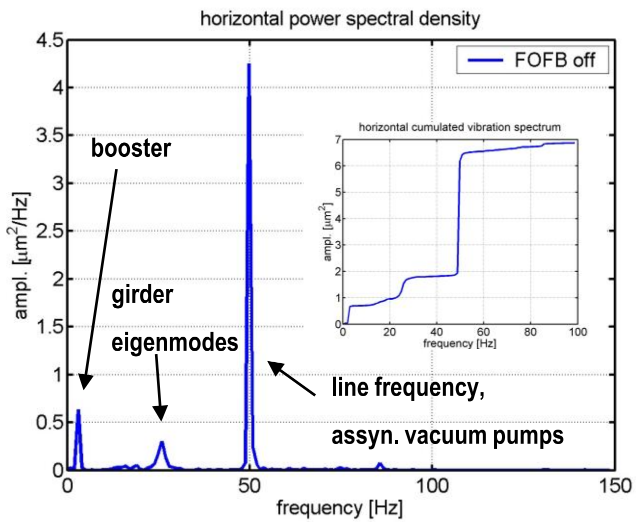
Integrated duration where FOFB is not running (and beam is not stable enough for many users) is negligible to overall accelerator downtime -> also no reason for (urgent) upgrade.



SLS1 FOFB Performance

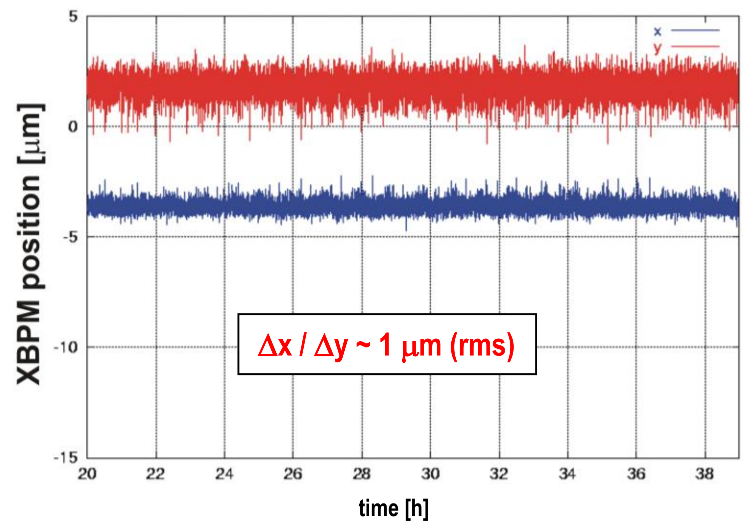
Power Spectral Density

Horizontal, measured at RF BPM outside of FOFB loop (β_x = 11 m).



Medium / Long Term Stability

Photon BPM signals at ID 06S, ~ 10 m from source point. Data points integrated over 1 s.



SLS Orbit Stability with FOFB

- Horizontally (1 - 100 Hz): $0.38\ \mu m \cdot \sqrt{\beta_x}$
- Vertically (1 - 100 Hz): $0.27\ \mu m \cdot \sqrt{\beta_y}$

Examples: tune BPM (β_y = 18 m) ⇨ Δy = 1.2 μm
ID 06S (β_y = 0.9 m) ⇨ Δy = 0.25 μm

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Future SLS BPMs

Initial plan (when we started designing VME-based E-XFEL & SwissFEL BPM electronics): Re-use PSI FEL BPM platform for SLS BPM upgrade:

- PSI FEL BPM platform (SwissFEL, E-XFEL) based on VME64x form factor, but does not use VME bus (standalone box with multi-gigabit SFP links at front & rear).
- Modular, could be equipped with SLS-specific RFFE/ADC.
- Had already developed prototype SLS RFFE (pilot tone, input crossbar switch, active temperature regulation, ...).

Future SLS BPMs

2017: Change of plan. Decision:

- Will not use VME64x any more as BPM form factor.
- Use latest technology:
  - Xilinx Zynq UltraScale+ MPSoC (FPGA + dual-core 32-bit ARM + quad-core 64-bit ARM CPUs) favored as general future SLS2/PSI processing platform (not only for BPMs).
  - JESD204B ADCs (ADCs with multi-gigabit serial links), at least for BPMs.

Why?

- SLS2: Using form factor VME64x with parallel bus concept from 1980s is technically feasible but IMHO suboptimal for SLS2 accelerator running from 2025-2045+.
- New technology allows to make BPM electronics simpler, cheaper (>1MCHF), more performant.

Future SLS BPMs

SLS2 BPMs: What form factor / crate standard?

- VME64x has no obvious successor (for us)
- PSI has not yet decided which future standard to use for SLS2 (ongoing evaluation: uTCA.0, uTCA.4, CPCI-serial, VPX, ...)
- All standards have drawbacks:
  - uTCA.4: Market size ~2-3% of VME → some companies stop developing/selling products (ELMA, Kontron, ...). Only used by accelerators & research.
  - ATCA: Made for telecom, but they start using other standards. PCBs "too large" for distributed smaller systems.
  - VPX: Larger & growing market, new standard for military that funds new designs, but expensive hardware & zoo of different backplane topologies.
  - CPCI-serial: Growing market, already used at PSI for neutron experiments, but no decision (yet?) to use it for PSI accelerators.

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Future SLS BPMs

SLS2 BPMs: What is the minimum I need/want?

- RF front-end (filters, variable amps/attenuators, pilot, crossbar, active temperature regulation of PCB, ...)
- ADC with multi-gigabit link (JESD204B)
- Zynq UltraScale+ MPSoC (handling three SLS BPMs)
- Housing, power (single 12V), cooling

Expected number of BPM applications (SLS2, upgrades of other machines) large enough to justify BPM specific hardware design -> start developing **"DBPM3" BPM platform** in 2017:

- Form factor determined by application requirements
- Cost estimate >1MCHF lower than alternative solutions we analyzed (PSI FEL platform, COTS VME/uTCA/..., ...).
- All-in-one PCB too large -> split DBPM3 into MPSoC back-end and several RFFEs (that include ADCs).

DBPM3 Complexity

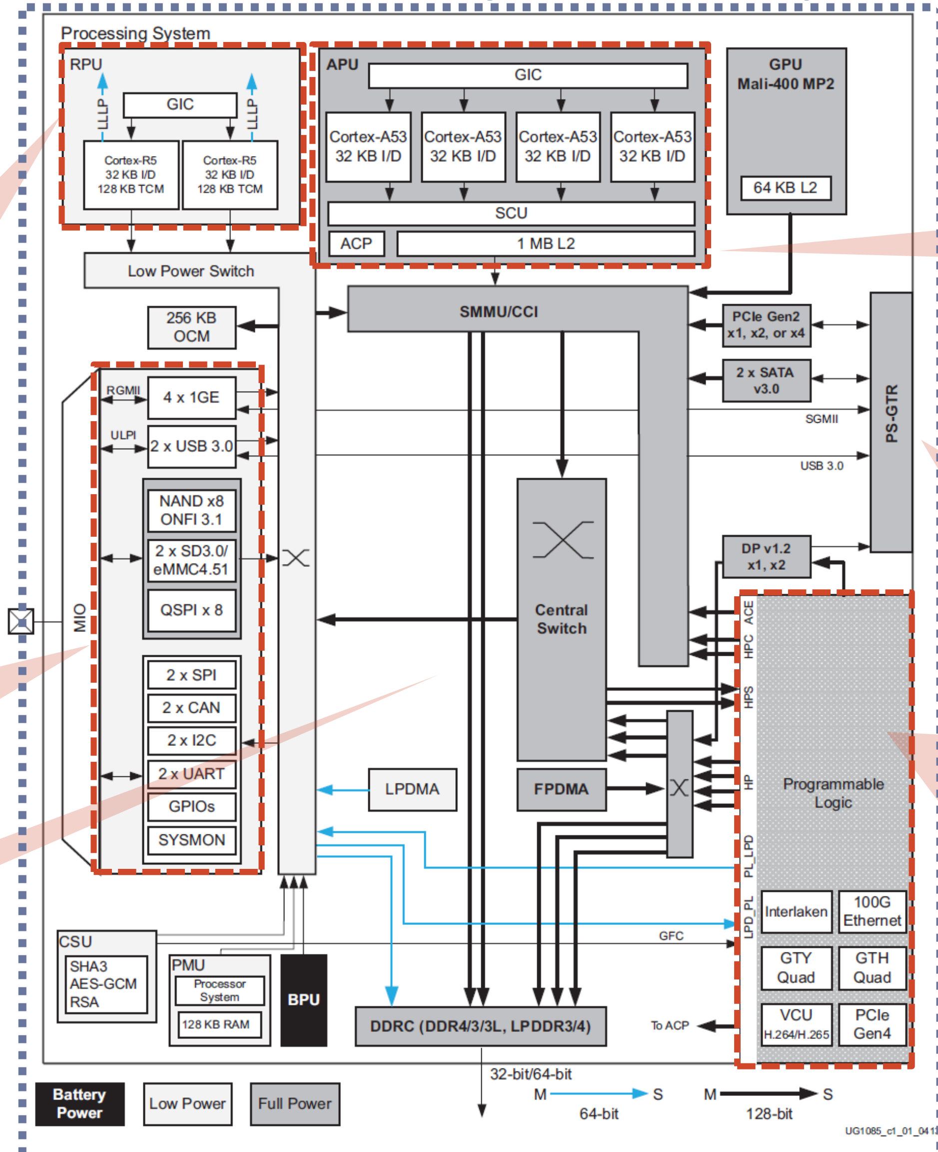
- DBPM3 platform has much lower hardware complexity and points of failure compared to SwissFEL & old SLS BPMs

- DBPM3 production can be fully outsourced (not possible for SwissFEL BPMs), assembly, test and hardware maintenance much easier.

BPM System	Extra Timing System VME Card Needed	Extra VME Crate + CPU card for EPICS IOC Needed	# Printed Circuit Boards per Button BPM	# FPGAs per Button BPM
Old SLS 1.0	yes	yes (1 per 6 BPMs)	10	2 + ASICs
SwissFEL Platform	no	yes (1 per 16 BPMs)	3.25	1.75
DBPM3 Platform	no	no	1.33	0.33

DBPM3: Xilinx Zynq UltraScale+ SoC

MultiProcessor System-On-a-Chip



RPU: Realtime processor for FOFB algorithm, BPM control & data processing, ...

Standard Interfaces (USB, EEPROM, FLASH memory, ...)

Flexible on-chip data/address "bus" (switch) system

APU: Processor for Linux with EPICS IOC

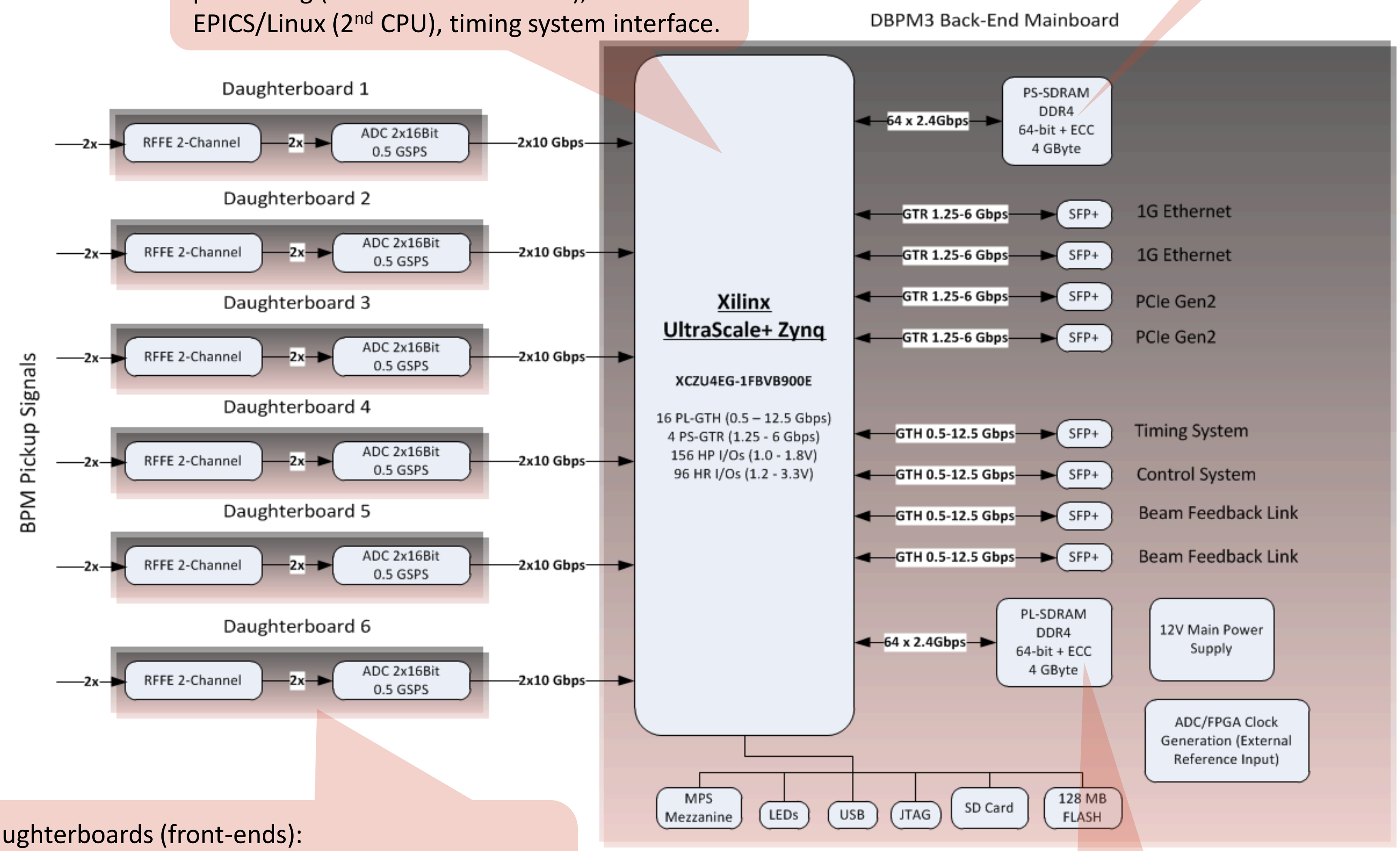
Multi-gigabit interfaces (PCIe, Ethernet, ...)

FPGA (logic elements with programmable interconnect, ...) for digital downconversion of ADC raw data, timing system interface, feedback interface, ...

DBPM3 Platform

System-on-Chip (SoC): BPM/feedback data processing (FPGA + real-time CPU), EPICS/Linux (2nd CPU), timing system interface.

RAM for Linux/ EPICS



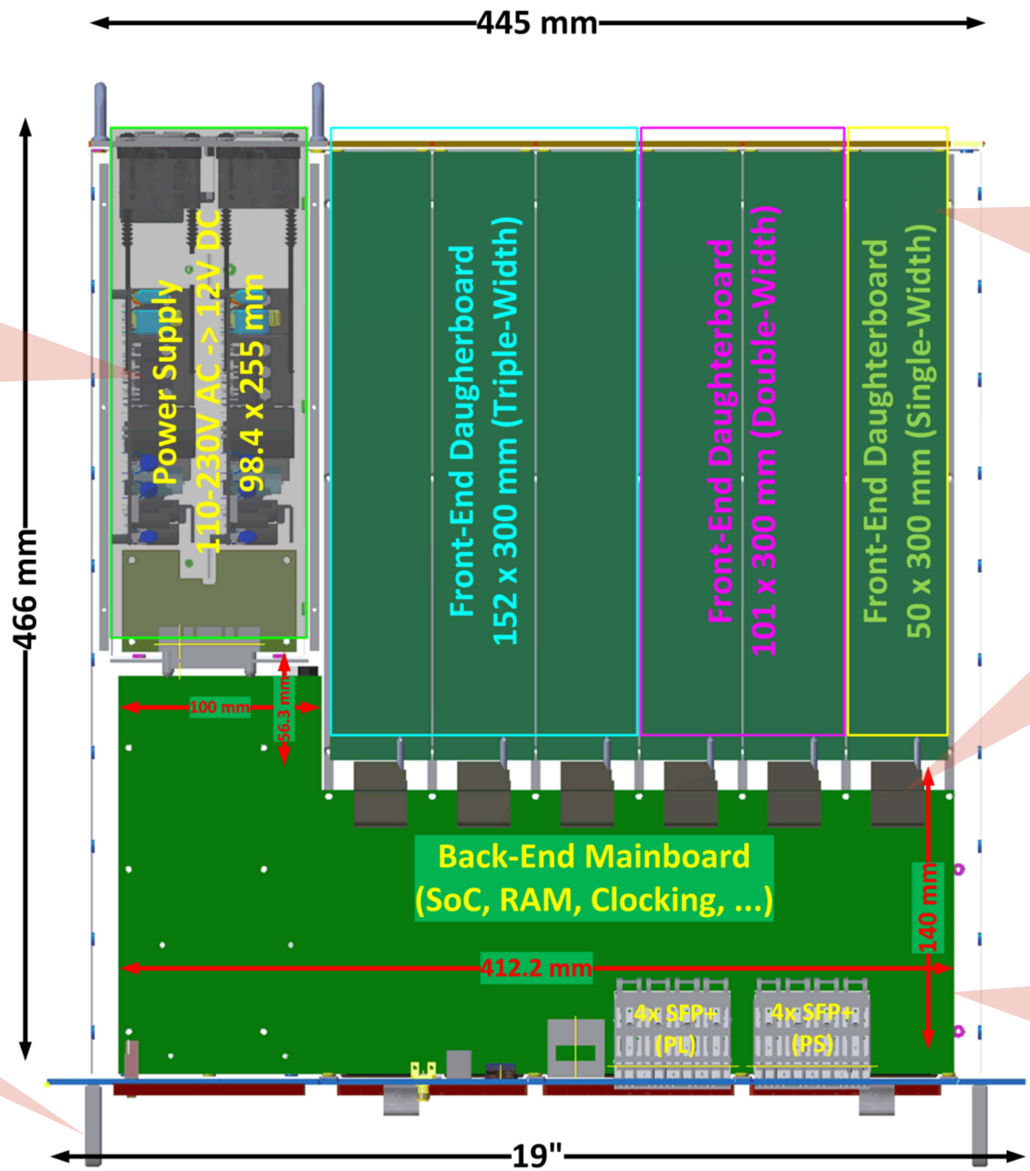
Daughterboards (front-ends):

- 6x single-width (feedback network SFP+ switch)
- or 3x double width (SLS button BPM)
- or 2x triple-width (SwissFEL cavity BPM)

RAM for measurement / ADC raw data

DBPM3 19" Unit

Commercial power supply (optional redundancy)



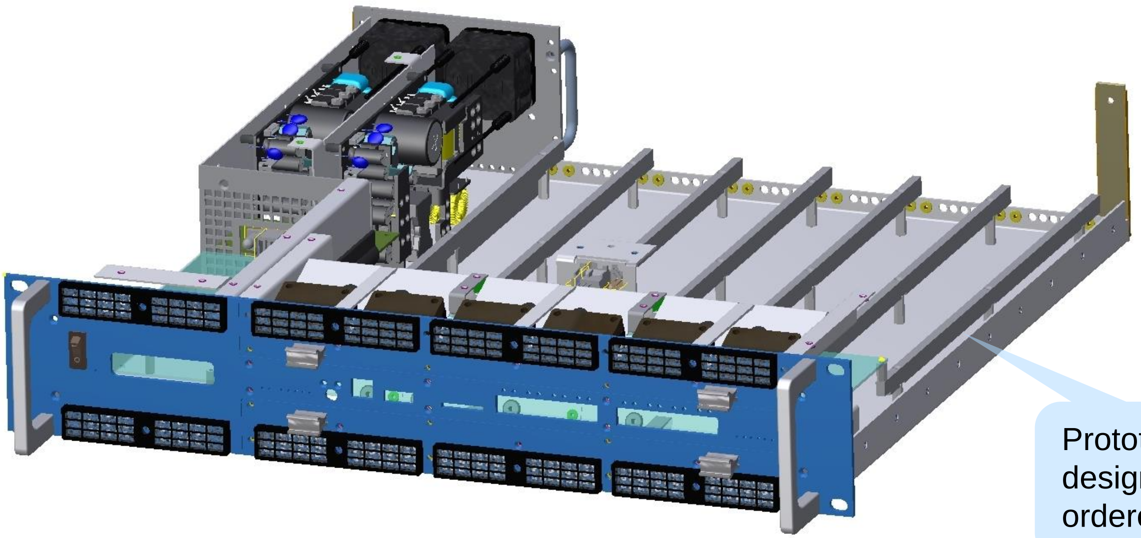
Front-ends ("daughter-boards") plugged in from rear side (live insertion possible)

Guided coplanar daughterboard connector (multi-gigabit data links, clocks, user IOs, ...). Dual-source.

Back-end mainboard (with MPSoC, external interfaces, ...)

Front side

DBPM3 Mechanics



Prototype designed & ordered

- RF front-ends with ADCs inserted from rear side (live insertion)
- Low-cost high-speed connectors from RFFE/ADC to FPGA board (coplanar, 25Gbps per diff pair, dual-source)
- Cost-optimized
- Single 12V supply
- Redundant fans, removable fan tray & filters
- Air flow front-to-rear for lower BPM position drift (VME: side-to-side flow would cause gradients over BPM channels)
- Mechanical dimensions allow use for BPMs (SLS, SwissFEL, proton machines), beam loss monitors (photomultipliers can be fitted on both PCB sides), ...
- Simple production & assembly

DBPM3 PCB Design: "Virtual" PCB Modules

- DBPM3 uses a new PCB design technology that allows to save personnel AND hardware costs and improve reliability and performance, using "virtual" PCB modules (Mentor Graphics "managed blocks", ...):
  - In the past, we had a modular BPM system where different PCBs were plugged together. Drawbacks:
    - Added costs
    - Lower reliability (more contact pins)
    - Lower performance (connectors degrade high-speed signals)
  - Now: "Virtual" PCB modules
    - Are designed once (schematics + layout) can then be re-used for different applications.
    - Are placed on the same PCB (no connectors): Less costs, higher reliability.
  - New SwissFEL DBPM3 RFFE already uses virtual PCB modules (ADC, RFFE)

DBPM3 Applications

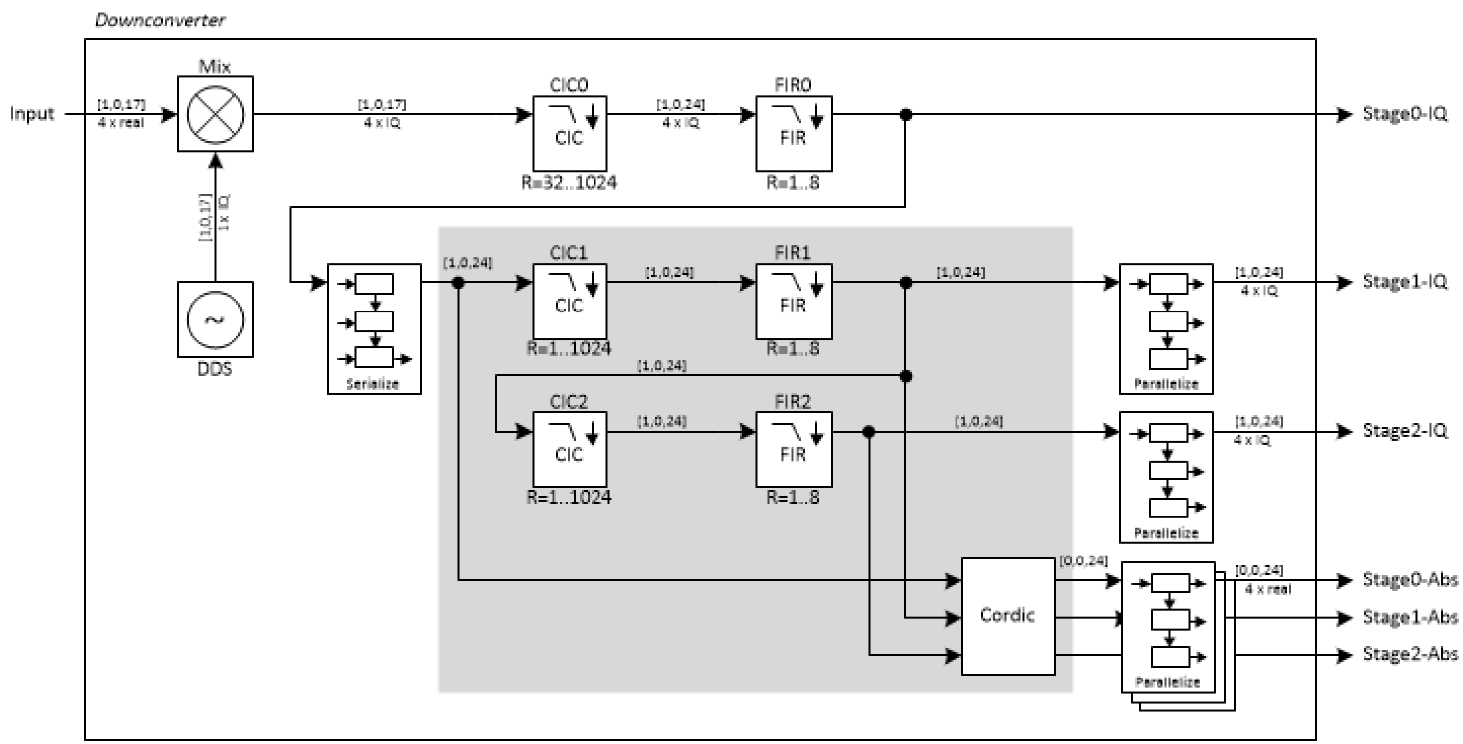
Application	#DBPM3 Units*	BPMs or SFPs per Unit**	Needed in Year	Develop-ment Status
SwissFEL BPM (Athos)	24	4	2019	Advanced
SLS1 RF BPM	76	3	2020+	WIP
SLS1 Fast Orbit Feedb.	18	16	2020+	WIP
SLS2 RF BPM	31	3	2024	WIP
SLS2 Fast Orbit Feedb.	27	16	2024	Concept
PSI Proton Accel. BPM	20	3	2025+	Concept
SLS2 Beam Loss Mon	...	...	2024	Idea
SLS2 Photon BPM	...	...	2024	Idea
SLS2 Low-Level RF	...	...	...	Idea
Overall ****	**196**			

* Incl. spares & prototypes

** Fast Orbit Feedback (FOFB) uses fiber optic tree network with SFP+ transceiver daughterboards.

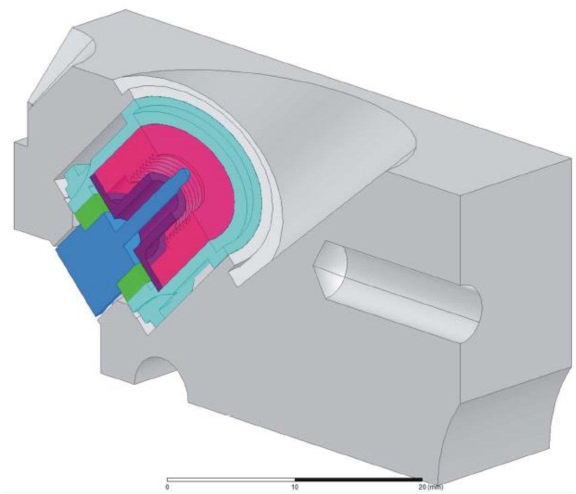
DBPM3: DDC Firmware (Prototype)

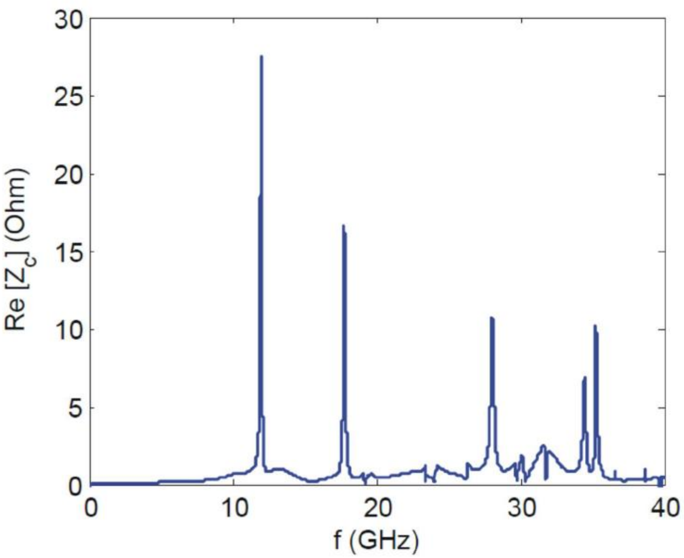
DBPM3: Digital downconverter (FPGA firmware module by PSI) provides turn-by-turn (1 MSPS), fast orbit feedback (20kSPS) and slow high-resolution data (few Hz) simultaneously (not possible with old SLS BPM system). Latest version optimized for parallel processing of beam and pilot signal frequency.



SLS2 BPM Mechanics/Electrodes

- SwissFEL BPMs already use low-cost glass ceramic RF feedthroughs developed by PSI with Swiss company BC-Tech
- SLS2: We are also evaluating glass ceramic feedthrough. Presently still "feasibility study". Status: PSI design proposal done, feasibility now to be checked by BC-Tech (production process, tolerances, ...).





SLS2 CDR / F. Marcellini et al.

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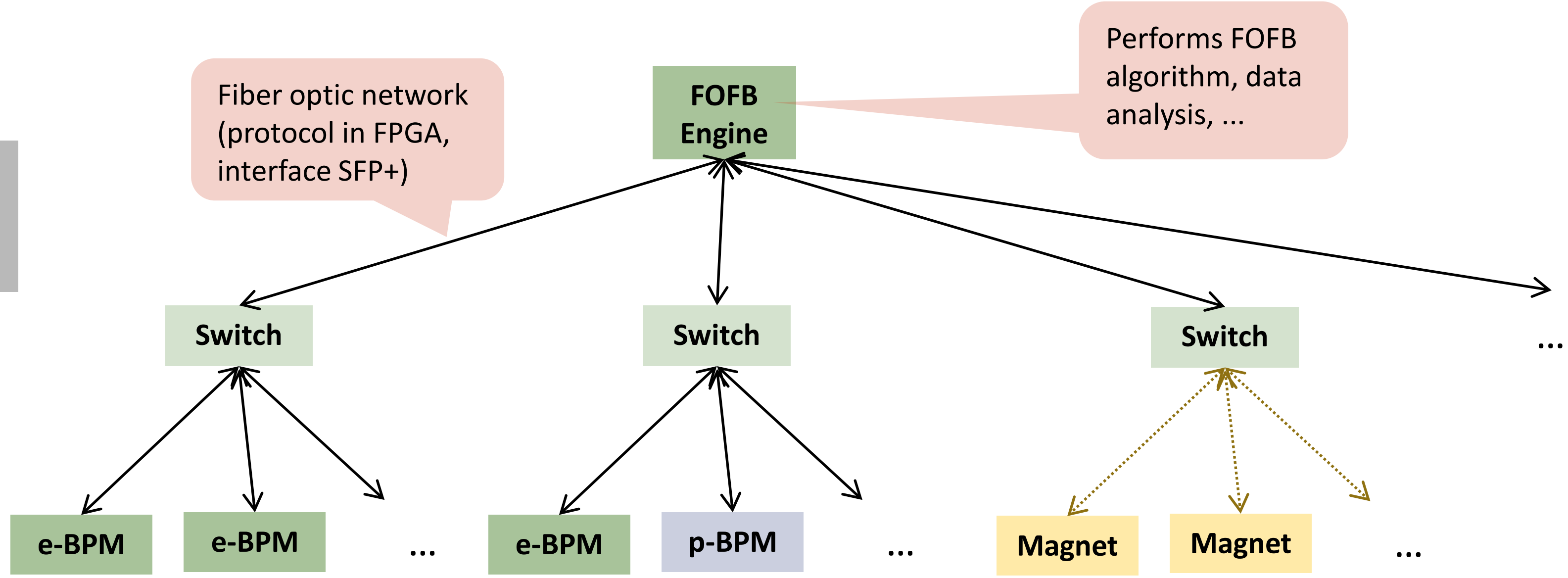
SLS FOFB Upgrade Steps

	SLS1 (now)	SLS1 (2022)	SLS2 (2024+)
Network Topology	Ring	Tree	Tree
FOFB Algorithm	Distributed (4kHz)	Centralized (4kHz)	Centralized (20kHz)
Scalable	No	Yes	Yes
Magnet PS	Original (2000)	Original (2000)	New (2020+)
Magnet PS Interface	VME	VME	Fiber
BPM Platform	DBPM1 (VME)	DBPM3 (Zynq U+)	DBPM3 (Zynq U+)

Final SLS2 FOFB System



<u>Data transfer from/to "FOFB Engine": Tree topology</u>

- Can be scaled/extended (size, performance)
- Allows mix of different monitors & actuators (e-BPM, <u>photon BPM</u>, magnet PS, ...)
- Uses fiber optic links (50MBaud POF for magnet PS, multi-gigabit SFP+ for everything else)
- e-BPM, Switch & FOFB Engine can use same FPGA board (Zynq U+ SoC).

Incremental SLS1 BPM/FOFB Upgrade

Former Upgrade Plan:

- Change from old to new BPM system in one shutdown
- Risk: Not much time to migrate rather large system (including controls, EPICS, ...), need/want fallback to old system in case something does not work.

Present Plan: Incremental Upgrade

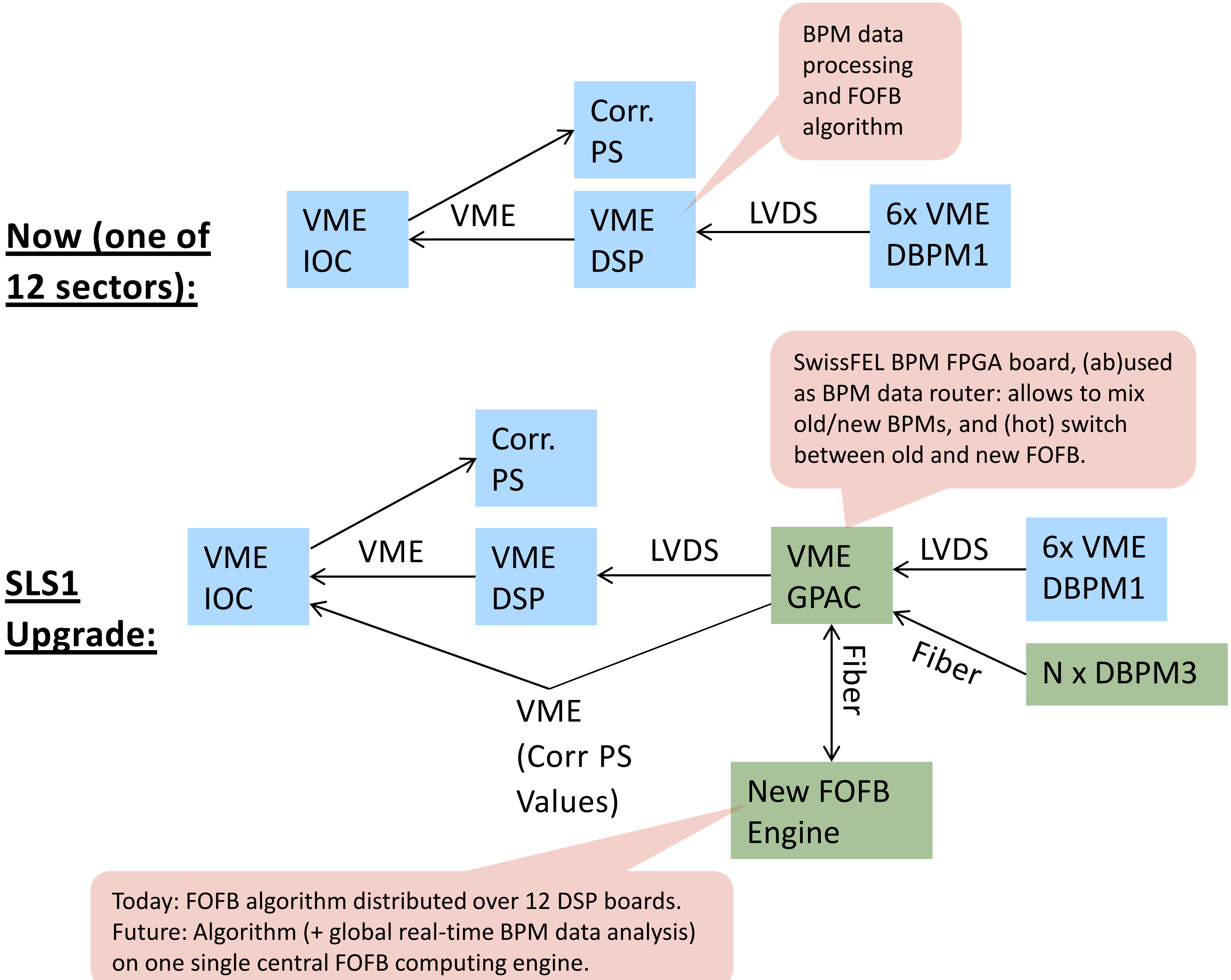
See next slide

- New BPMs & FOFB installed parallel to old hardware (in same racks)
- Old and new BPMs can be mixed (transparently), by making new BPMs look like old ones (to old FOFB & control system)
- Old and new FOFB installed in parallel, fast switch from old to new system (e.g. for tests in machine shift) and back

Advantages:

- Gradual migration from old to new system reduces risks
- Easier to get experience with new BPMs & FOFB
- Possibility to mix old and new BPMs relaxes spare part situation

Incremental SLS1 BPM/FOFB Upgrade



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Summary & Outlook

- New DBPM3 BPM platform under development.
- First tests with Zynq UltraScale+ & ADC eval board promising (noise, drift using pilot tone, data errors at 10Gbps, ...).
- Presently focusing more on 1st application (SwissFEL cavity BPMs, needed end 2019) rather than usage for SLS1/SLS2 (2022-2024).
- Expect daughterboards prototypes for SwissFEL (cavity BPM RFFE/ADC) and SLS (button BPM RFFE/ADC) in 2019.
- General control system hardware platform for all SLS2 systems not yet defined, evaluation (VME, uTCA, CPCI-Serial, ...) ongoing.
- Many other new SLS2 systems most likely also will use Zynq UltraScale+ (already decided for magnet power supplies) -> synergies with BPM system.
- DBPM3 platform also suitable for other systems (e.g. loss monitors)

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Wir schaffen Wissen – heute für morgen

Thank you for your attention!

Thanks to my group:

- D. Engeler (Zynq U+ board)
- G. Marinkovic (Firmware & Software)
- D. Treyer (RF)

and all supporters at PSI, including:

- F. Marcellini (BPM pickups)
- R. Ditter (DBPM3 Crate)
- M. Stadler (SwissFEL RFFE)
- M. Gloor (ADC)
- M. Böge

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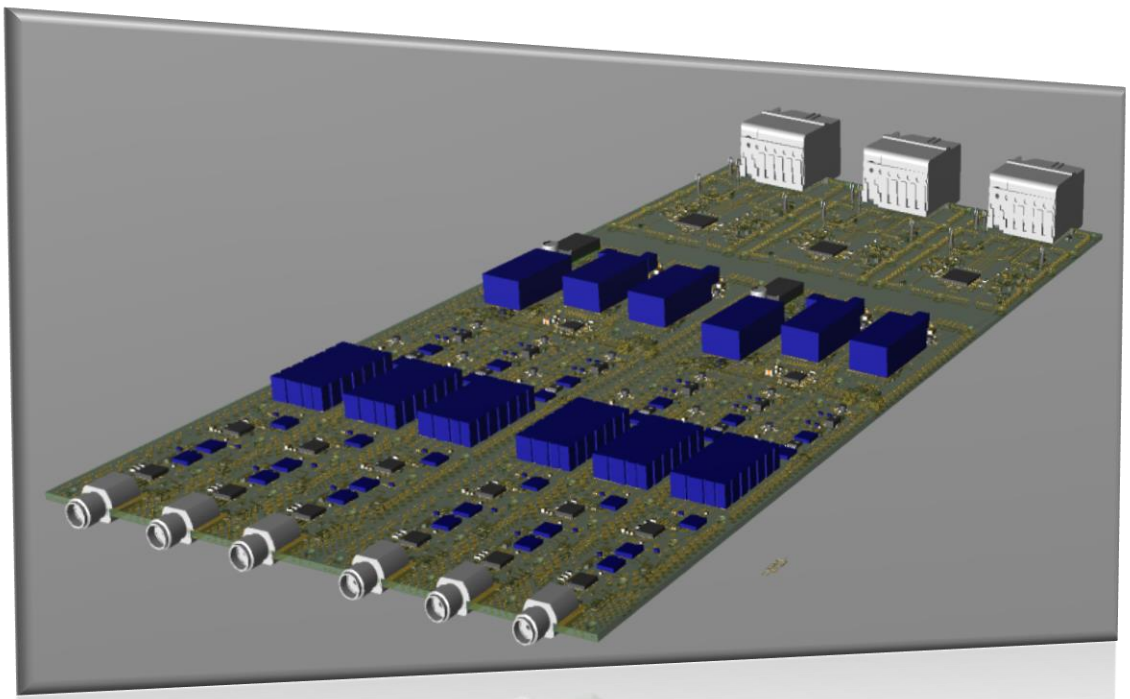
Supplementary Slides

DBPM3: Athos High-Q RFFE/ADC

- One DBPM3 unit handles 4 SwissFEL high-Q cavity BPMs (2 RFFEs per unit, 2 BPMs / 6 channels per RFFE).
- 500 MSPS 16-Bit ADCs (JESD204B, 10Gsps per link)
- Multi-gigabit connectors to DBPM3 FPGA board
- Design (M. Stadler / M. Gloor)
- Prototypes/pre-series planned 2019



Final SLS2 FOFB: Photon BPM Integration

Possible Steps

1. Photon BPM characterization
   1. Long-term stability
   2. Systematic errors/dependencies (bunch pattern/charge, ...)
   3. ...
2. Stabilize photon BPM position reading with slow (~Hz) high-level feedback
3. Start using photon BPMs in fast feedback loop, beginning with beamline(s) that benefit (most) from this

Challenges & Risks

- Vibrations of beamline components: Using photon BPMs that see such vibrations in fast feedback loop may deteriorate global electron beam stability (leakage of fast orbit correction around beamline source points)
- Photon BPMs may have to be taken in and out of feedback loops more often than e-BPMs (ID changes, ...) -> Integration into FOFB may need more frequent FOFB restart
- General: Using photon BPMs of one beamline for fast orbit feedback has higher risk of interference with other beamlines.
- Photon & e-BPMs may have different bandwidth & latency (and photon BPM bandwidth may vary e.g. with intensity) -> use in same feedback loop not trivial

SLS BPM & FOFB Components & Features

Subsystem	SLS1 Now	SLS1 2022	SLS2 Day1	SLS2 Final
Electron BPM Pickups & Mechanics	Old	Old	New	New
BPM Electronics Hardware	Old	New	New	New
BPM Electronics Firmware/Software	Old	New	New*	New*
Fast Orbit Feedback DSP Hardware	Old	New	New*	New*
Fast Orbit Feedback DSP Software	Old	New	New*	New*
Fast Orbit Feedback Magnet Power Supplies	Old	Old	New	New
Fast Adaptive / ID Gap Feed-Forward	-	-	New	New
Timing System Interface	Old	New	New*	New*
Control System Interface	Old	New	New*	New*
Slow Photon BPM Based Orbit Feedback	Old	Old	New	New
Fast Photon BPM Based Orbit Feedback	-	-	-	New
Operator/Expert High-Level Applications	Old	Mix	New	New
Slow Orbit Feedback (Backup for Fast Feedback)	Old	Old	New	New
Physics / Beam Optics Applications	Old	Mix	New*	New*
Fast First-Fault Detection/Archiving	-	-	New	New
Automated/Pro-Active Fault Detection	-	-	-	New

- *Significant adaptations for SLS2 (different from SLS1) needed (optics, lattice, performance, number of elelements, data rates, control & timing system, ...)*