# Data transmission & digitisation – what is state of the art today?

## *For Beams Instrumentation & LHC Experiments*

**Manoel Barros Marin**

Joint ARIES Workshop on Electron and Hadron Synchrotrons:
"Next Generation Beam Position Acquisition and Feedback Systems"
(12/11/2018)


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- Introduction
- Current Generation (LHC Run 1)
- New Generation (LHC Run 3)
- Next Generation (HL-LHC)
- Summary


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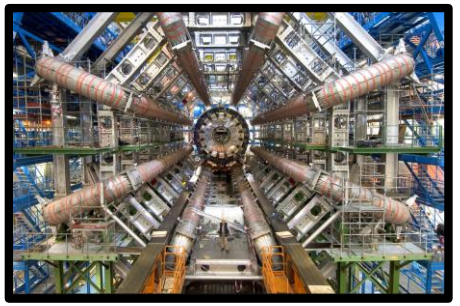
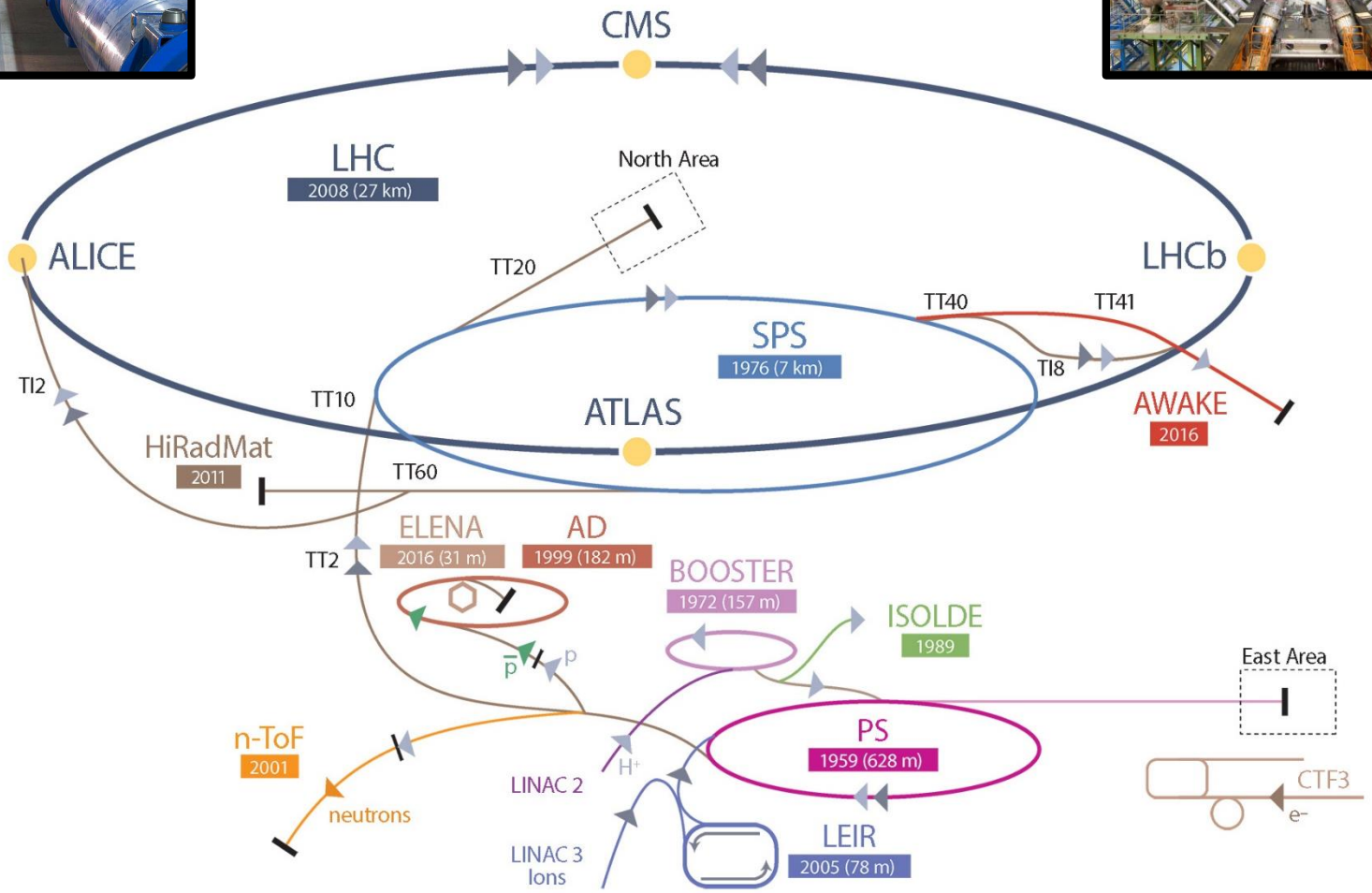
# Introduction

## Particle Accelerators & LHC Experiments at CERN

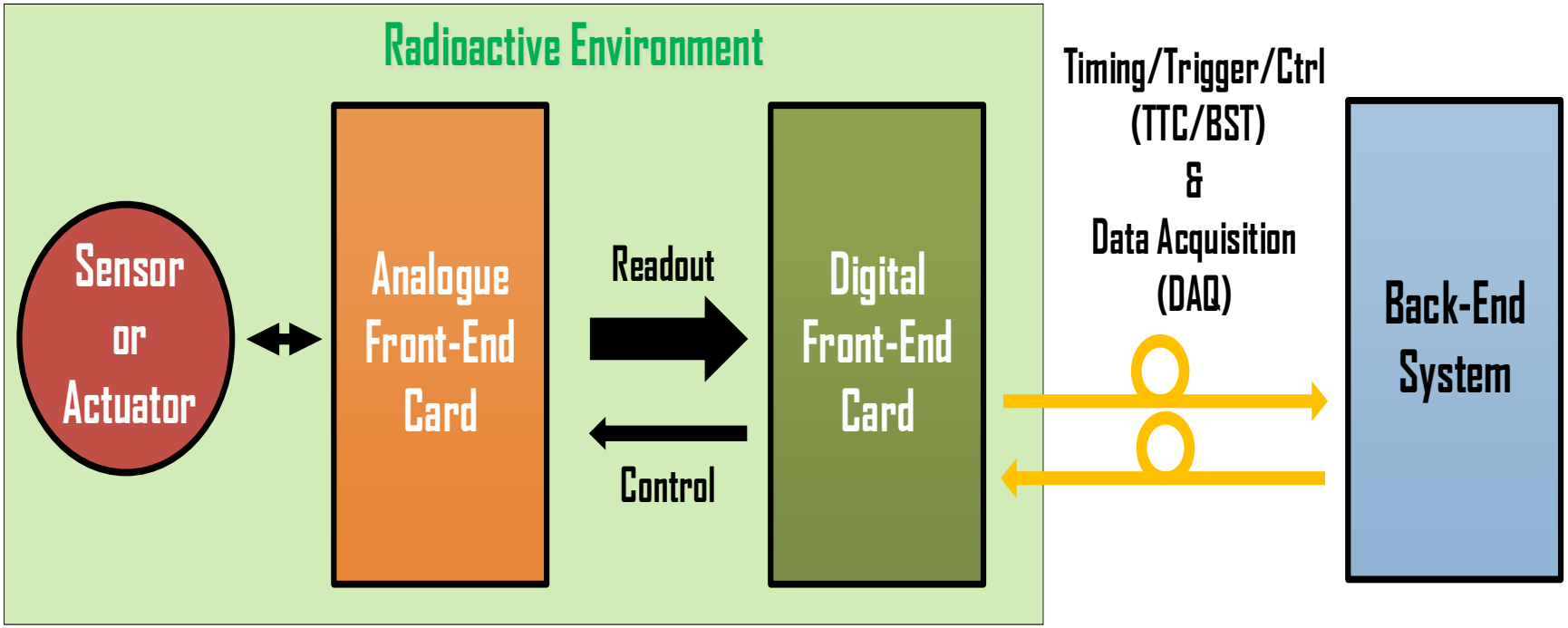




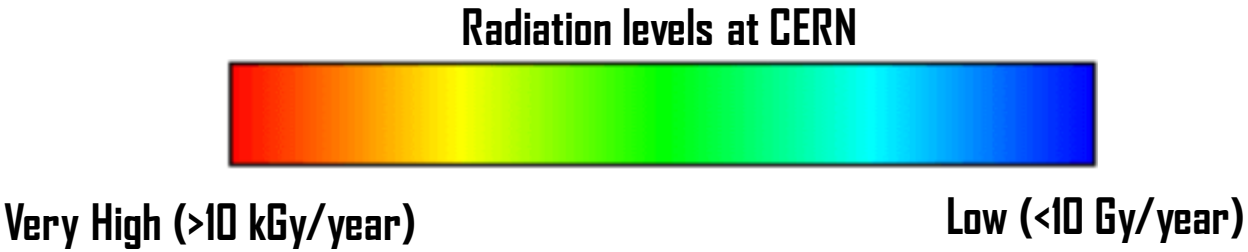
# Introduction

## Electronics for Beam Instrumentation & LHC Experiments

- Similar architecture in many projects




- Electronics may be exposed to high radiation levels



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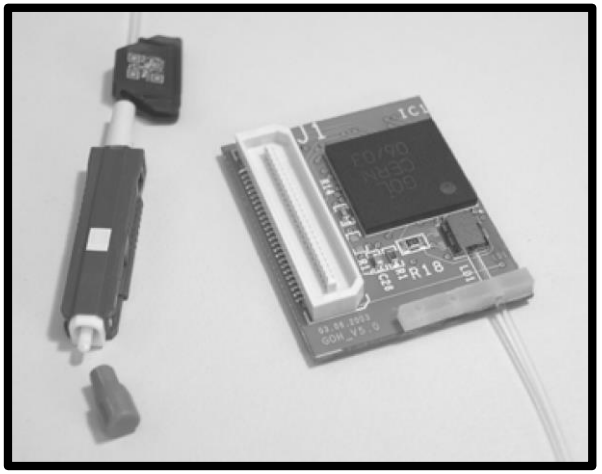
# Current Generation (LHC Run 1)

## Common approach

- **Adopted by LHC BLM, ATLAS, CMS, LHCb, ALICE…**
- **Non-Rad-Hard Front-End & Back-End electronics based on COTS* components**
- **Data Link: Gigabit Optical Link (GOL)**
  - Rad-Hard design from CERN (EP-ESE)
  - Line Rate:
    - Fast: 1.6 Gbps (1.28 Gbps payload: 32 bits @ 40 MHz)
    - Slow: 0.8 Gbps (0.640 Gbps payload: 16 bits @ 40MHz)
  - Encoding Protocols:
    - G-Link
    - 8b/10b
  - Used for Data Readout
  - Optical transmission:
    - Multi-mode
    - Single-mode
  - Radiation Tolerance:
    - TID > 100 kGy (dose rate (X-rays): 100.6 Gy (SiO2)/min)
    - SEE > 3x10^8 p/cm2s (200 MeV proton beam)

GOL Opto-hybrid (GOH)



*Commercial Off-The-Shelf (COTS)

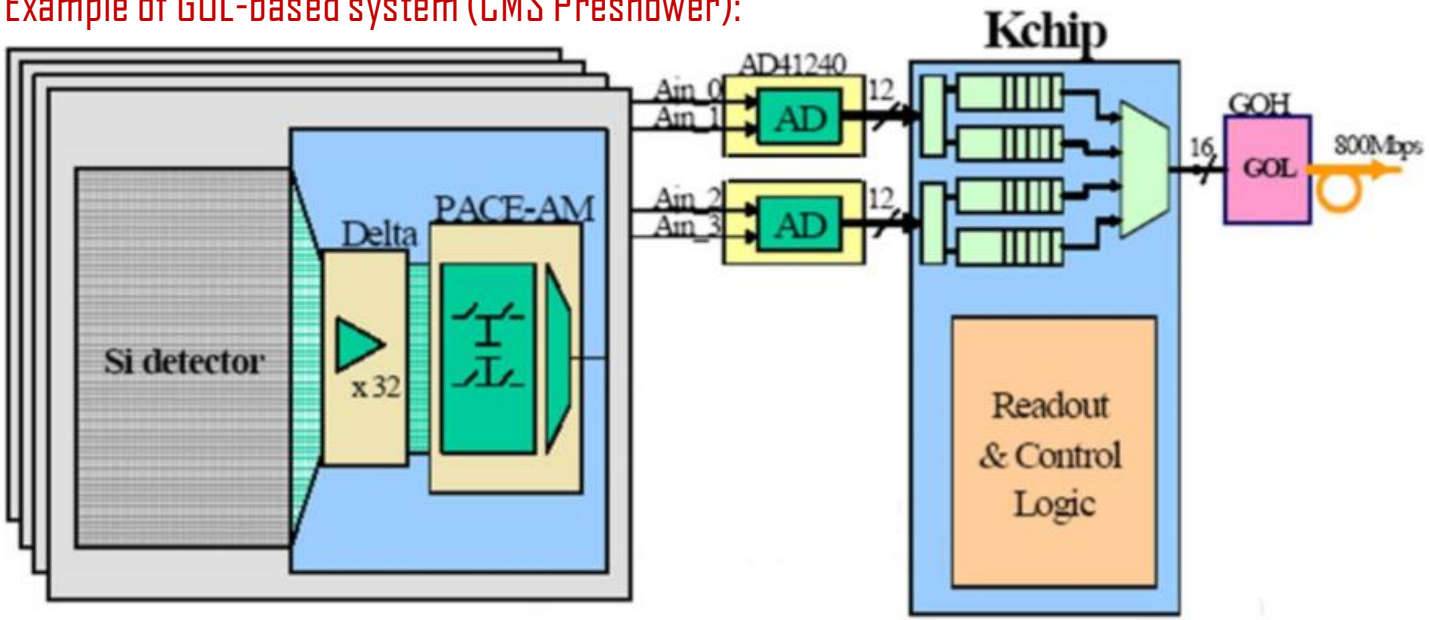
# Current Generation (LHC Run 1)

## Common approach

- **ADC: AD41240**
  - Rad-Hard design from CERN (EP-ESE)
  - Pipelined Analogue-to-Digital Converter (ADC)
  - 4 x 12-bit @ 40 Msps (or 1 x 14 @ 40 Msps)
  - Differential analogue inputs & Parallel digital outputs
  - Radiation Tolerance:
    - TID > 100 kGy (dose rate (X-rays): 333.3 Gy (SiO2)/min)
    - SEE > 3x10^8 p/cm2s (200 MeV proton beam)

AD41240

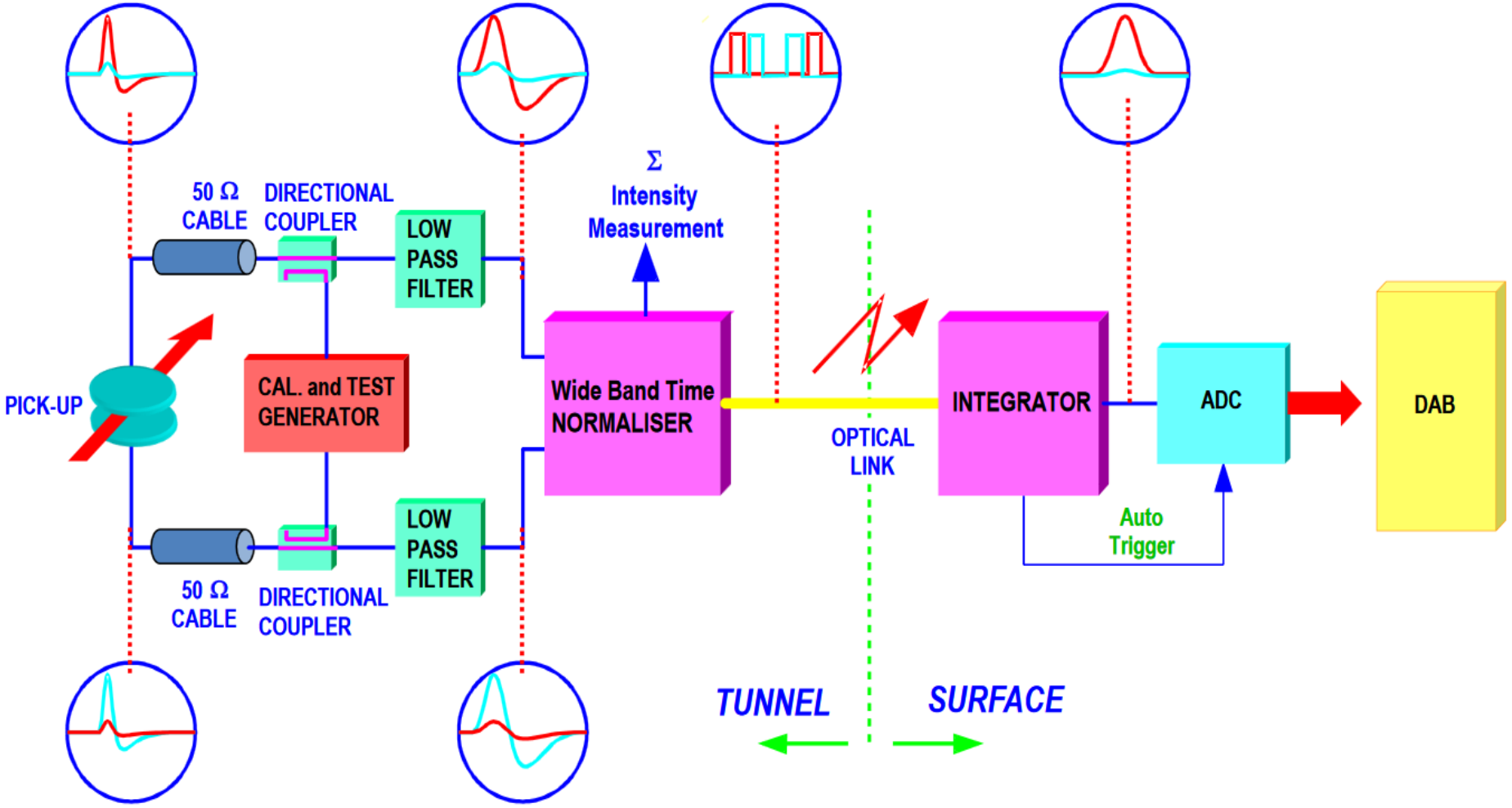

Example of GOL-based system (CMS Preshower):



# Current Generation (LHC Run 1)

## Application specific

- e.g. LHC BPM (analogue data transmission)




(Diagram courtesy of Eva Calvo (CERN BE-BI))

# Data transmission & digitisation – what is state of the art today?

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# New Generation (LHC Run 3)

## Common approach

- **Adopted by SPS BPM, ATLAS, CMS, LHCb, ALICE…**
- **Non-Rad-Hard Front-End & Back-End electronics based on COTS components**
- **No new Rad-Hard ADC developed at CERN for this generation (AD41240 still used)**
- **Data Link: GigaBit Transceiver (GBTx)**
  - Rad-Hard design from CERN (EP-ESE)
  - Encoding Protocols:
    - Wide-Bus (No Error Detection)
    - GBT (FEC16 (Reed-Solomon))
  - Line Rate:
    - Wide-bus protocol: 4.8. Gbps (4.56 Gbps payload: 114 bits @ 40MHz)
    - GBT protocol: 4.8 Gbps (3.28 Gbps payload: 82 bits @ 40 MHz)
  - Latency Deterministic (Downstram/Upstream)
  - Use for Data Readout & Timing, Trigger and Control
  - Radiation Tolerance:
    - TID > 1 MGy (dose rate (X-rays): 1 kGy (SiO2)/min)
    - SEE > 1x10^8 p/cm2s (36 MeV proton beam)

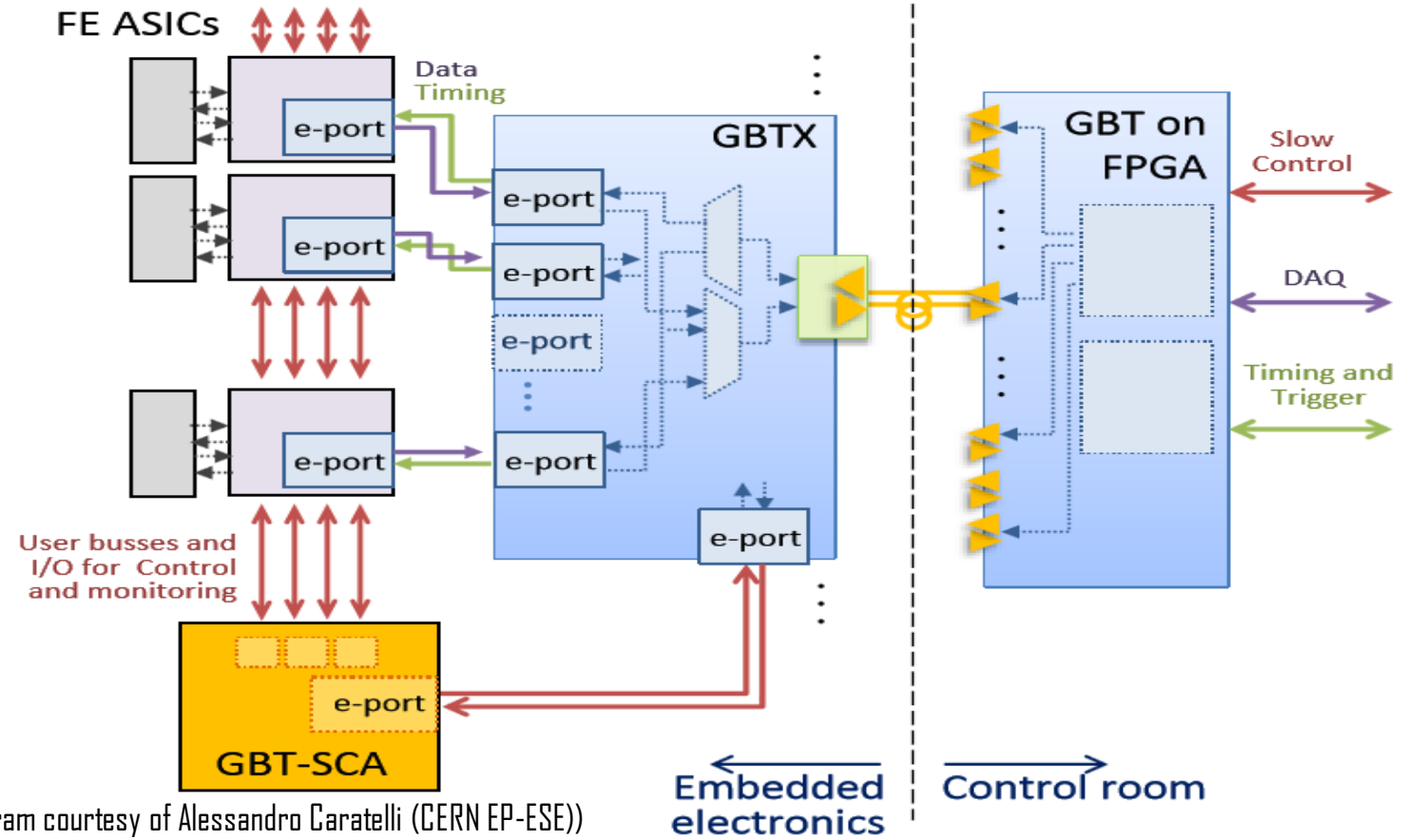
GBTx

# New Generation (LHC Run 3)

## Common approach

- Adopted by SPS BPM, ATLAS, CMS, LHCb, ALICE…
- Non-Rad-Hard Front-End & Back-End electronics based on COTS components
- No new Rad-Hard ADC developed at CERN for this generation (AD41240 still used)
- Data Link: GigaBit Transceiver (GBTx)

Back-End/Front-End GBT Link diagram

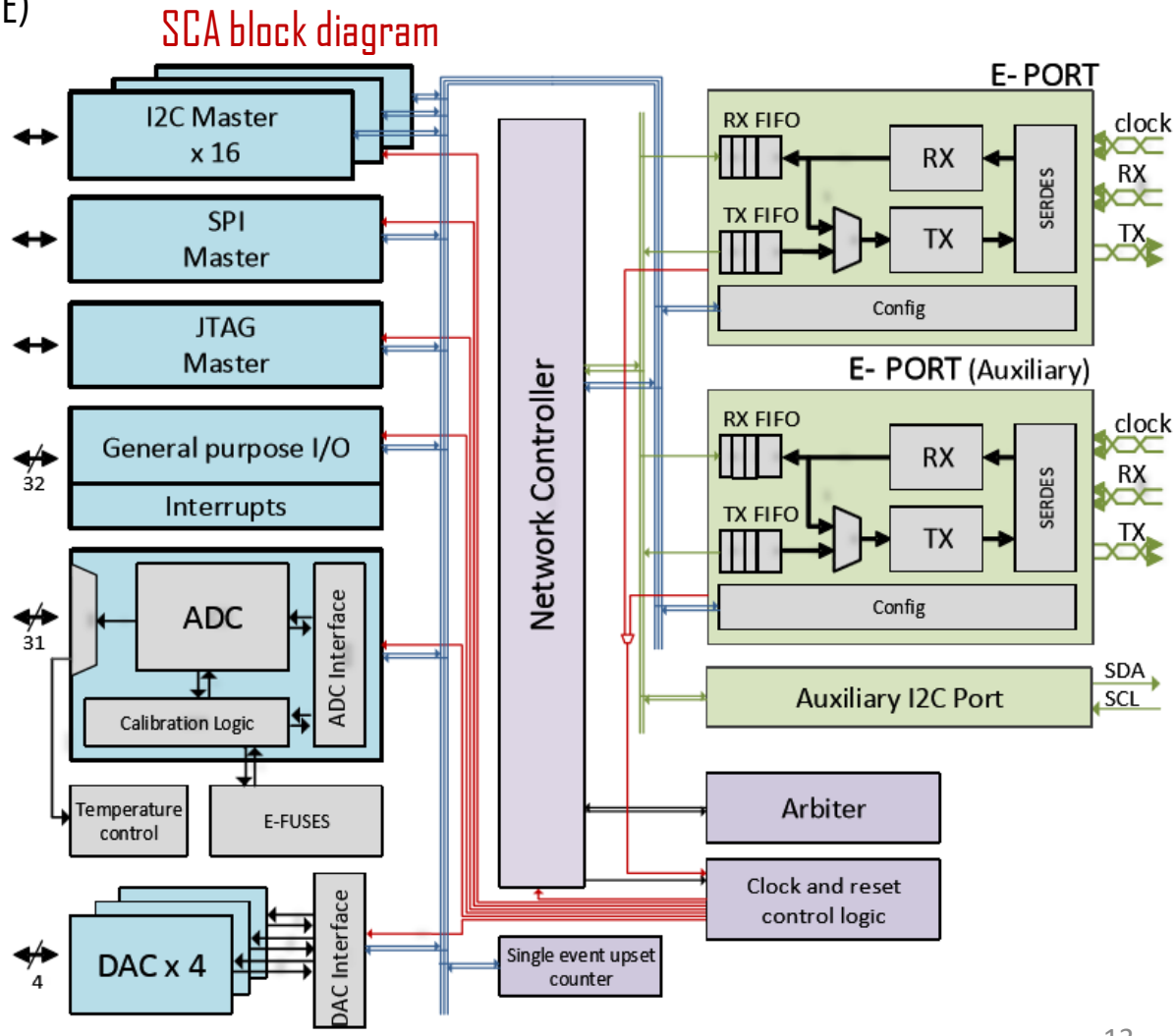



(Diagram courtesy of Alessandro Caratelli (CERN EP-ESE))

# New Generation (LHC Run 3)

## Common approach

- **GBT Slow Control Adapter(SCA)**
  - Rad-Hard design from CERN (EP-ESE)
  - Similar Rad-Hardness as GBTx
  - Features:
    - Dual redundant e-links
    - Network controller
    - Arbiter
    - 16x I2C masters
    - 1x JTAG masters
    - 1x SPI masters
    - 32x GPIO
    - 31x mux analogue inputs ADC
    - 4x DAC
    - 1x Auxiliary I2C test port



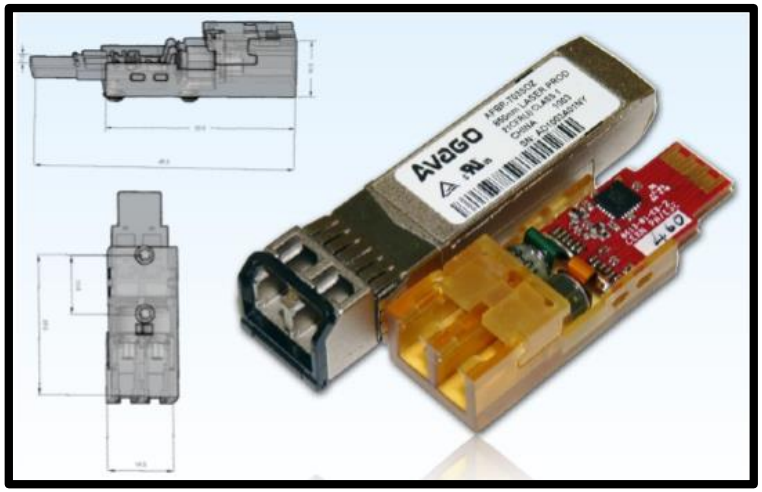

(Diagram courtesy of Alessandro Caratelli (CERN EP-ESE))

# New Generation (LHC Run 3)

## Common approach

- **Versatile Link (VTRx)**
  - Rad-Hard design from CERN (EP-ESE)
  - Line Rate:
    - Up to 5.0 Gbps
  - Transmission/Reception modes:
    - Full-Duplex (Rx/Tx): VTRx
    - Dual Transmitter (Tx/Tx): VTTx
  - Optical transmission:
    - Multi-mode (MM VTRx / MM VTTx) (850 nm)
    - Single-mode (SM VTRx) (1310 nm)
  - Radiation Tolerance:
    - TID > 500 kGy (5x10^14 n/cm2)

VTRx vs SFP+ form factors



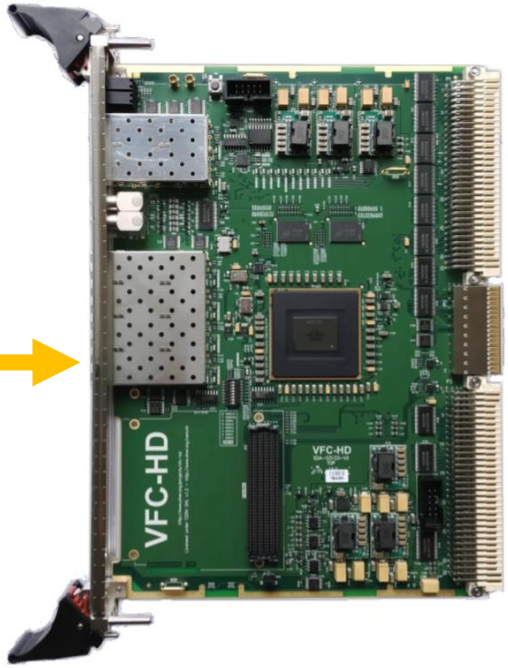

(Diagram courtesy of Jan Troska (CERN EP-ESE))

# New Generation (LHC Run 3)

## Common approach

- Example of GBT/Versatile Link-based project

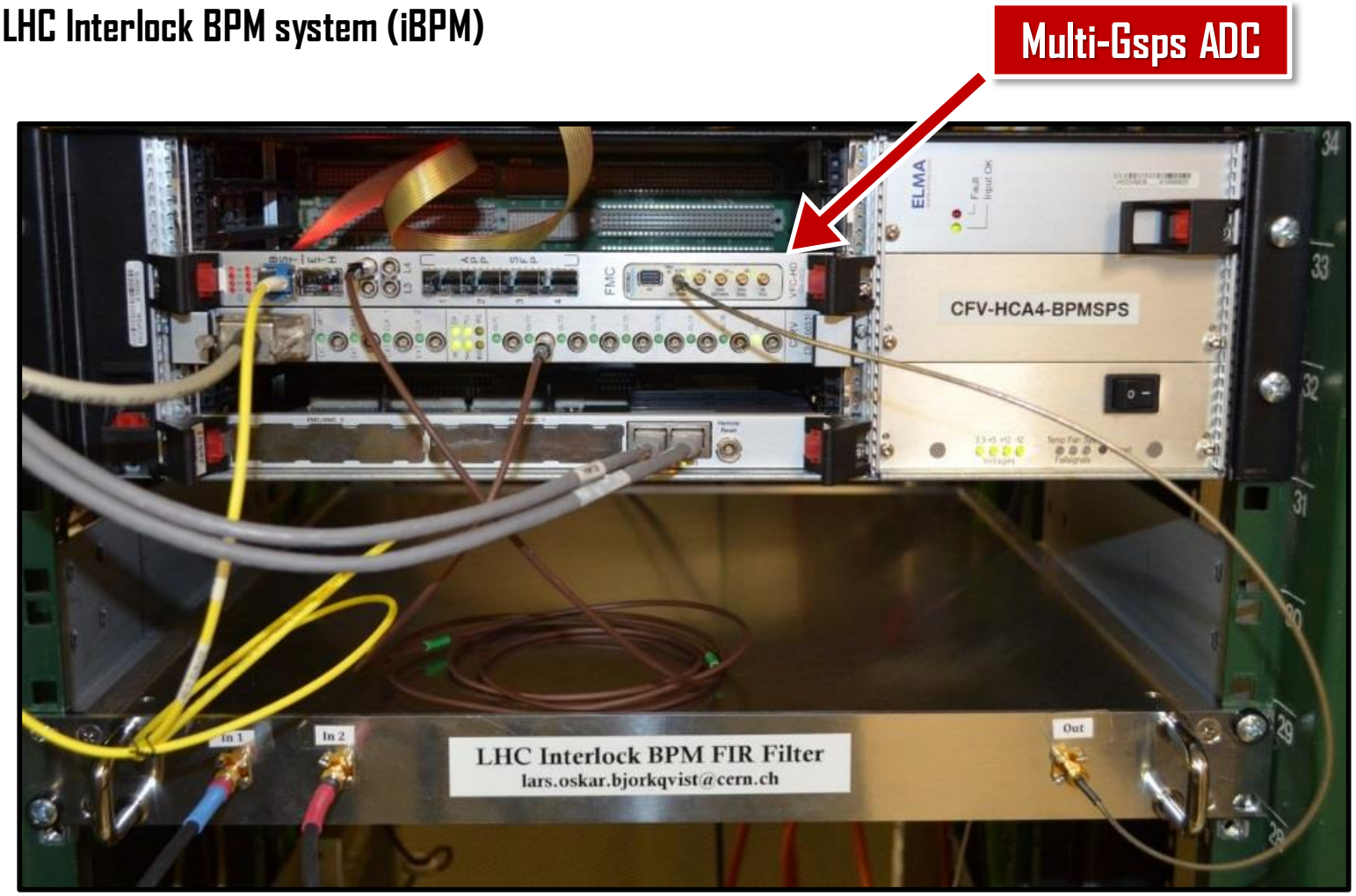
SPS BPM (ALPS) electronics



# New Generation (LHC Run 3)

## Application specific approach

- e.g. LHC Interlock BPM system (iBPM)




More info in Andrea's presentation

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# Next Generation (HL-LHC)

## Common approach

- **Adopted by ATLAS, CMS, LHCb, ALICE…**
- **Non-Rad-Hard Front-End & Back-End electronics based on COTS components**
- **No new Rad-Hard ADC developed at CERN for this generation**
- **Low Power GigaBit Transceiver (LpGBTx)**
  - Rad-Hard design from CERN (EP-ESE)
  - Encoding Protocols:
    - Downstream: FEC12 (Reed-Solomon)
    - Upstream: FEC5 or FEC12 (Reed-Solomon))
  - Asymmetric line rate:
    - Downstream: 2.56 Gbps (1.28 (FEC12) Gbps payload)
    - Upstream: Up to 10.24 Gbps (8.96 (FEC5) or 7.68 (FEC12) Gbps payload)
    - Features extra Slow Control (SC-EC) elink (80 Mbps) (SCA compatible)
  - Latency Deterministic (Downstram/Upstream)
  - Use for Data Readout & Timing, Trigger and Control
  - Subset of SCA features embedded on-chip (e.g. ADC, DAC, I2C, GPIO, etc.)
  - Radiation Tolerance: about 2 times GBTx

# Next Generation (HL-LHC)

## Common approach

- Adopted by SPS BPM, ATLAS, CMS, LHCb, ALICE…
- Non-Rad-Hard Front-End & Back-End electronics based on COTS components
- No new Rad-Hard ADC developed at CERN for this generation
- Low Power GigaBit Transceiver (LpGBTx)

**LpGBT Project Schedule**

Q1-Q3 2018:
- Package procurement and engineering completed
- MPW tapeout 25th July 2018
- Test system: PCB / Software under production

Q4 2018
- Prototypes available (~300 ASICs)
  - Option for additional 300 if all OK

Q1 – Q3 2019:
- Prototype functional testing
- Radiation qualification
- Production testing development

Q4 2019:
- Engineering run

Q3 2020
- Engineering ASICs (~40k) available to the users

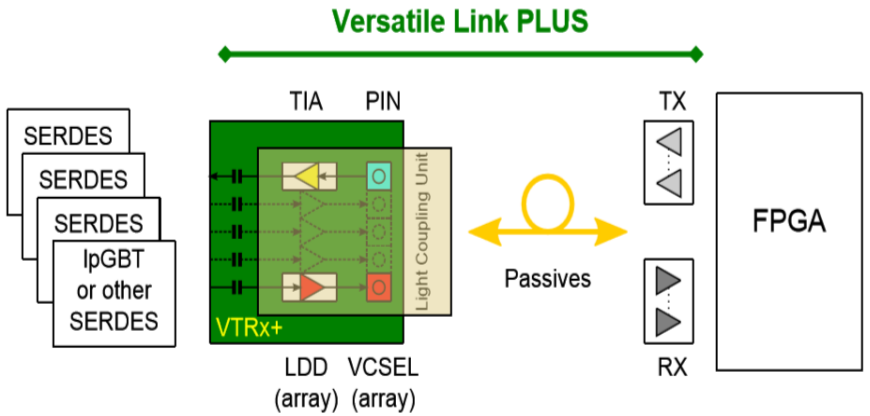
Q3 2021:
- Production completed (~100k ASICs)

# Next Generation (HL-LHC)

## Common approach

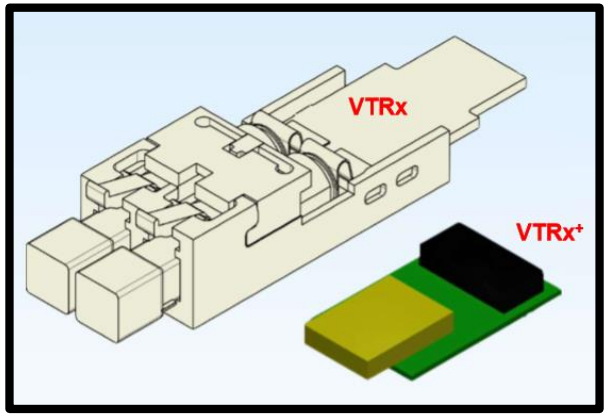
- **Versatile Link PLUS (VTRx+)**
  - Rad-Hard design from CERN (EP-ESE)
  - Line Rate:
    - Tx: Up to 10.0 Gbps
    - Rx: Up to 2.5 Gbps
  - Transmission/Reception modes:
    - Up to 4 Tx + Up to 1 Rx
  - Optical transmission:
    - Multi-mode only (850nm VCSEL)
  - Radiation Tolerance:
    - TID > 1 MGy (5x10^15 hadrons/cm2)
  - Project Schedule:
    - Proof of concept (Apr 2014 - Oct 2015)
    - Feasibility demonstration (Oct 2015 – Apr 2017)
    - Pre-production readiness (Apr 2017 – Oct 2018)
  - Pieces to be produced: ~50k

Versatile Link PLUS diagram

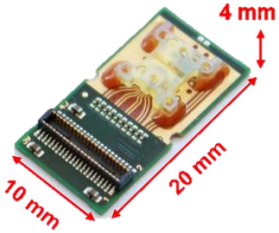



(Diagram courtesy of Csaba Soós (CERN EP-ESE))

VTRx vs VTRx+ form factor




VTRx+ dimensions



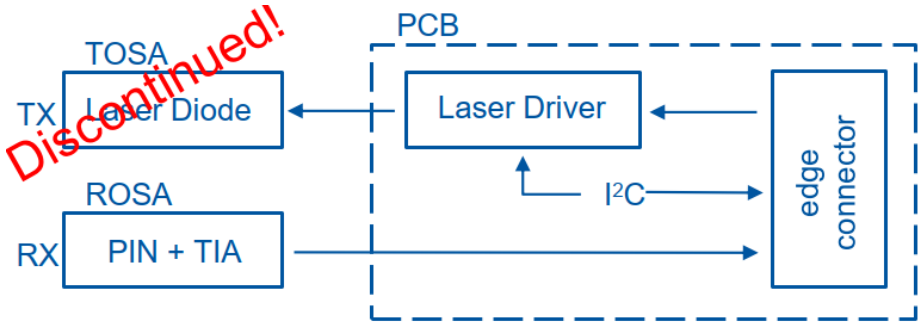

(Diagram courtesy of Francois Vasey (CERN EP-ESE))

# Next Generation (HL-LHC)

## Common approach

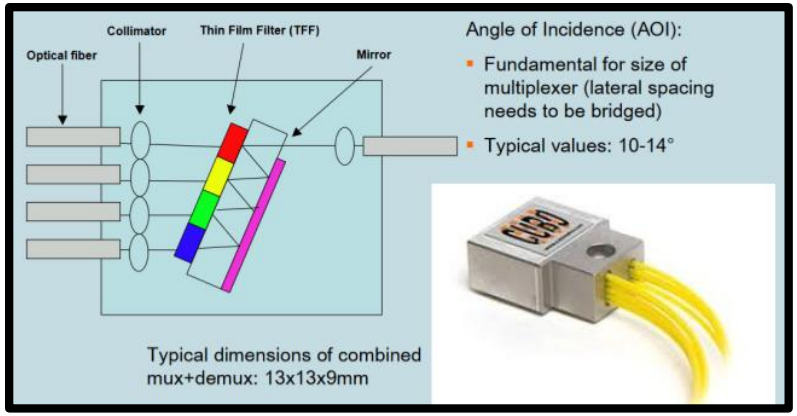
- **New VTRx SM**
  - Rad-Hard design from CERN (EP-ESE)
  - Line Rate:
    - Up to 10.0 Gbps (GBTx & LpGBTx compatible)
  - Transmission/Reception modes:
    - Full-Duplex (Rx/Tx): VTRx
    - Up to 4 Tx + 1 Rx (Using additional CWDM*)
  - Optical transmission:
    - Single-mode in four colours (1270, 1290, 1310, 1330 nm)
  - Form factor SFP+ compatible under study
  - Radiation Tolerance:
    - New VTRx SM: TID > 500 kGy (5x10^14 n/cm2)
    - CWDM: Still under study

VTRx diagram




(Diagram courtesy of Carmelo Scarcela (CERN EP-ESE))

CWDM 4 to 1 MUX/DEMUX diagram & image




(Diagram courtesy of Carmelo Scarcela (CERN EP-ESE))

* Coarse Wavelength Division Multiplexing (CWDM)

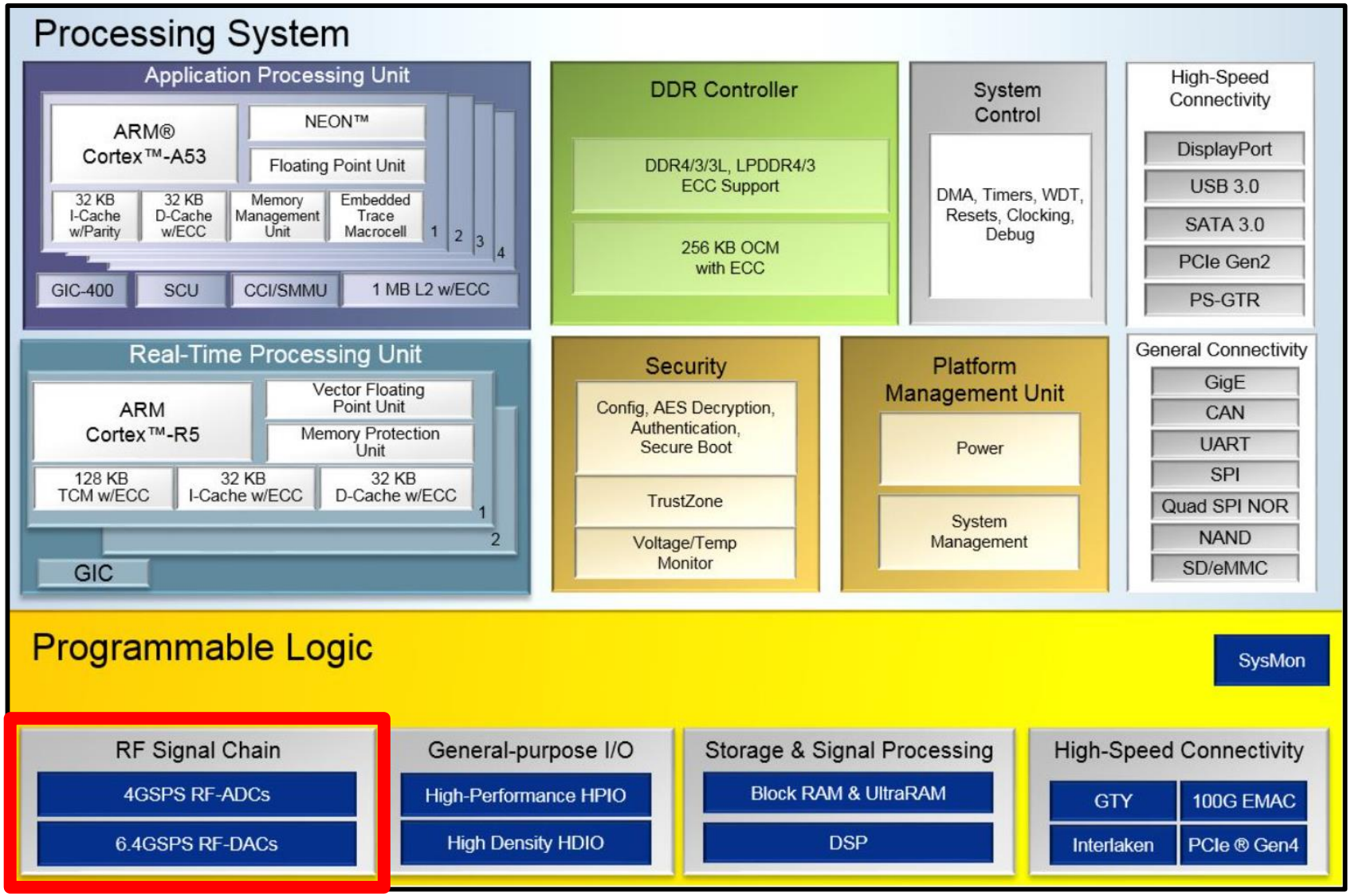
# Next Generation (HL-LHC)

## Application specific data links

- e.g. LHC BPM Upgrade

More info in Andrea's presentation

Example diagram of SoC FPGA with embedded ADC/DAC



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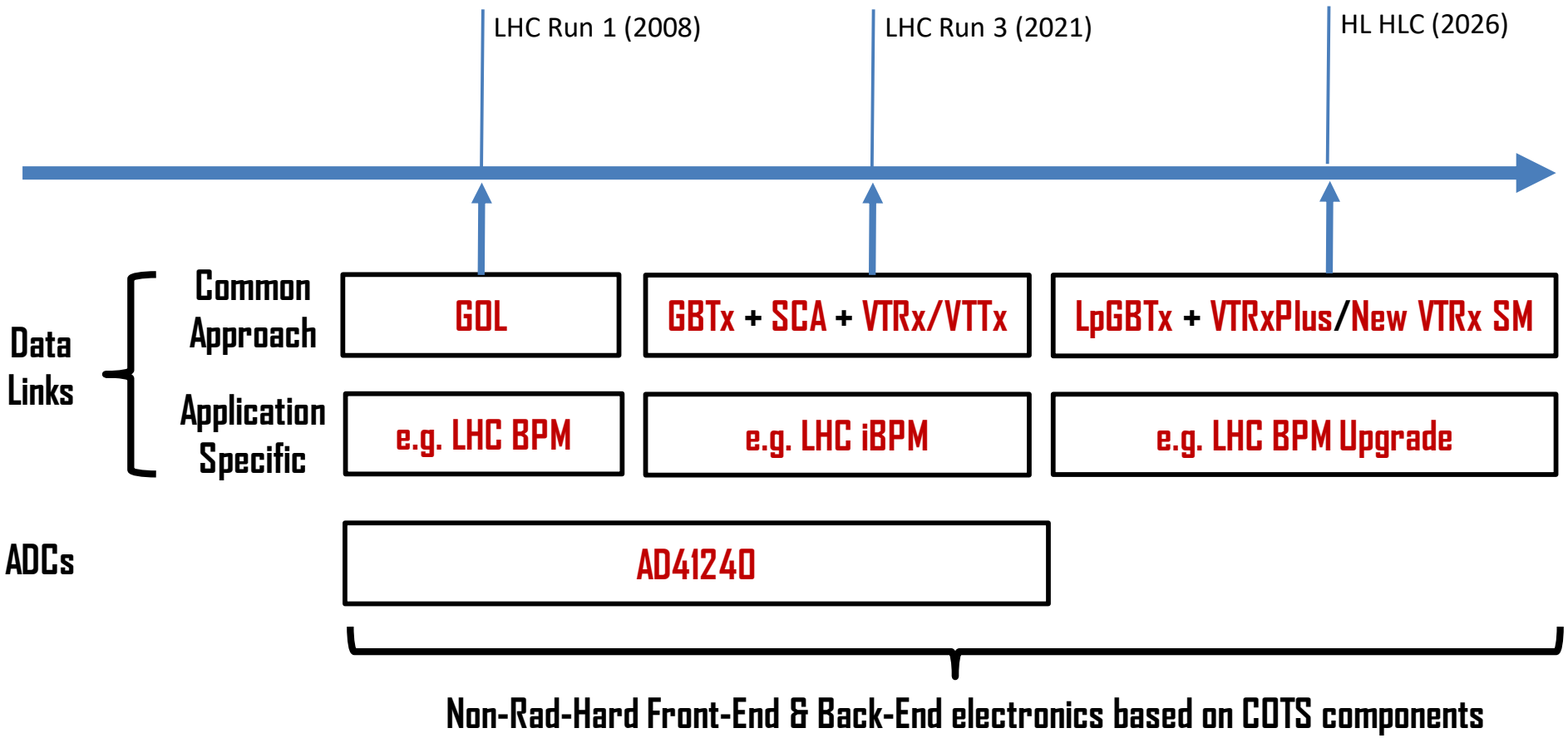
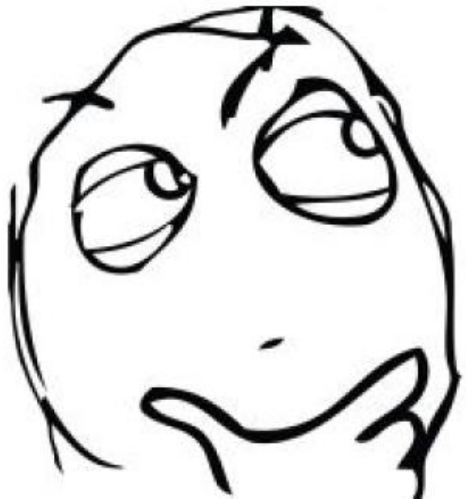
# Summary


LHC Run 1 (2008)
LHC Run 3 (2021)
HL HLC (2026)
Data Links
Common Approach
GOL
GBTx + SCA + VTRx/VTTx
LpGBTx + VTRxPlus/New VTRx SM
Application Specific
e.g. LHC BPM
e.g. LHC iBPM
e.g. LHC BPM Upgrade
ADCs
AD41240
Non-Rad-Hard Front-End & Back-End electronics based on COTS components

# Any Question?



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