New SPring-8 Bunch-by-Bunch Feedback Processor for Hybrid Filling

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POHANG ACCELERATOR LABORATORY / PLS-II

The Joint ARIES Workshop on Electron and Hadron Synchrotrons:
Next Generation Beam Position Acquisition and Feedback Systems
ALBA Synchrotron, November 12 - 14, 2018.

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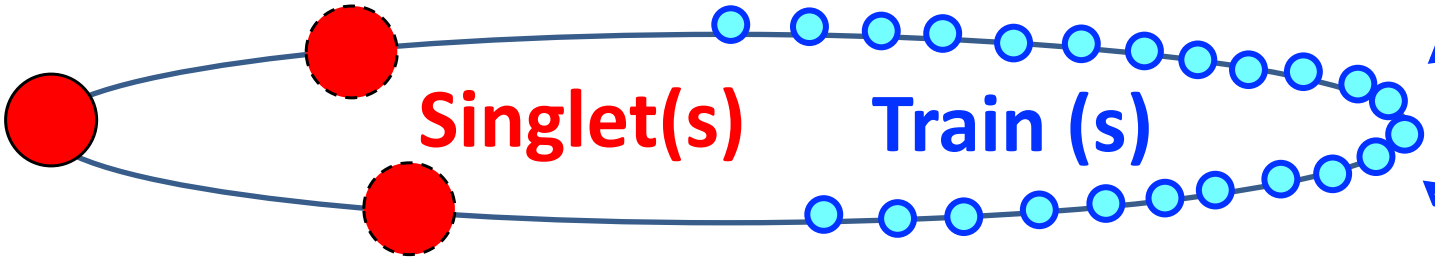
Transverse Feedback for Hybrid Filling

Hybrid Filling

Singlets
(**High** Bunch Current)

+

Trains (Low Bunch Current,
High stored current)



Single-bunch Instabilities

Mode-coupling

Beam pipe broad band impedance,
Resistive-wall, tapers of In-Vacuum IDs

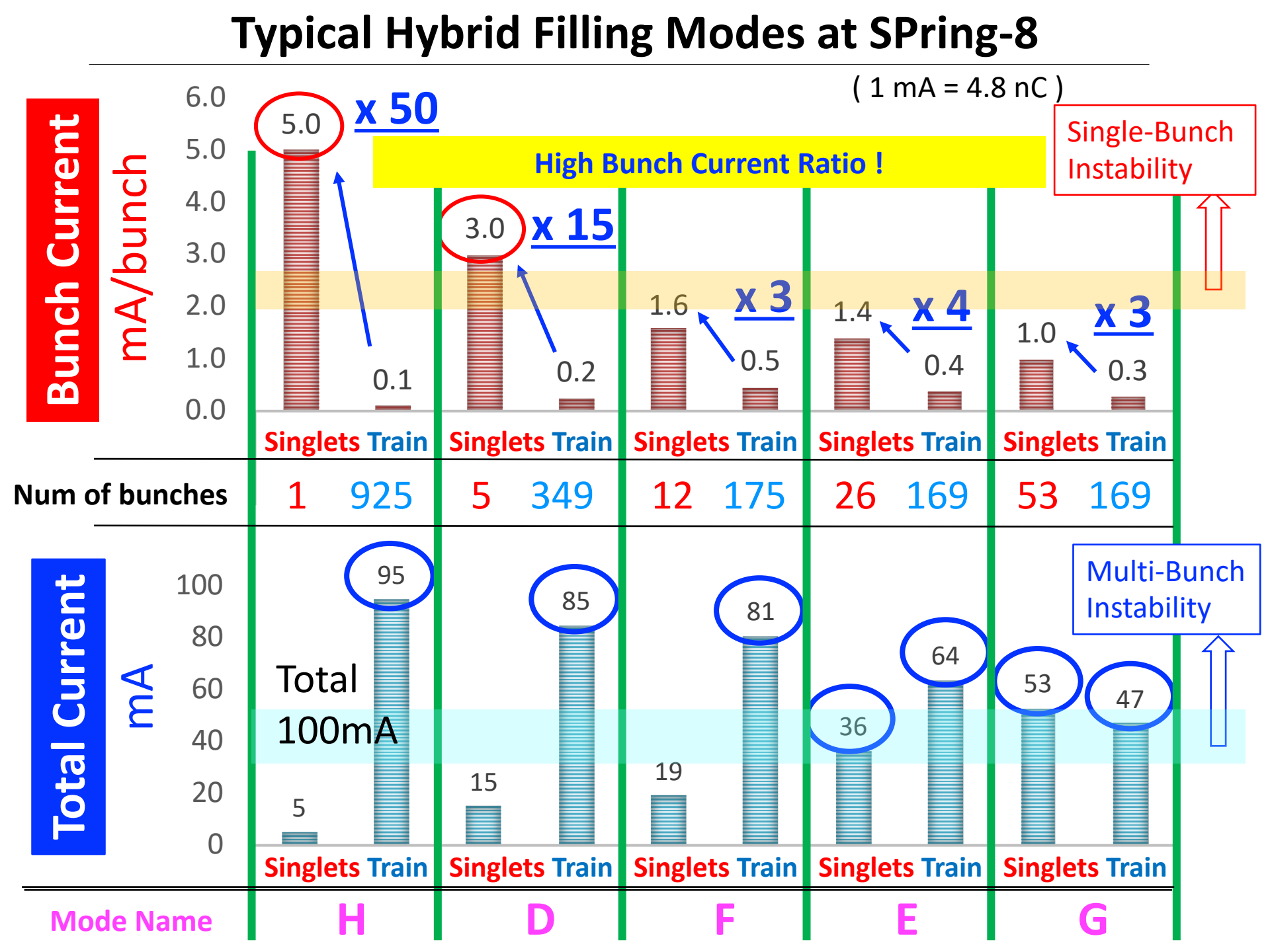
Multi-bunch Instabilities

Resistive-wall of in-vacuum IDs
Cavity HOM

"Simultaneous Suppression"

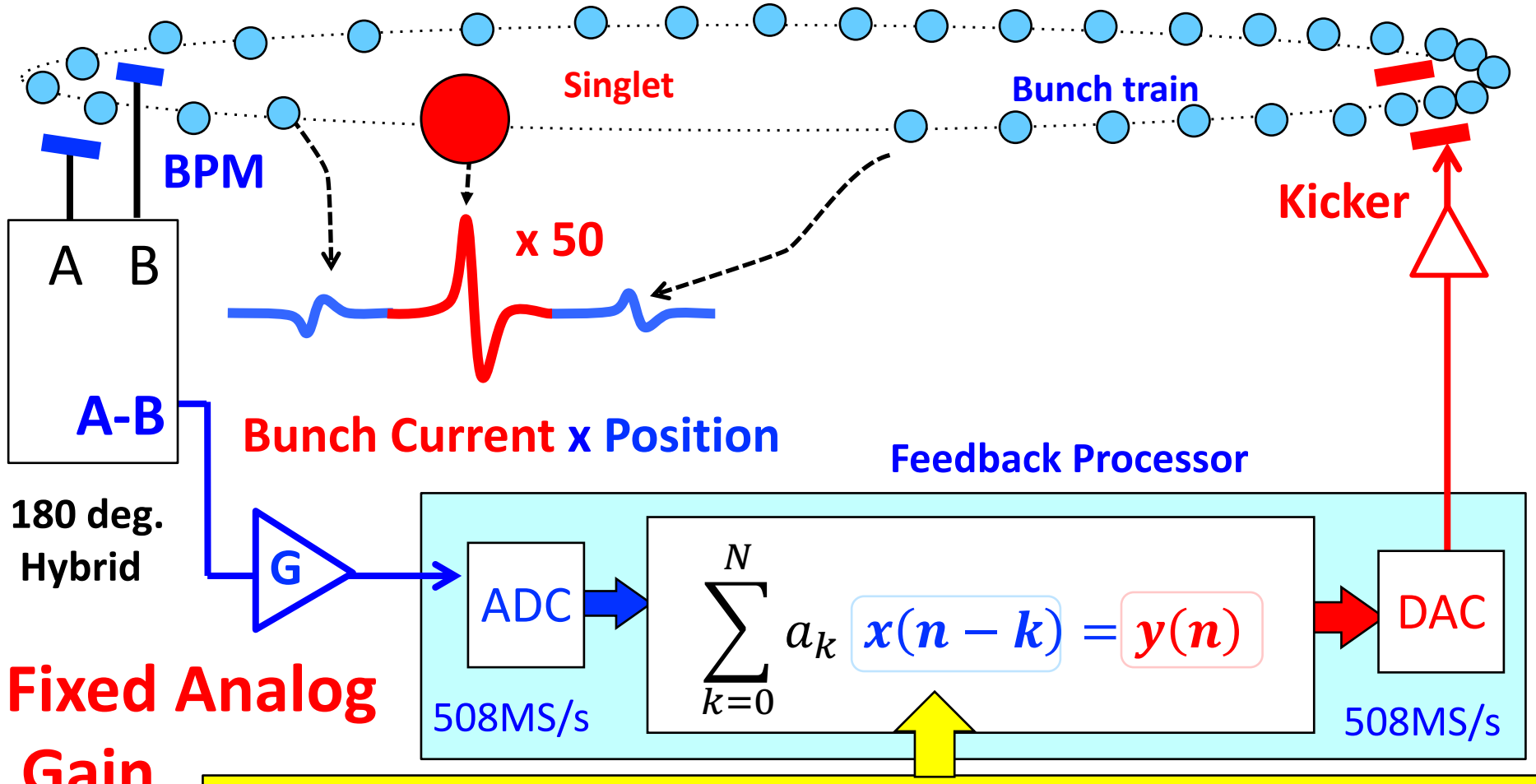
Transverse Bunch-by-bunch Feedback System

Typical Hybrid Filling Modes at SPring-8



Single Front-end Feedback

Usual Feedback Processor with Single ADC and Single Front-end



Feedback Gain ∝ BPM Signal Strength ∝ **Bunch Current**

=> Digital Gain Switching for bunch current

for compensation of feedback gain

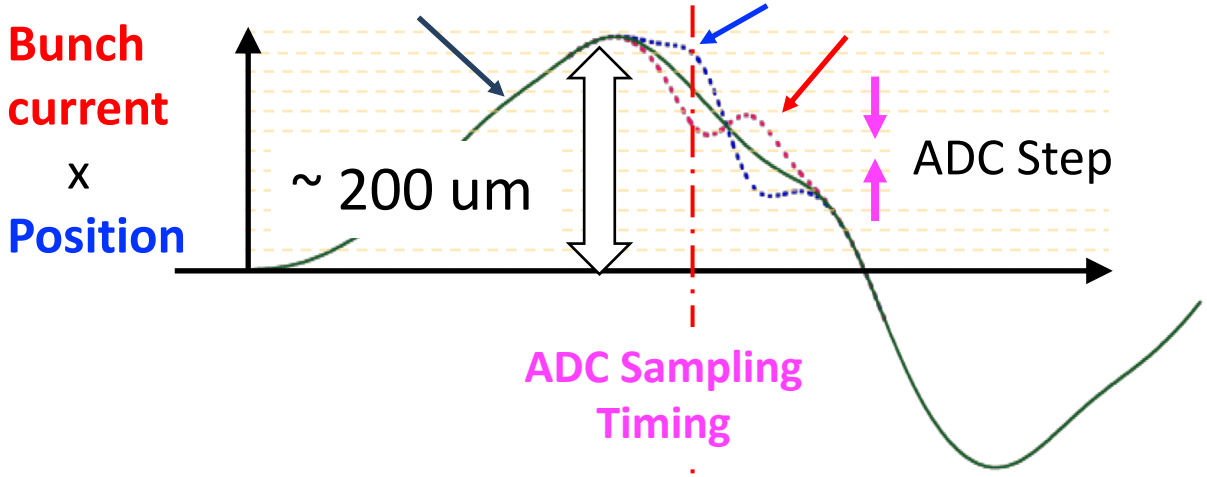
Single Front-end = Fixed Analog Gain

BPM Signal (A-B)

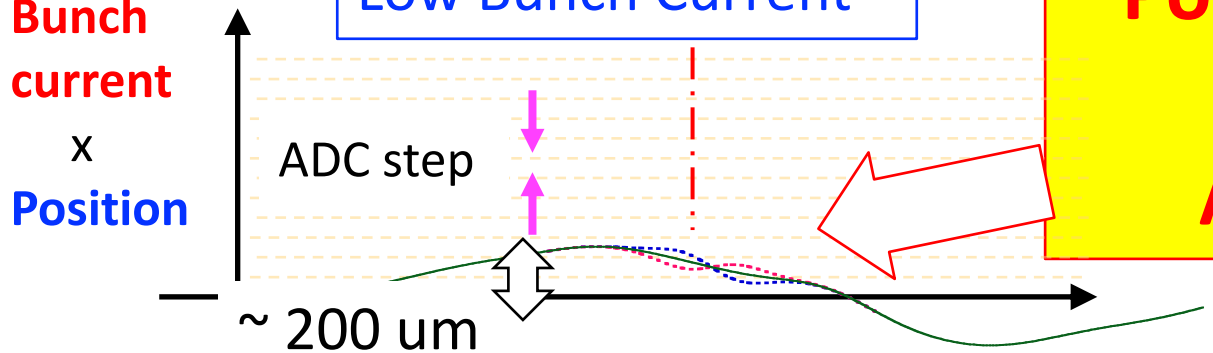
High Bunch Current

Offset signal

Position dependent Signal
~ um (required)



Low Bunch Current



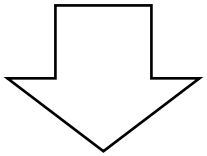
Offset signal

Unbalance of BPM structure, Cabling, Reflection

Observed in many rings

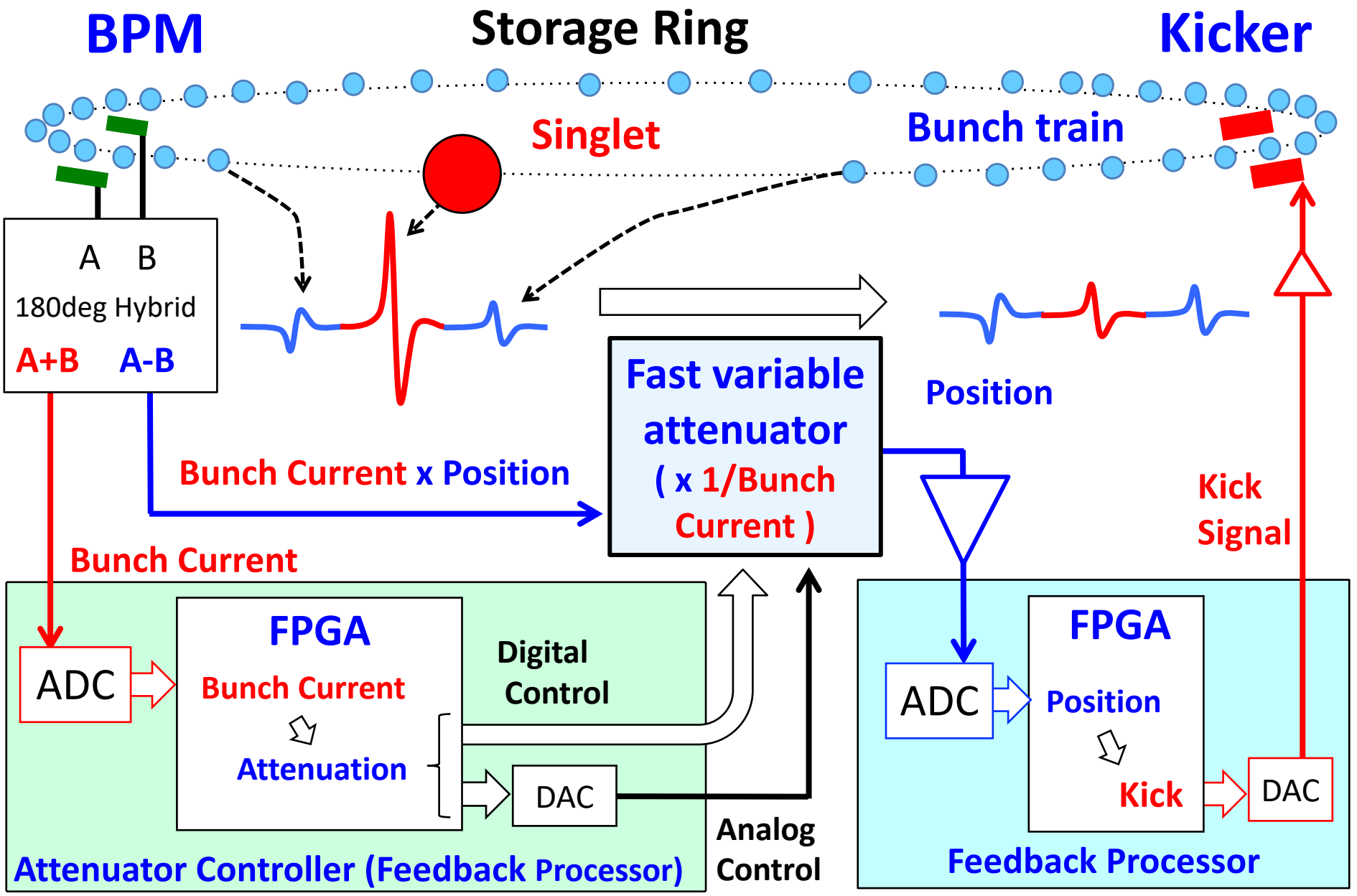
Position Resolution limited by ADC resolution

Fixed Analog Gain + **Digital Gain** Switching



Analog Gain Switching

Analog Gain switching by Fast Variable Attenuator



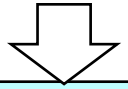
K. Kobayashi, T. Nakamura, THB006, ICALEPCS'09. (T. Nakamura, K. Kobayashi, et al., THPC127, EPAC08.)

Analog Gain switching by Fast Variable Attenuator

Complex system

* Two Processors
* Fast Variable Attenuators

Less S/N ratio for high bunch current



New SPring-8 Feedback Processor*

Switching

{ Front-end (analog gain) + ADC } sets

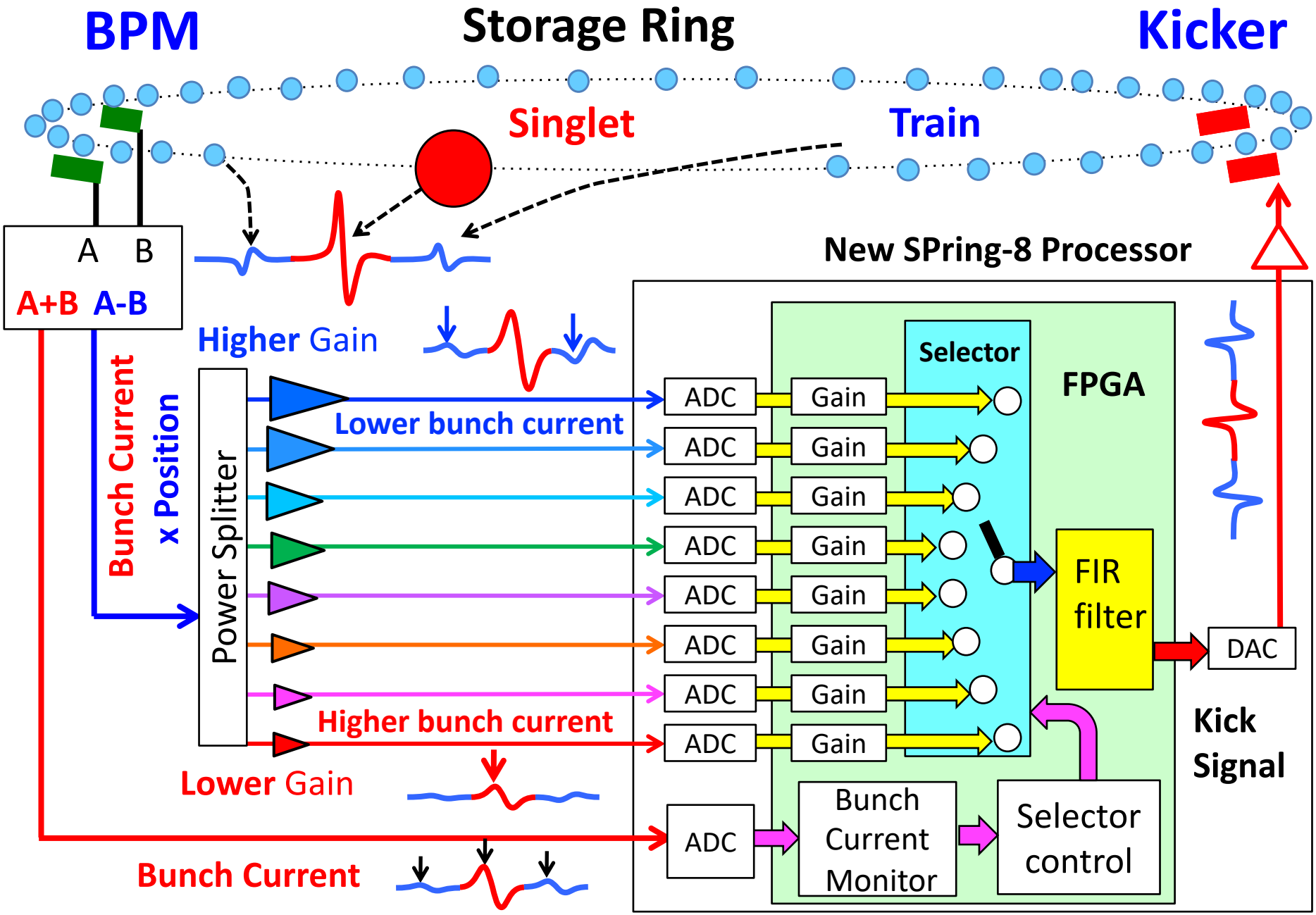
for bunch current

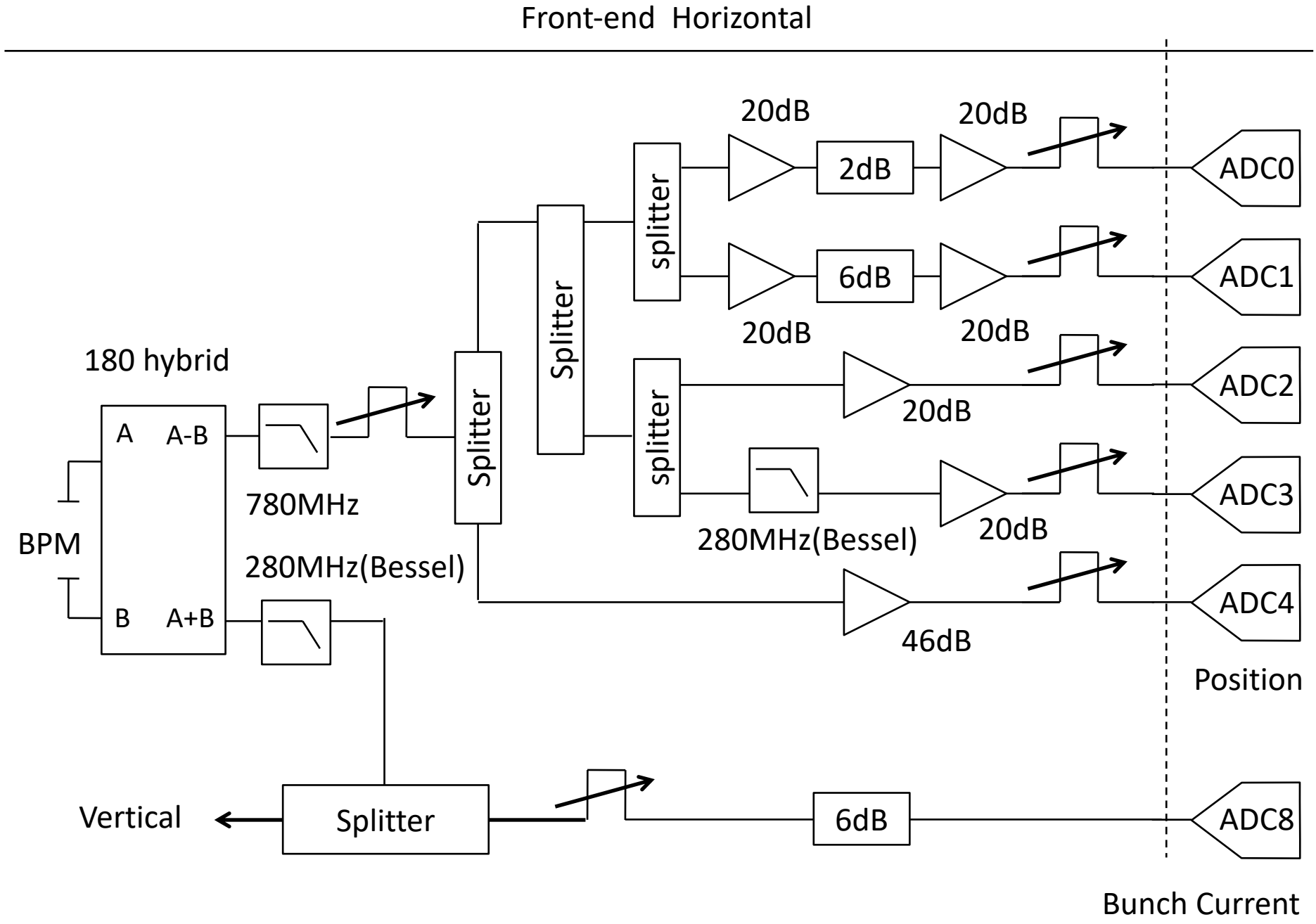
Design : JASRI/SPring-8 with the advice of SOLEIL and PAL / PLS-II

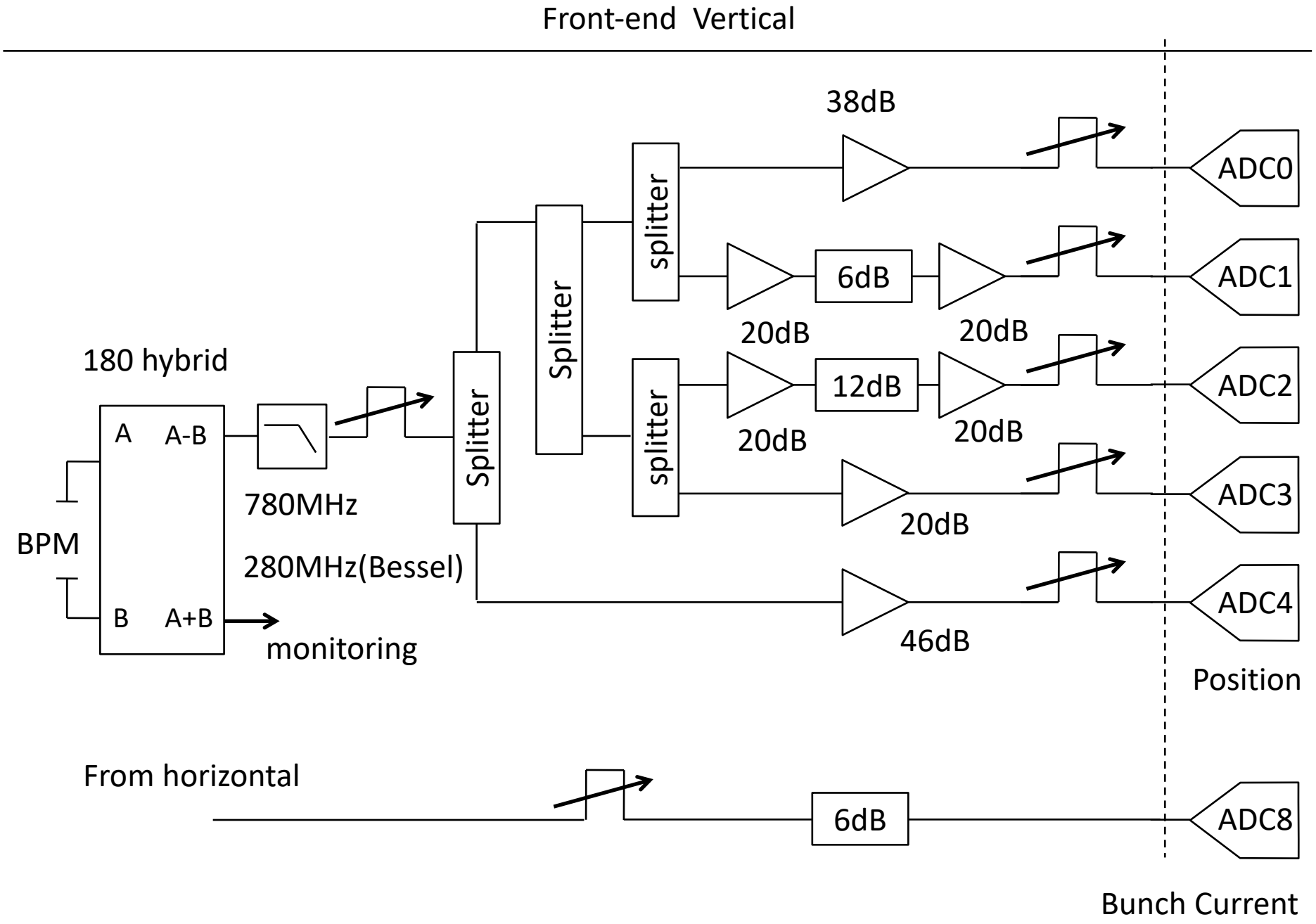
Manufacturing and initial programing :

Tokyo Electron Device (TED, www.teldevice.co.jp)

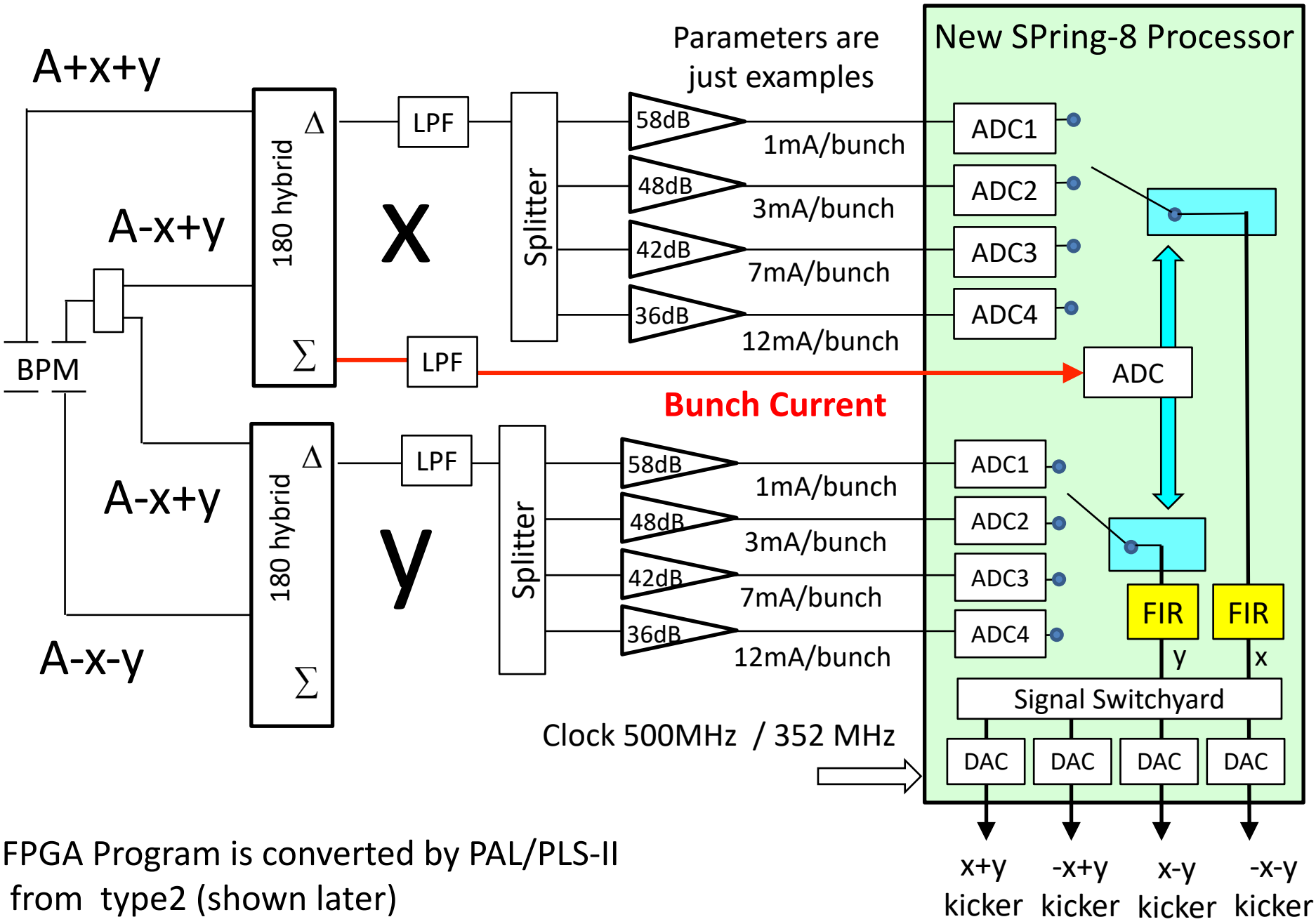
New SPring-8 Feedback Processor (in operation 2016-)




Front-end Horizontal
20dB
20dB
2dB
ADC0
splitter
6dB
ADC1
20dB
20dB
180 hybrid
Splitter
splitter
ADC2
20dB
A
A-B
780MHz
Splitter
splitter
ADC3
280MHz(Bessel)
20dB
BPM
280MHz(Bessel)
ADC4
46dB
B
A+B
Position
Vertical
Splitter
6dB
ADC8
Bunch Current

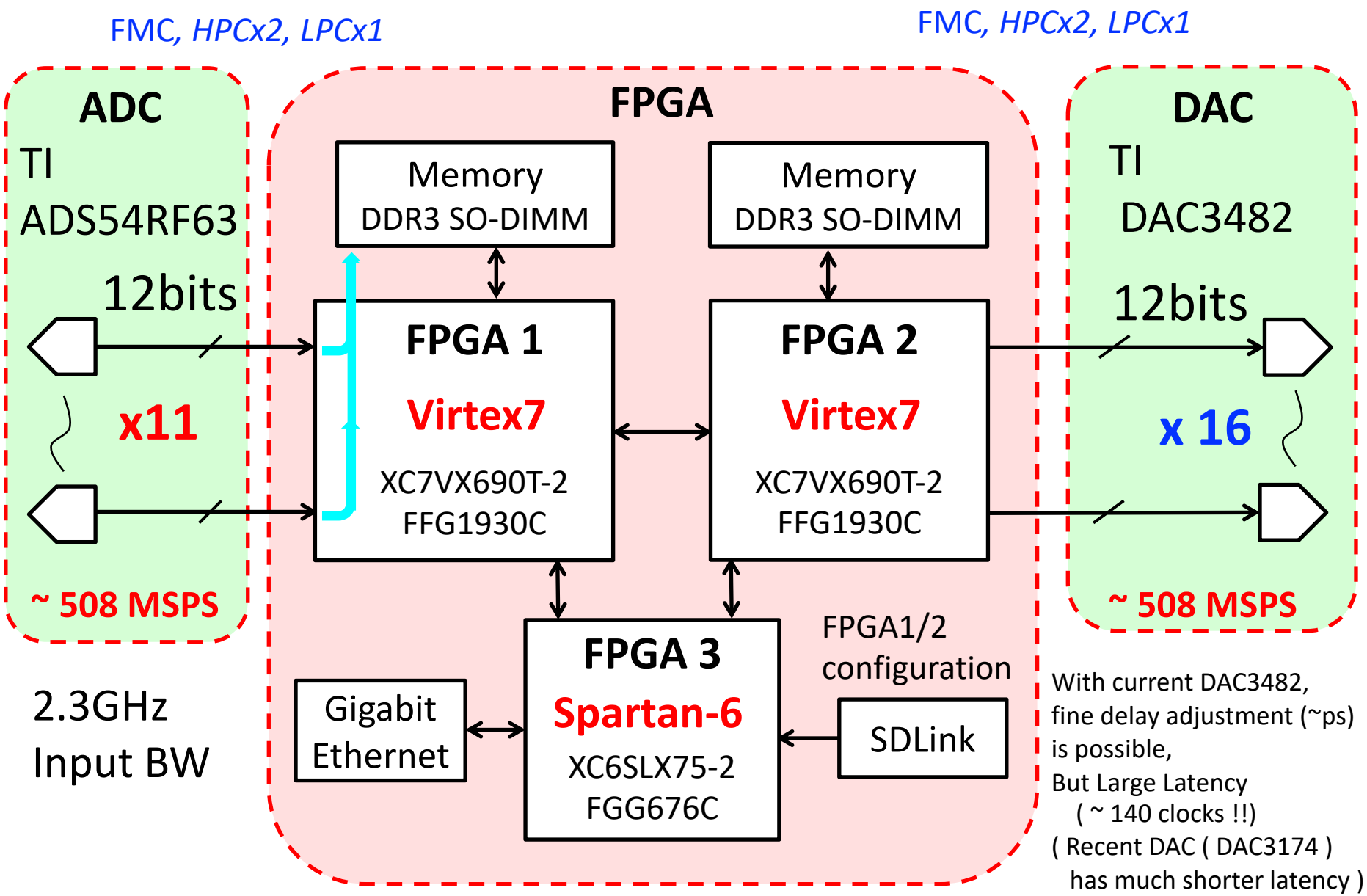

Front-end Vertical
38dB
ADC0
splitter
6dB
ADC1
20dB
20dB
180 hybrid
Splitter
12dB
ADC2
splitter
20dB
20dB
A
A-B
780MHz
Splitter
ADC3
20dB
BPM
280MHz(Bessel)
ADC4
B
A+B
46dB
monitoring
Position
From horizontal
6dB
ADC8
Bunch Current

For Hybrid Filling for PLS-II : H and V in one processor



FPGA Program is converted by PAL/PLS-II from type2 (shown later)

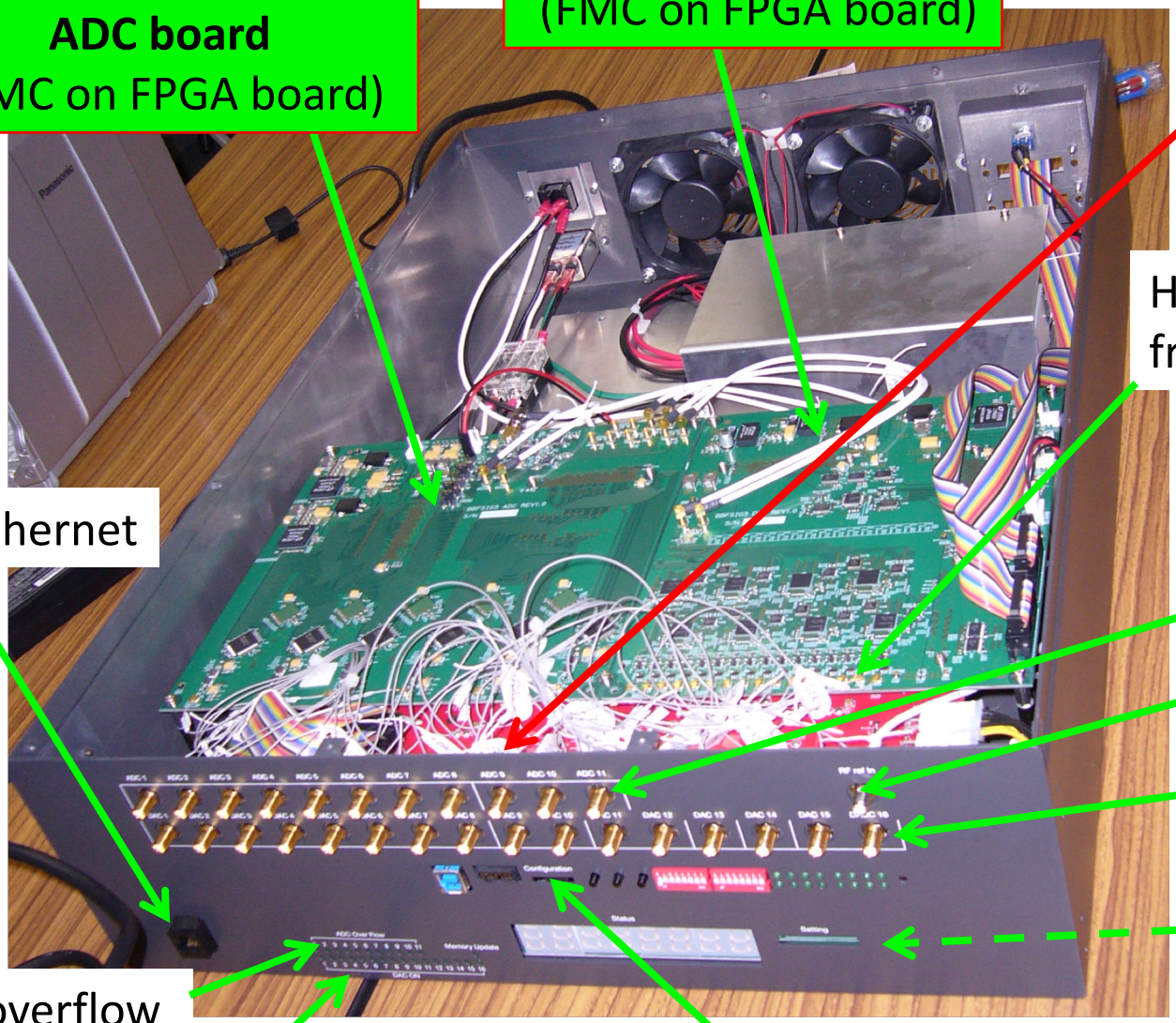
Hardware Block Diagram



http://www.design-gateway.com/SDLink.html

Kazuo KOBAYASHI / SPring-8

New SPring-8 Signal Processor (upside down)



DAC board
(FMC on FPGA board)

ADC board
(FMC on FPGA board)

FPGA board
(red board)

Hirose U.FL connectors
from/to board

Gb Ethernet

ADC inputs (11)

Clock (RF ref.)

DAC outputs (16)

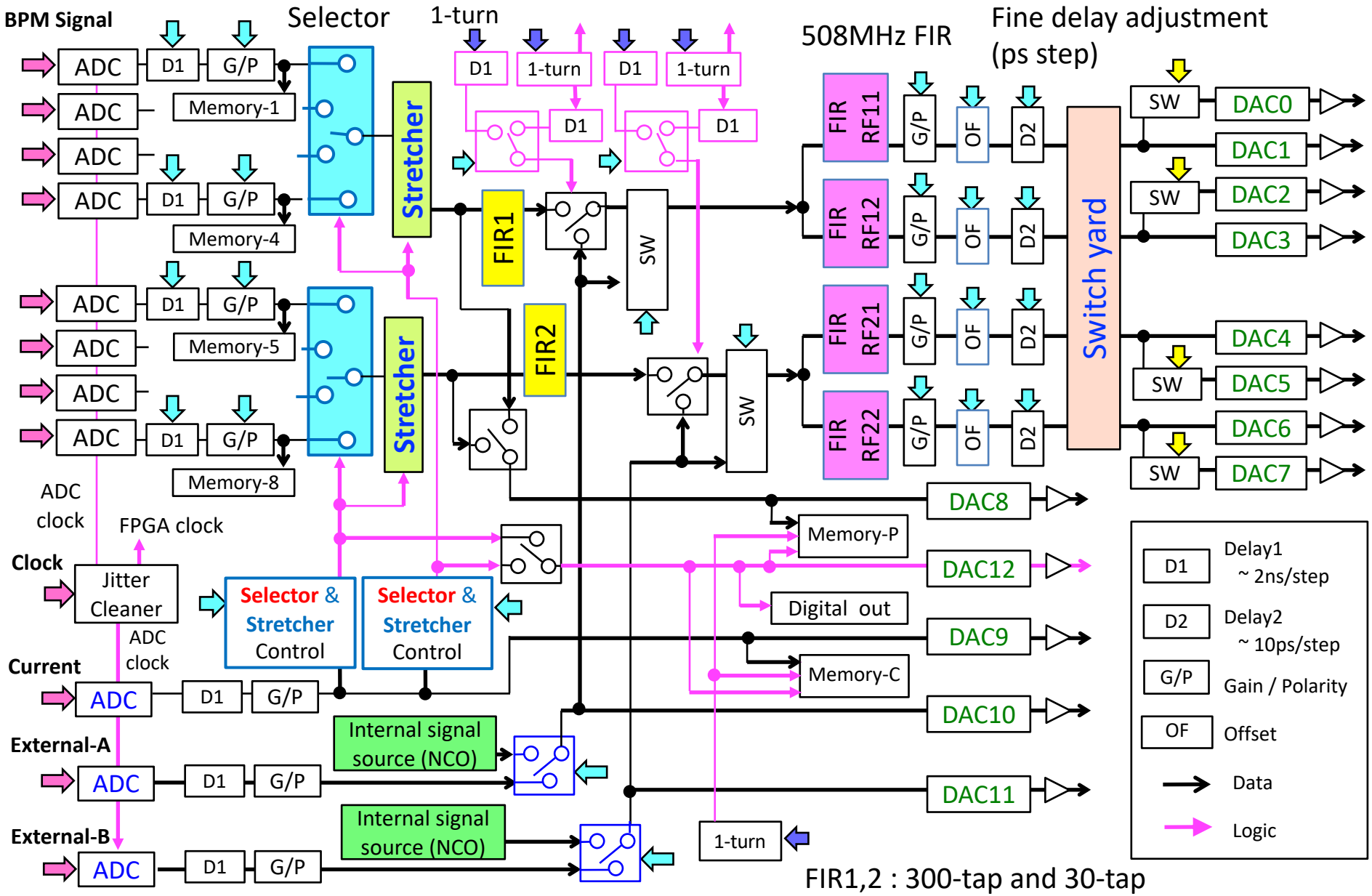
SD card slot
for parameter file
(not implemented)

ADC overflow
indicators

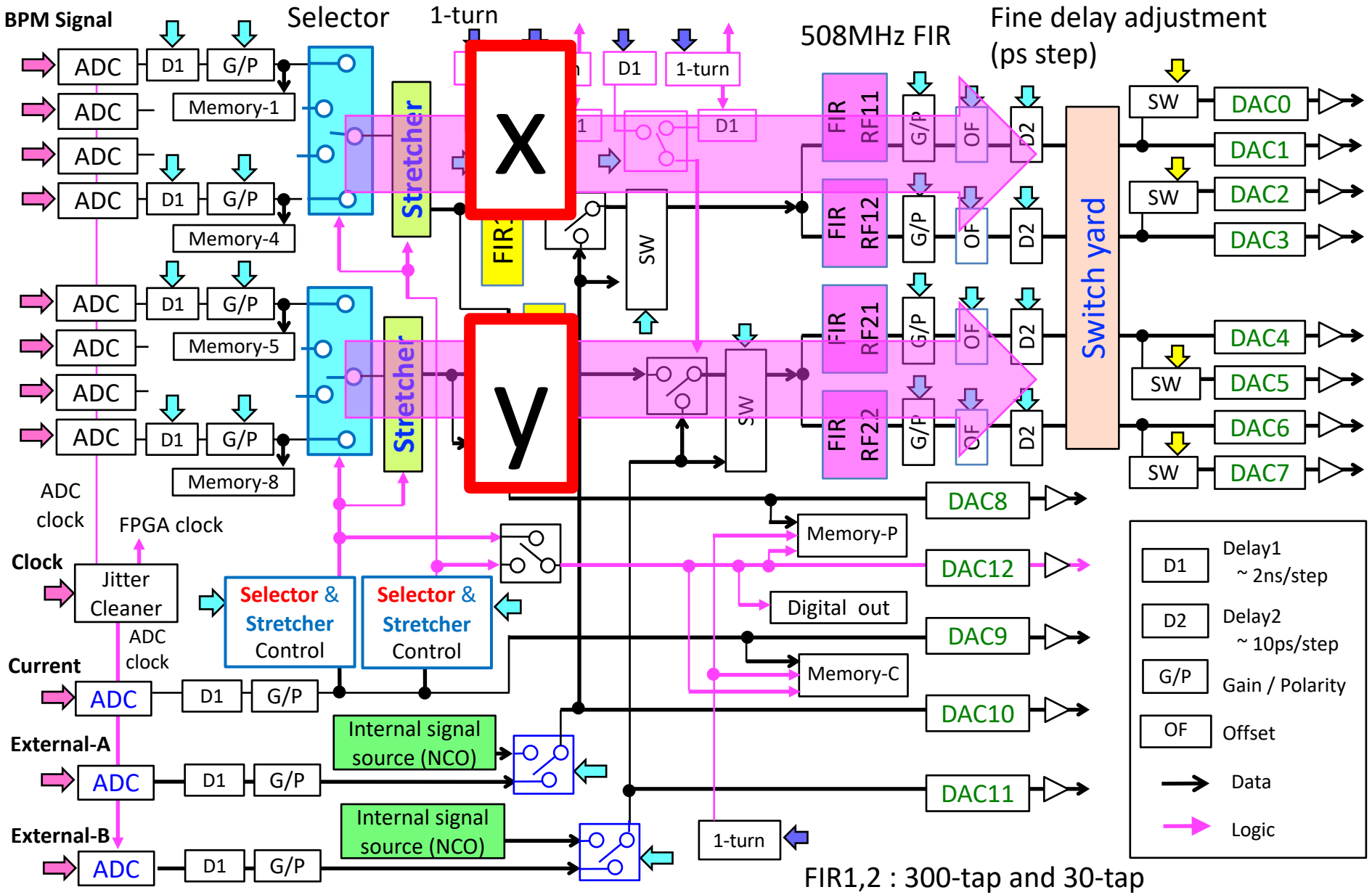
DAC on/off indicators

micro SD slot for configuration

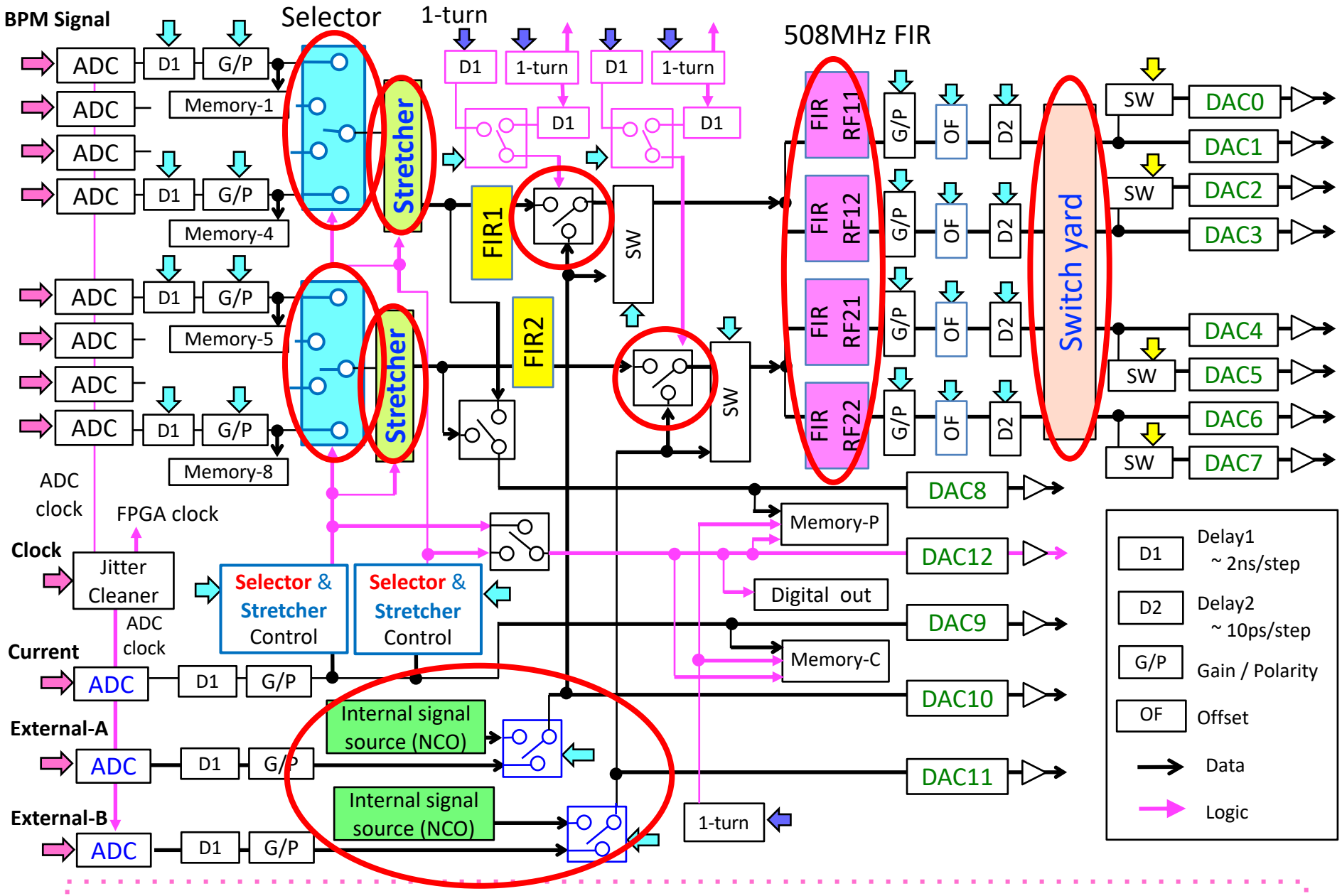
Function Block Diagram



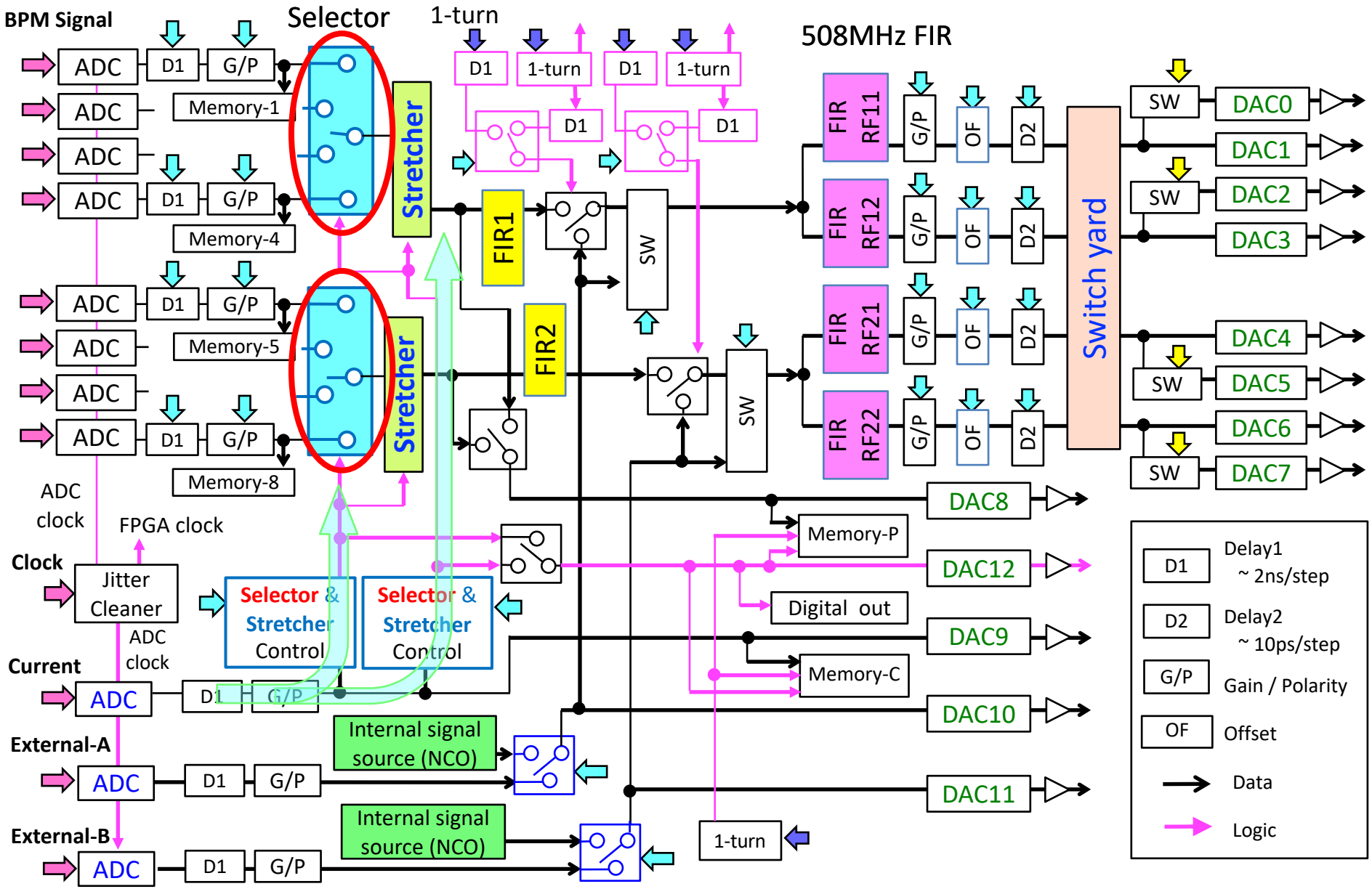
Function Block Diagram



Gadgets


BPM Signal
Selector
1-turn
508MHz FIR
ADC
D1
G/P
Memory-1
Memory-4
Memory-5
Memory-8
Stretcher
FIR1
FIR2
SW
1-turn
FIR RF11
FIR RF12
FIR RF21
FIR RF22
OF
D2
Switch yard
DAC0
DAC1
DAC2
DAC3
DAC4
DAC5
DAC6
DAC7
DAC8
DAC9
DAC10
DAC11
DAC12
Memory-P
Memory-C
Digital out
ADC clock
FPGA clock
Clock
Jitter Cleaner
Selector & Stretcher Control
Current
External-A
External-B
Internal signal source (NCO)
Delay1 ~ 2ns/step
Delay2 ~ 10ps/step
Gain / Polarity
Offset
Data
Logic
Analog input
Digital input
Ethernet control
Digital input & Ethernet Cont.

Selection of ADC with Bunch Current Controlled Selector



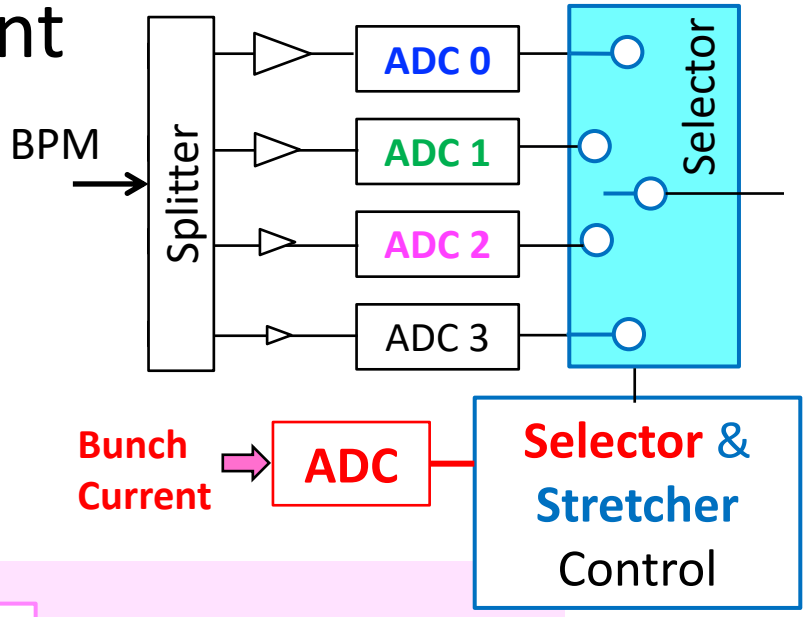
Selector Control with anti-chattering

ADC Selection for bunch current

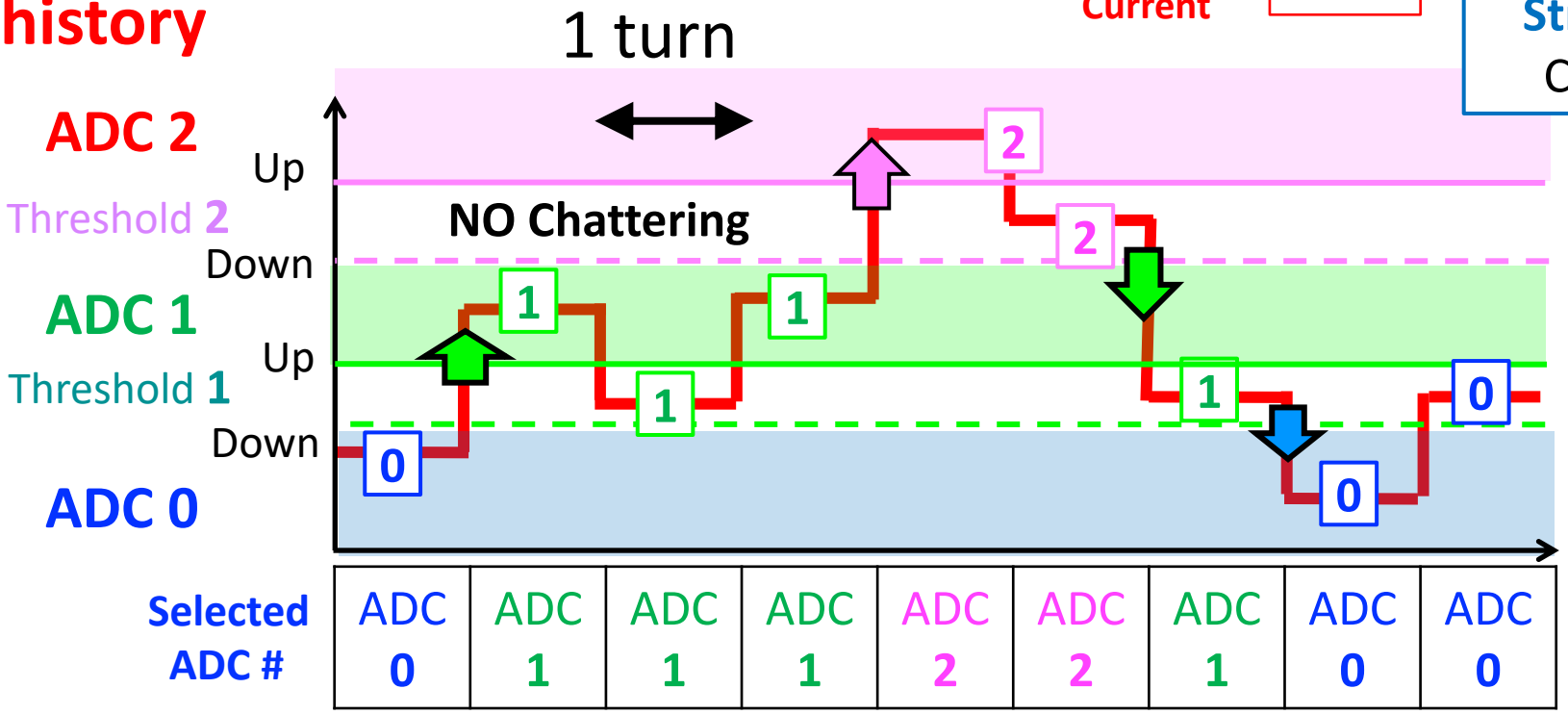
Anti-chattering by

Up-ward threshold and

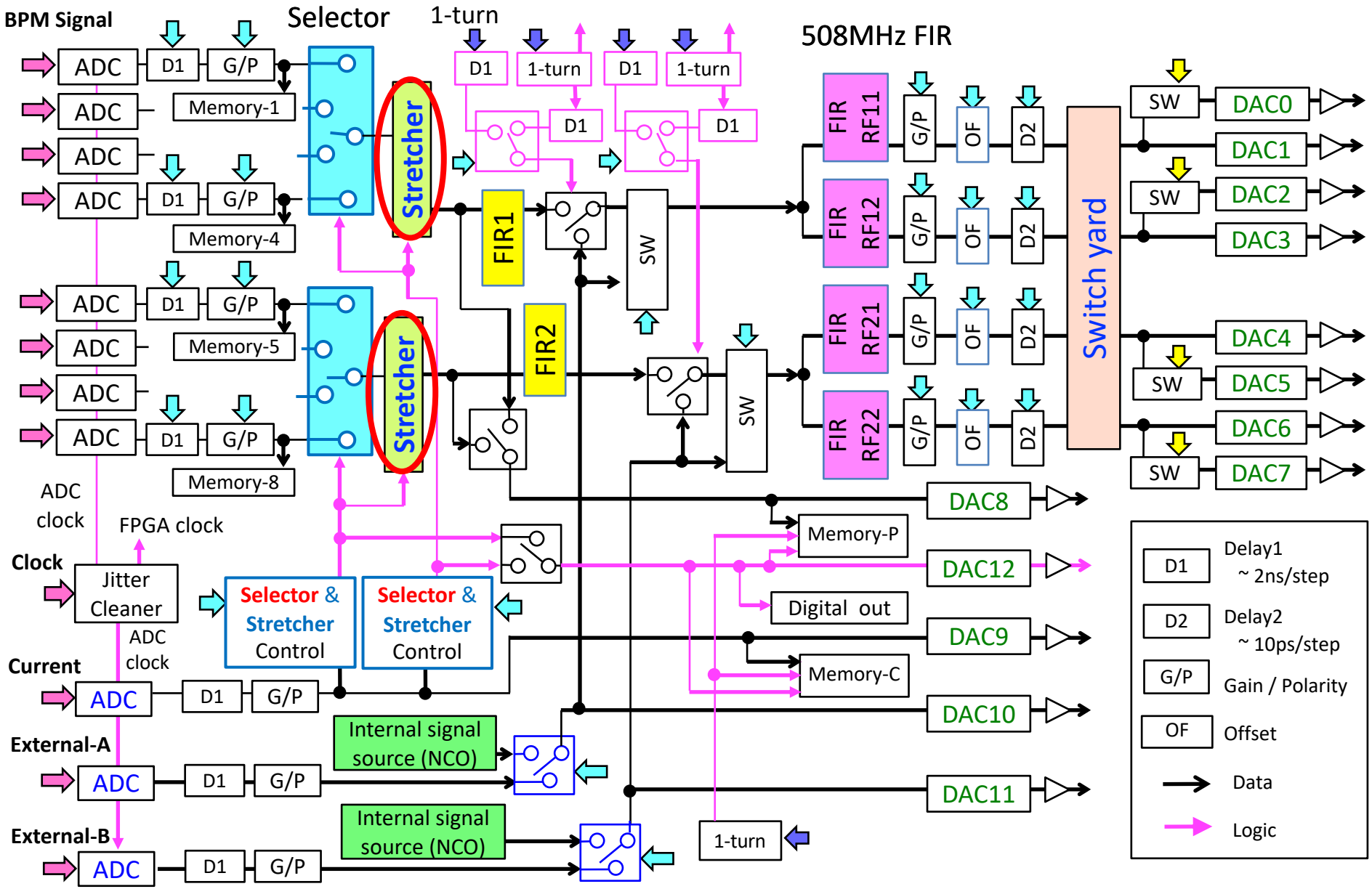
Down-ward threshold



Turn-by-turn Bunch current history



Stretcher


BPM Signal
Selector
1-turn
508MHz FIR
ADC
D1
G/P
Memory-1
Memory-4
Memory-5
Memory-8
Stretcher
FIR1
FIR2
SW
FIR RF11
FIR RF12
FIR RF21
FIR RF22
OF
D2
Switch yard
DAC0
DAC1
DAC2
DAC3
DAC4
DAC5
DAC6
DAC7
DAC8
DAC9
DAC10
DAC11
DAC12
Memory-P
Memory-C
Digital out
ADC clock
FPGA clock
Clock
Jitter Cleaner
Selector & Stretcher Control
Current
External-A
External-B
Internal signal source (NCO)
Delay1 ~ 2ns/step
Delay2 ~ 10ps/step
Gain / Polarity
Offset
Data
Logic
Analog input
Digital input
Ethernet control
Digital input & Ethernet Cont.

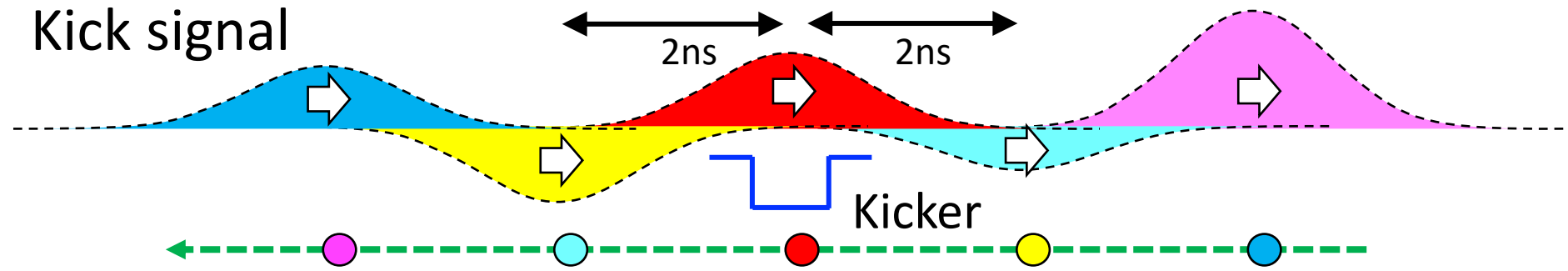
Stretcher

For Isolated bunch (high current singlets)

Kick Pulse Length is **Stretched** for **Full usage of kicker length**

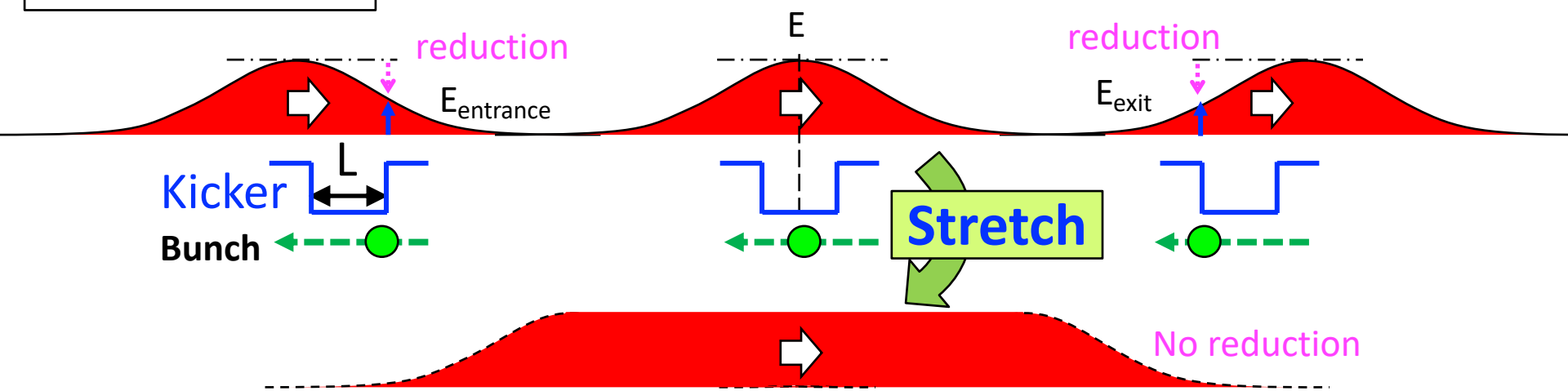
Bucket-by-bucket (train)

Kick pulse for Each Bunch is not long enough for Time constant (filling time) of Kicker

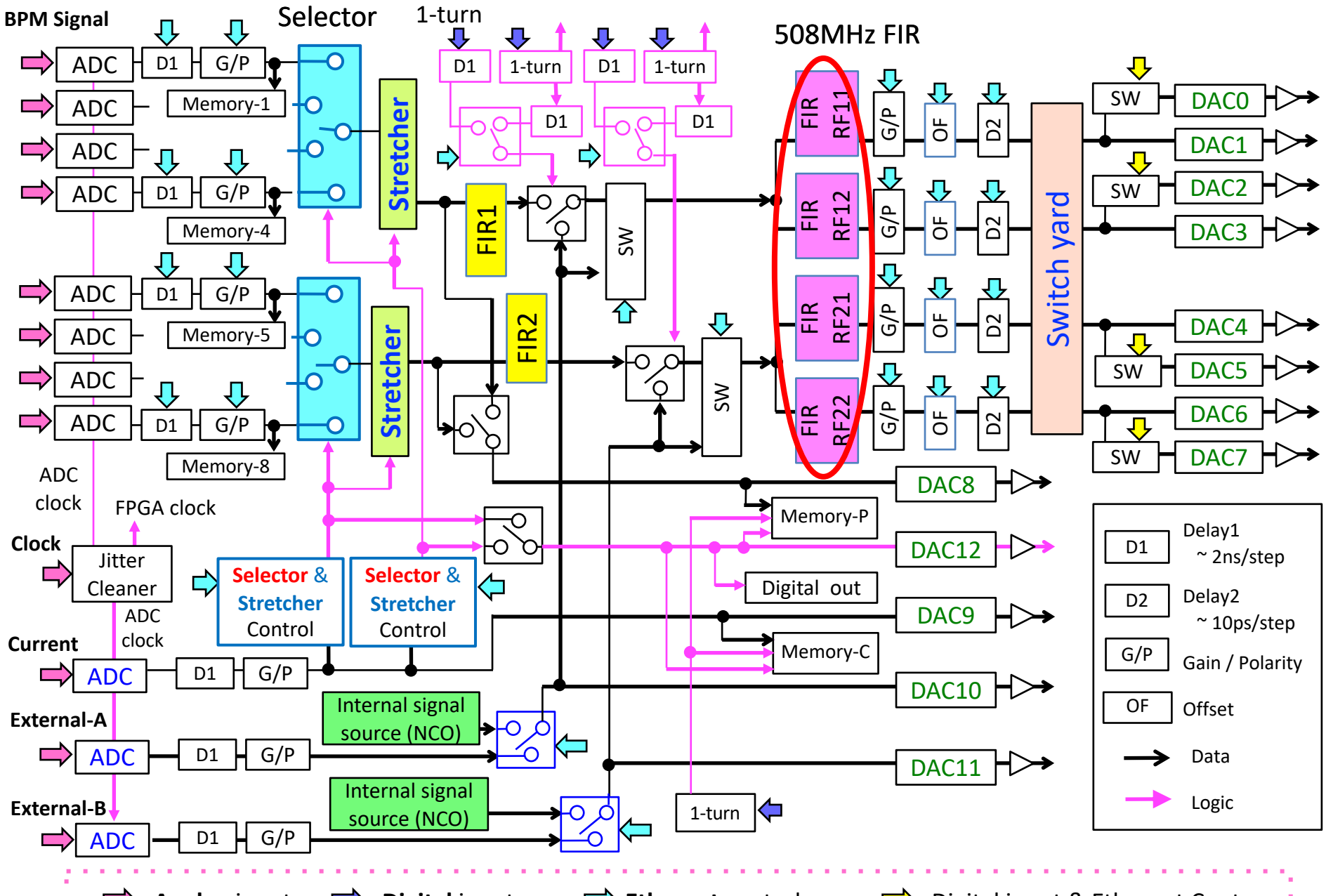


Isolated bunch

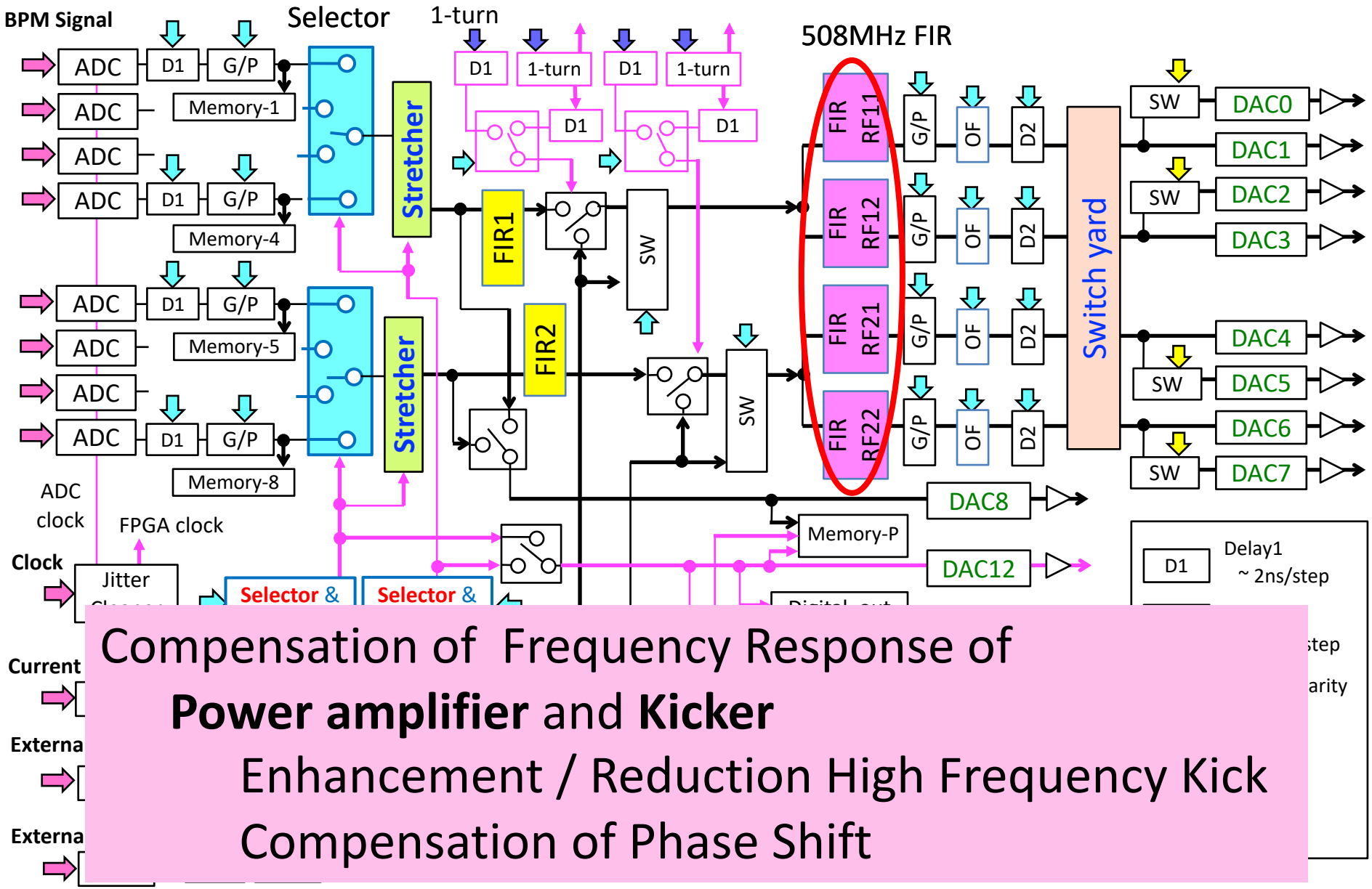
Kicker time constant = 2L/c = 2 x **0.3m** / c = **2 ns**



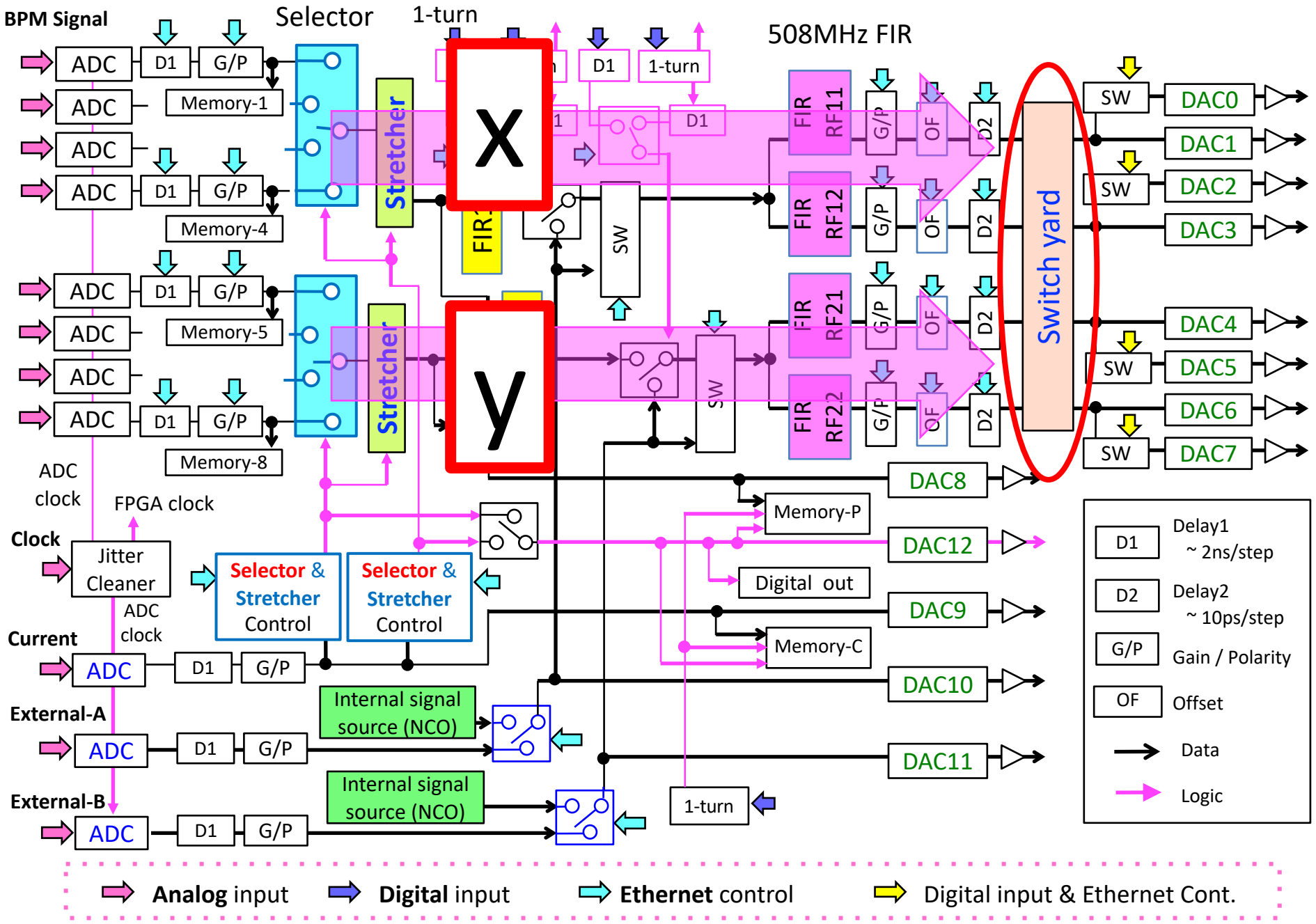
500MHz FIR filter



500MHz FIR filter



Switch yard


BPM Signal
Selector
1-turn
508MHz FIR
ADC
D1
G/P
Memory-1
Memory-4
Memory-5
Memory-8
Stretcher
X
y
FIR
SW
FIR RF11
FIR RF12
FIR RF21
FIR RF22
OF
D2
Switch yard
SW
DAC0
DAC1
DAC2
DAC3
DAC4
DAC5
DAC6
DAC7
DAC8
DAC12
DAC9
DAC10
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Memory-P
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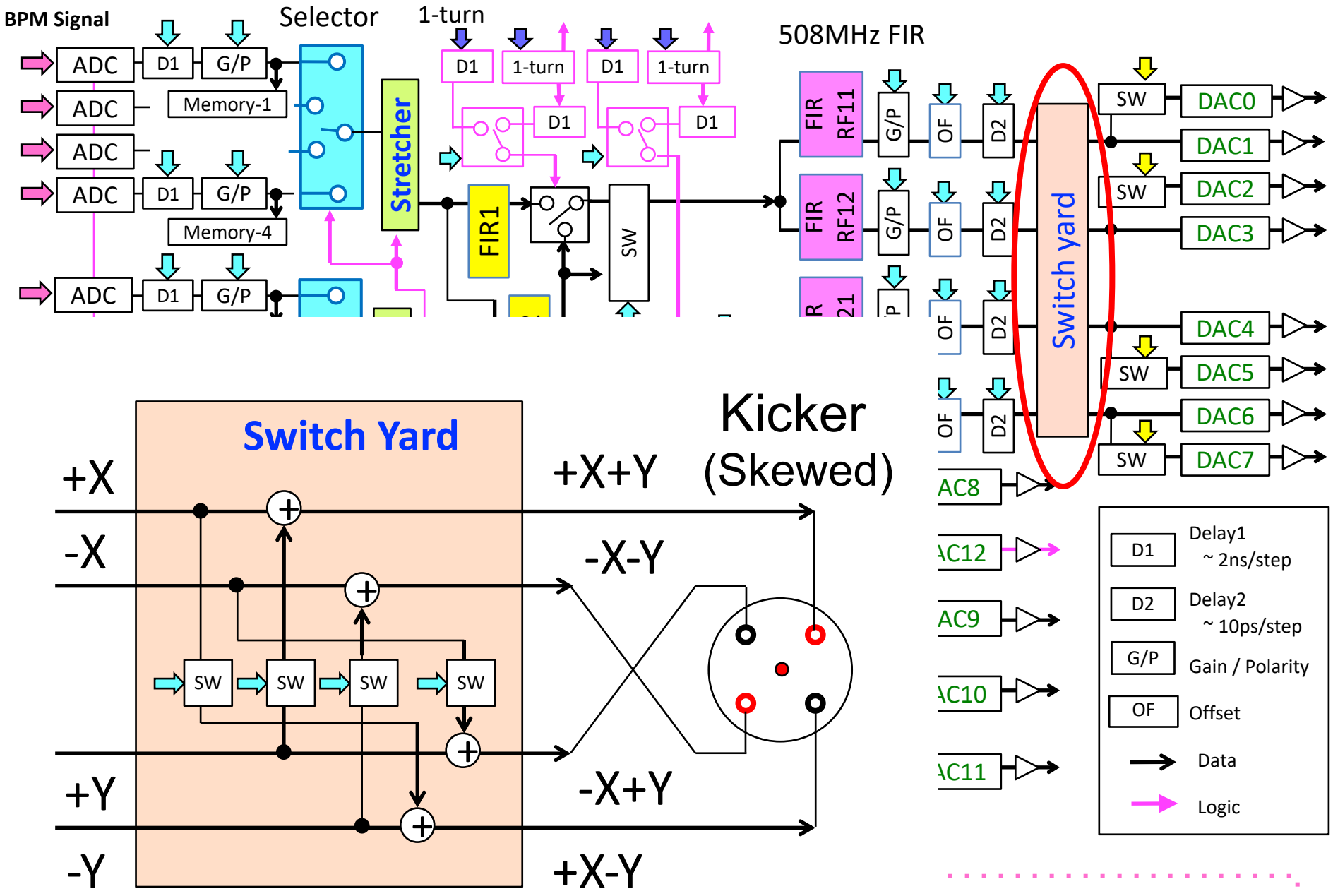
1-turn
ADC clock
FPGA clock
Clock
Jitter Cleaner
Selector & Stretcher Control
Current
External-A
External-B
Internal signal source (NCO)
Delay1 ~ 2ns/step
Delay2 ~ 10ps/step
Gain / Polarity
Offset
Data
Logic
Analog input
Digital input
Ethernet control
Digital input & Ethernet Cont.

Switch yard


BPM Signal
ADC
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Memory-1
Memory-4
Selector
Stretcher
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FIR1
SW
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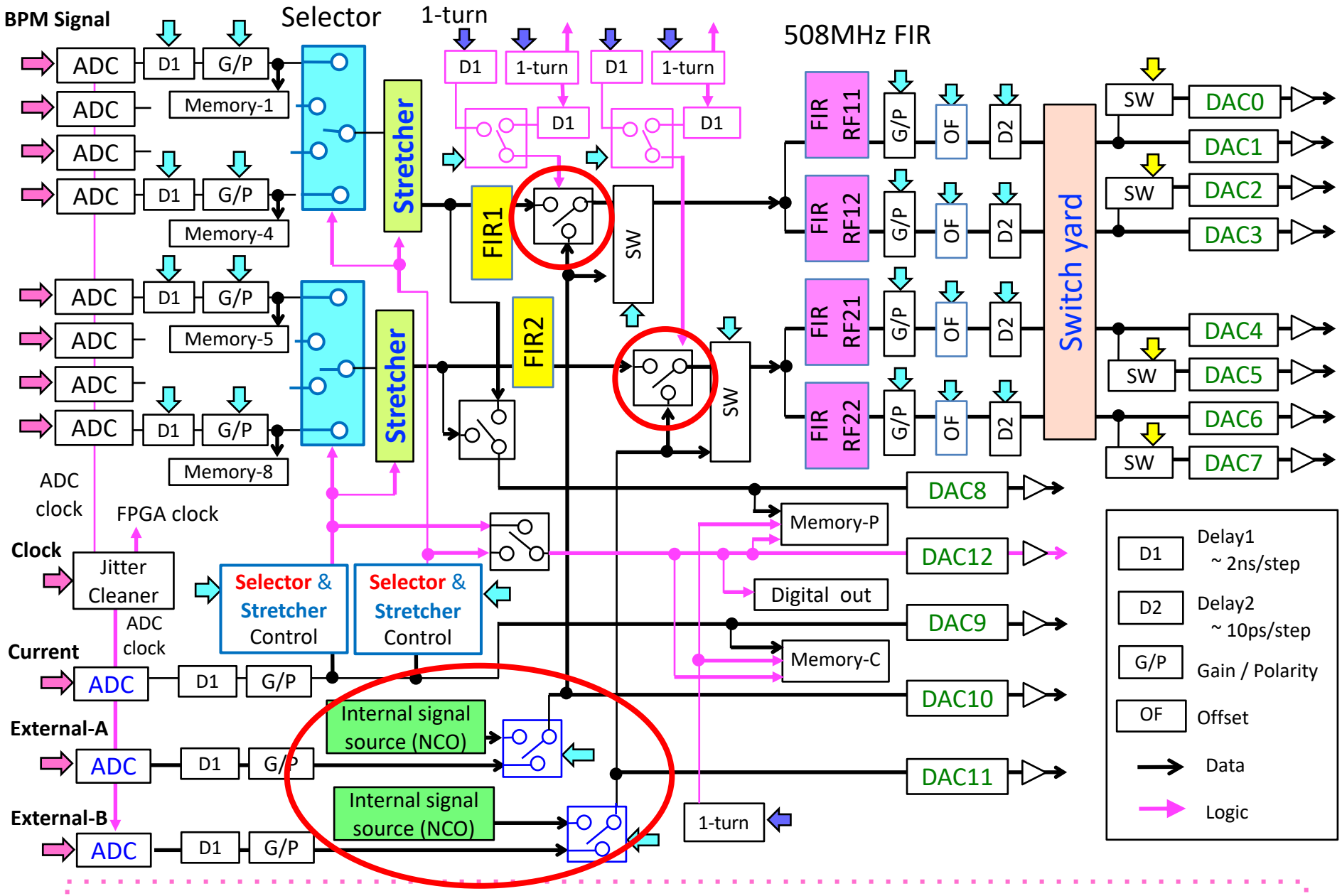
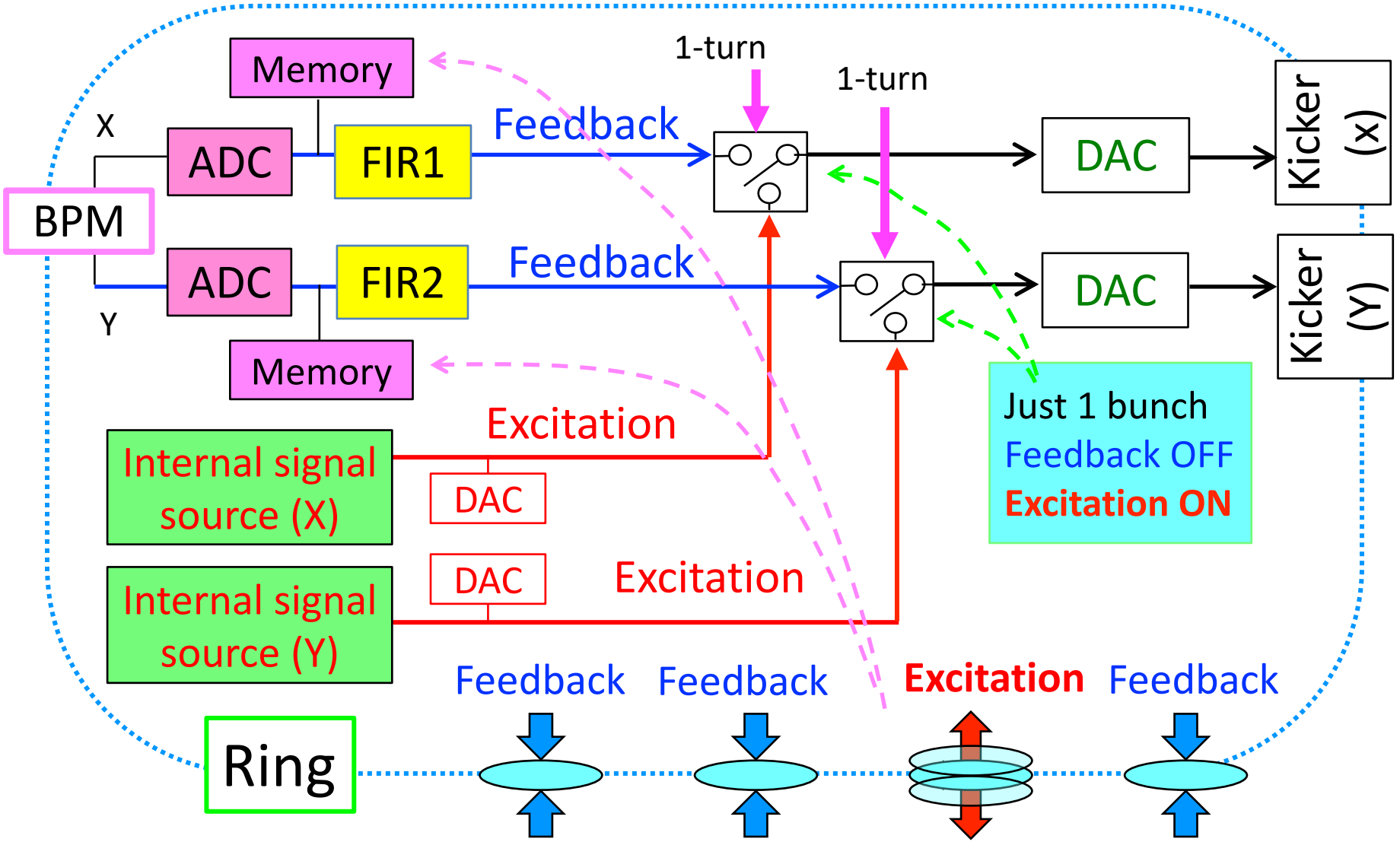
FIR RF11
FIR RF12
OF
D2
Switch yard
DAC0
DAC1
DAC2
DAC3
DAC4
DAC5
DAC6
DAC7
Switch Yard
+X
-X
+Y
-Y
+X+Y
-X-Y
-X+Y
+X-Y
Kicker
(Skewed)
Delay1
~ 2ns/step
Delay2
~ 10ps/step
Gain / Polarity
Offset
Data
Logic
Digital input & Ethernet Cont.

Tune Measurement with One Bunch Excitation



Tune Measurement with One Bunch Excitation

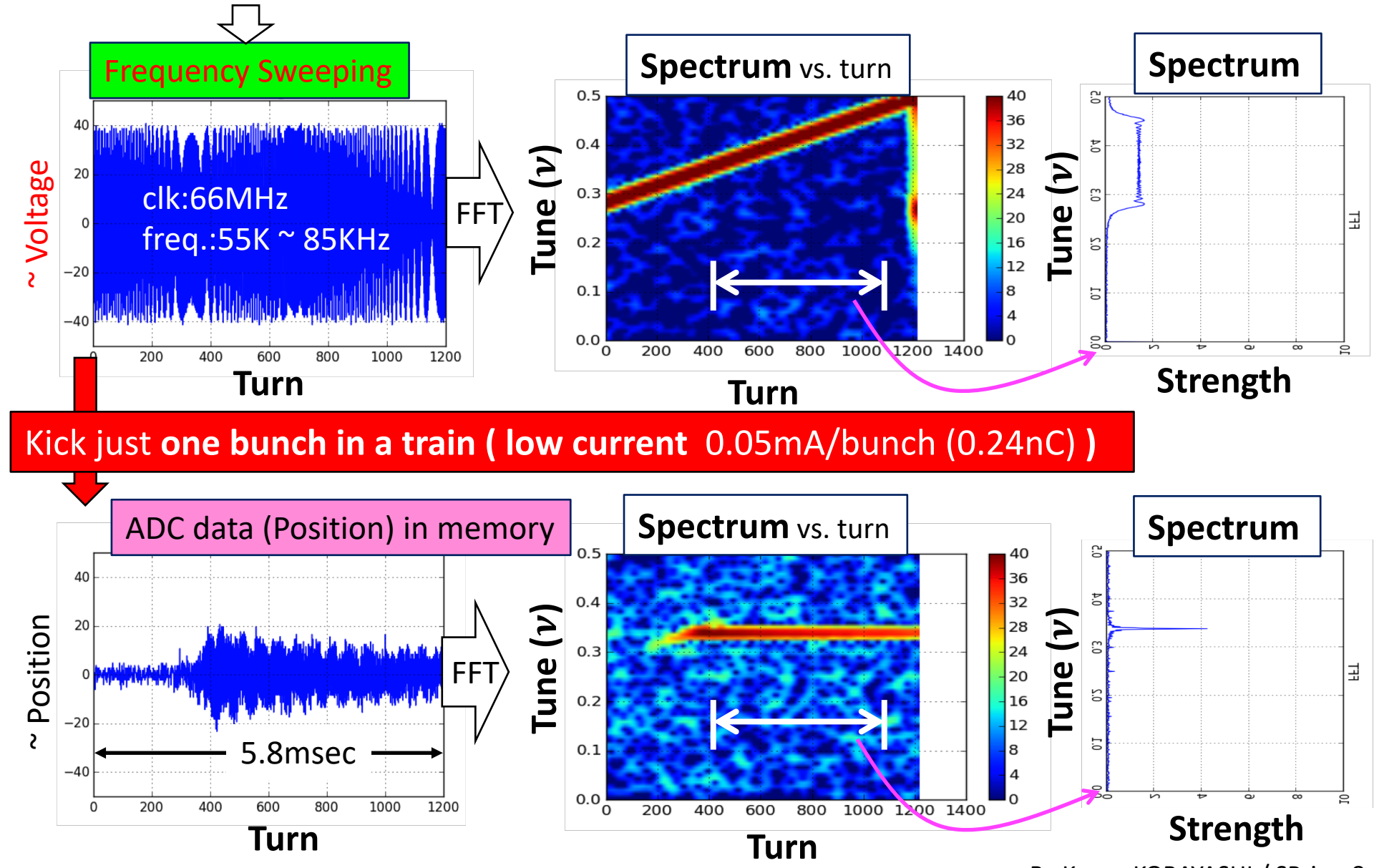
Just one bunch is excited, others are feedbacked => small effect to users



Based on the tune measurement system for the previous version of the processor developed by **R. Sreedharan and R. Nagaoka (SOLEIL)**

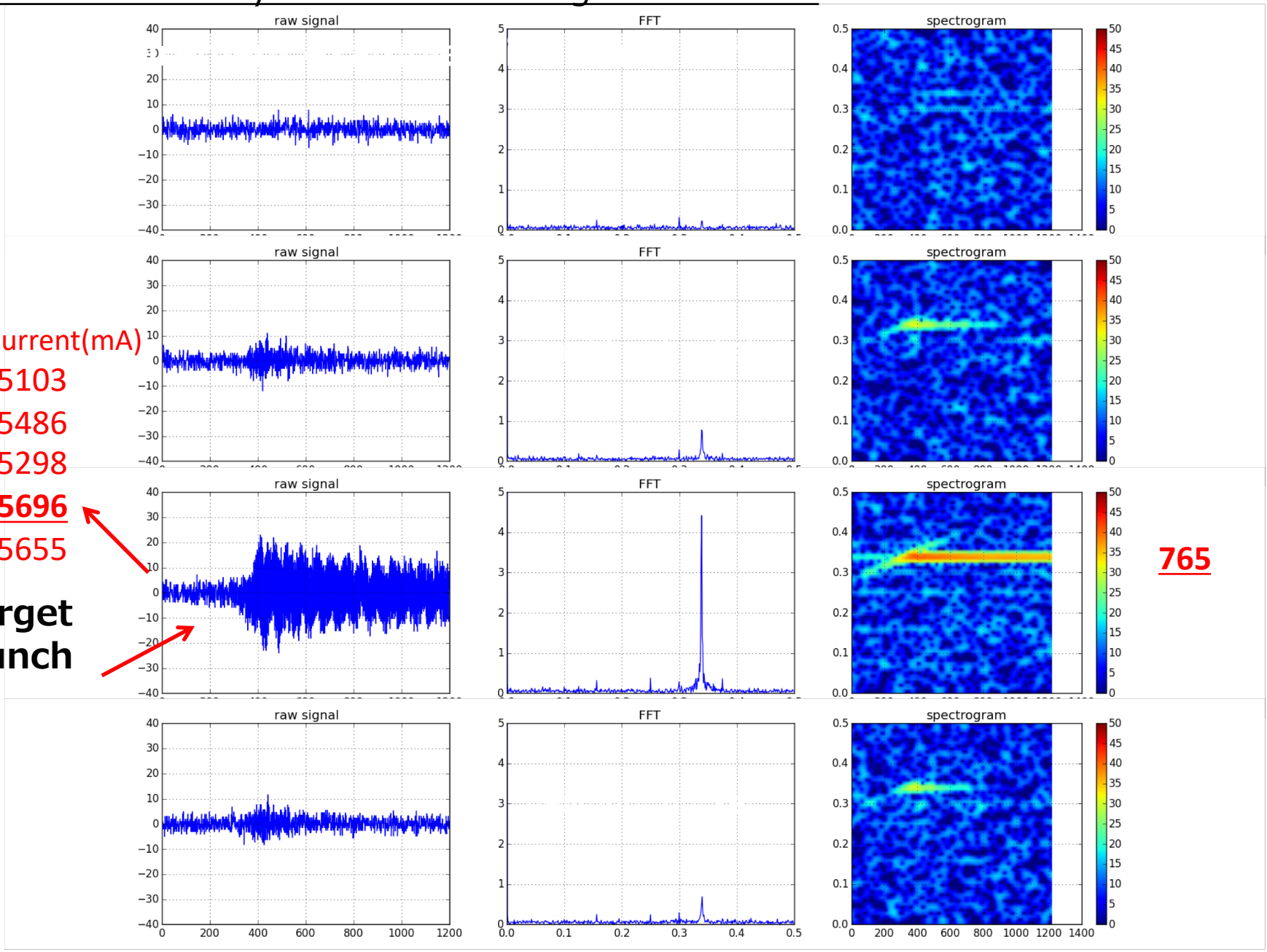
Tune Measurement with One Bunch Excitation

Excitation Signal by Internal Signal Source (NCO)



By Kazuo KOBAYASHI / SPring-8

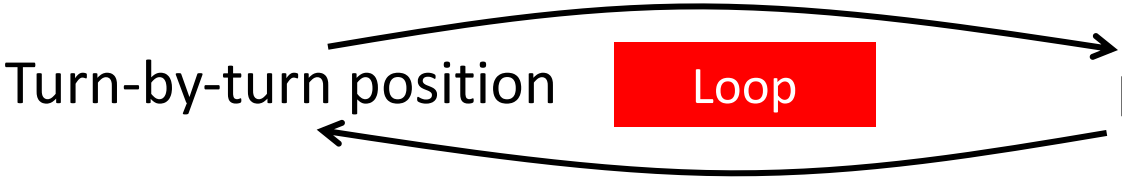
❑ Tune observation system with New Signal Processor



By Kazuo KOBAYASHI / SPring-8

Feedback with Multiple BPMs for Stability at High Gain

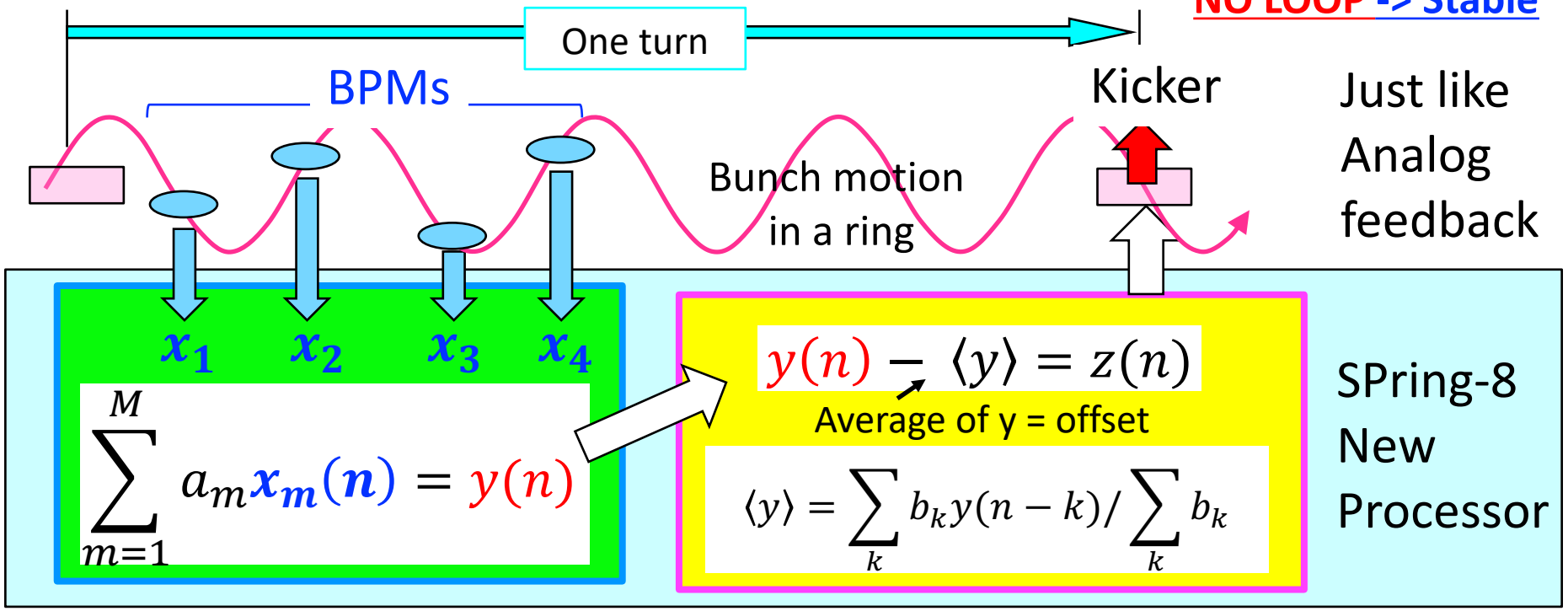
Kick <= **Turn-by-turn Position** with a single BPM



Loop ->
Unstable At High Gain

Kick <= **Multiple Positions (BPMs) in a SINGLE TURN**

NO LOOP -> Stable

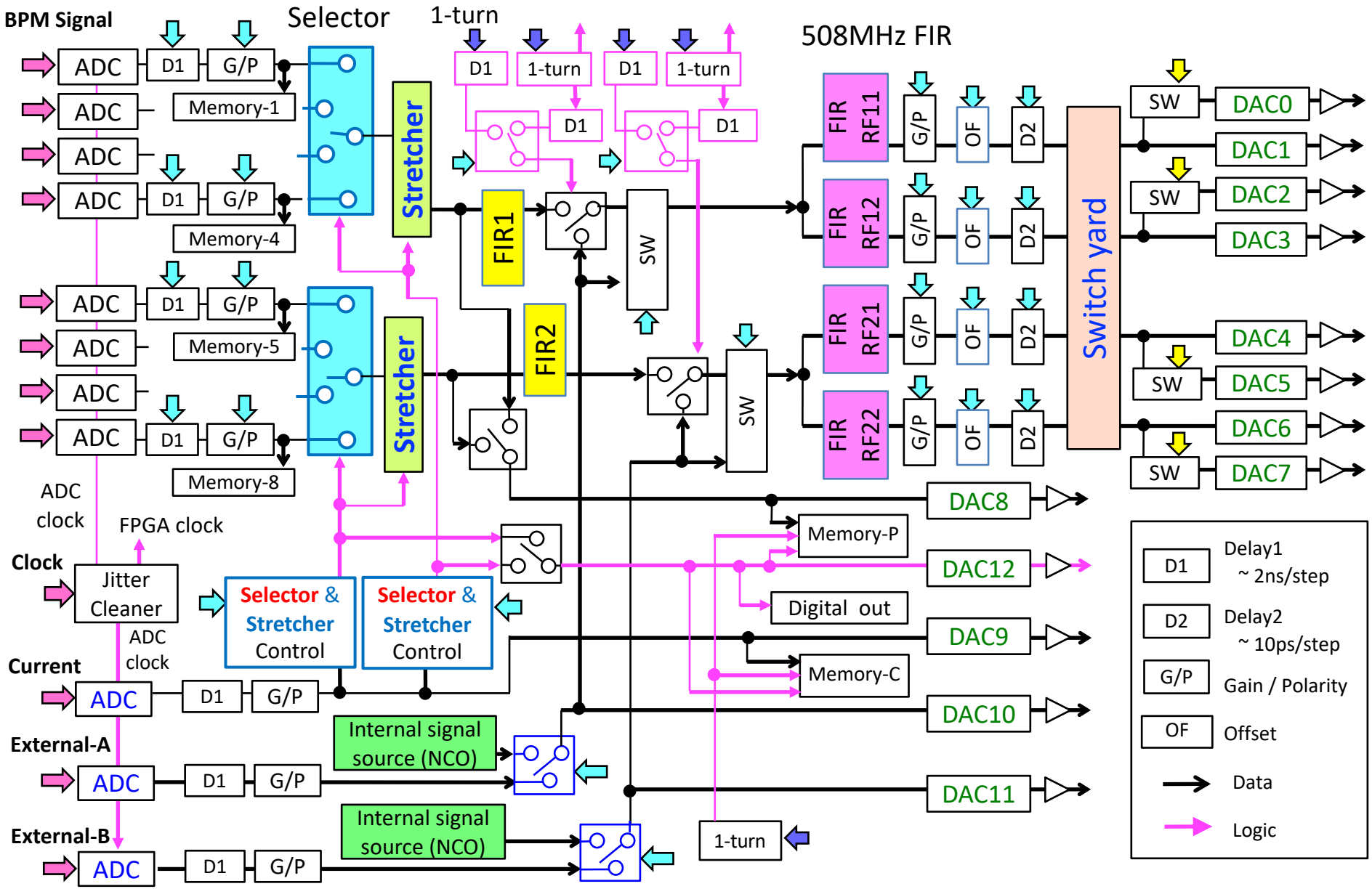


1 or 2 BPMs : enough if those have good phase relations each other and kicker

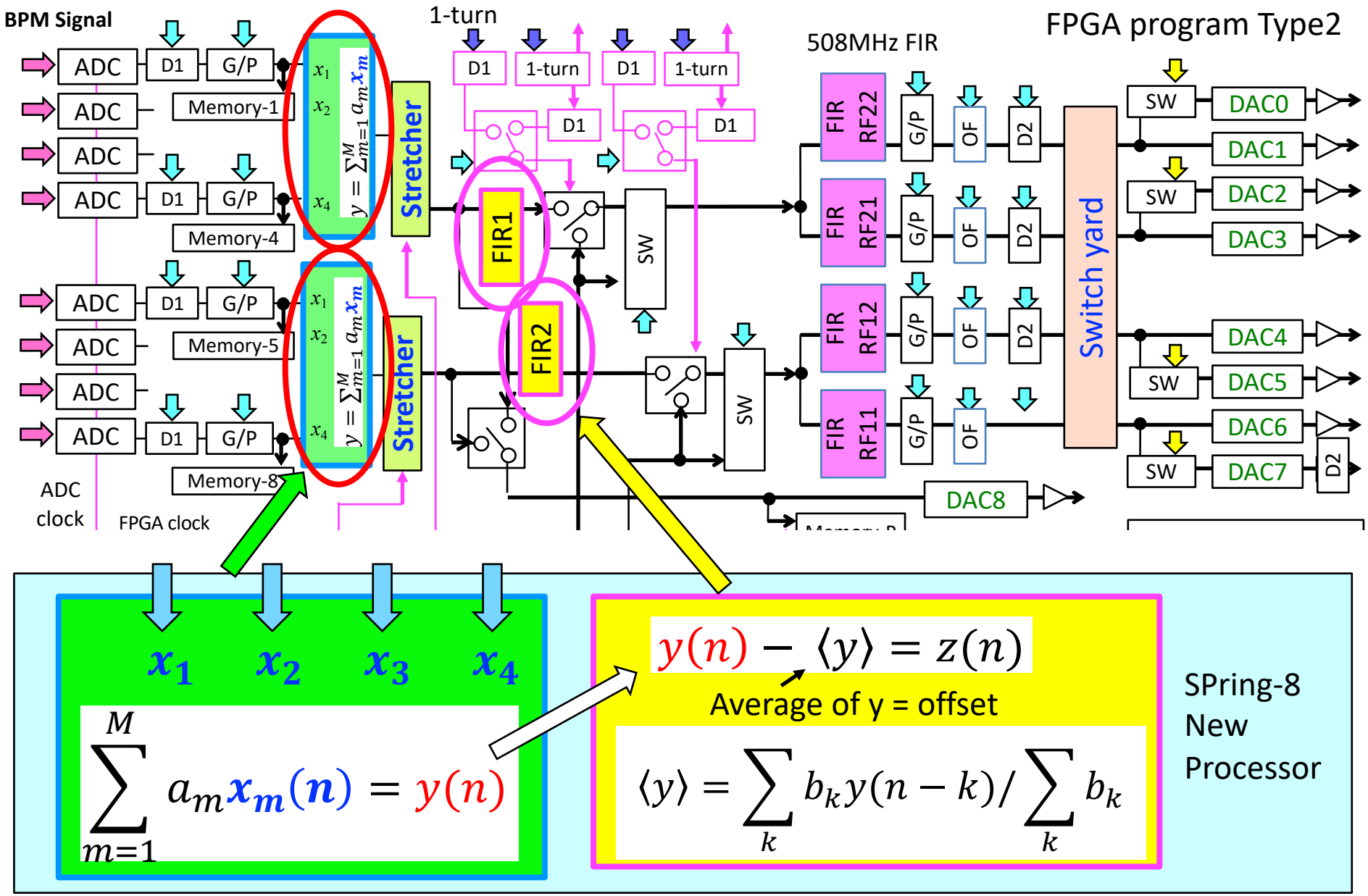
T. Nakamura, Proc. of *14th Ann. Meet. Part. Accel. Soc. Japan,* paper TUP090, Aug. 1-3, 2017

Proc. of IPAC18, . tuzgbd2

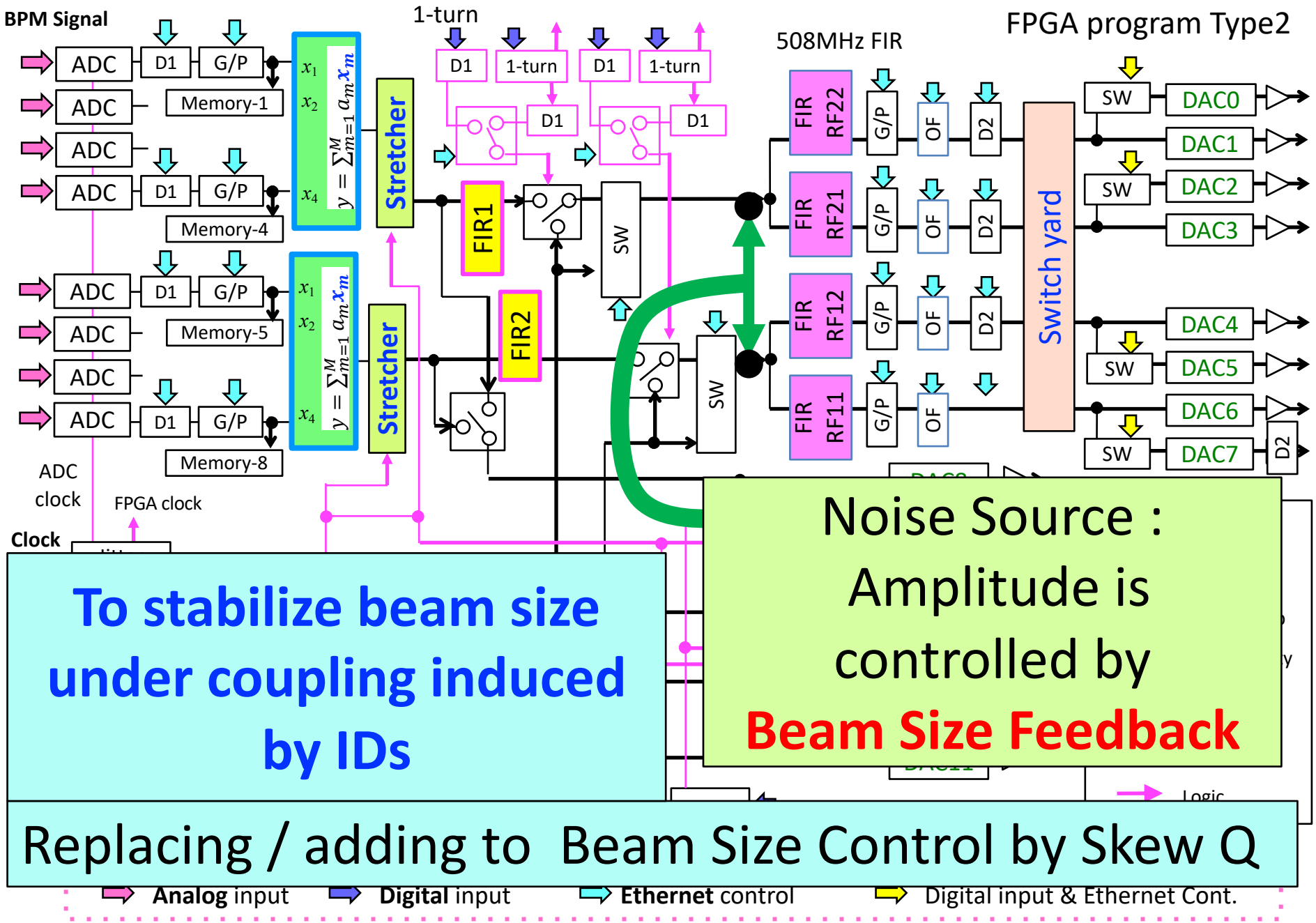
Selector => Filter for Multiple BPMs



Feedback with Multiple BPMs for Stability at High Gain



Beam Size Feedback Control (SOLEIL)



Head-Tail Feedback for Single Bunch Instability

with head-tail monitor and kicker

(just concept and simulation)

T. Nakamura, Proc. of the 15th Ann. Meet. of Part. Acc. Soc. of Japan, 2018
https://www.pasj.jp/web_publish/pasj2018/proceedings/PDF/THP0/THP089.pdf

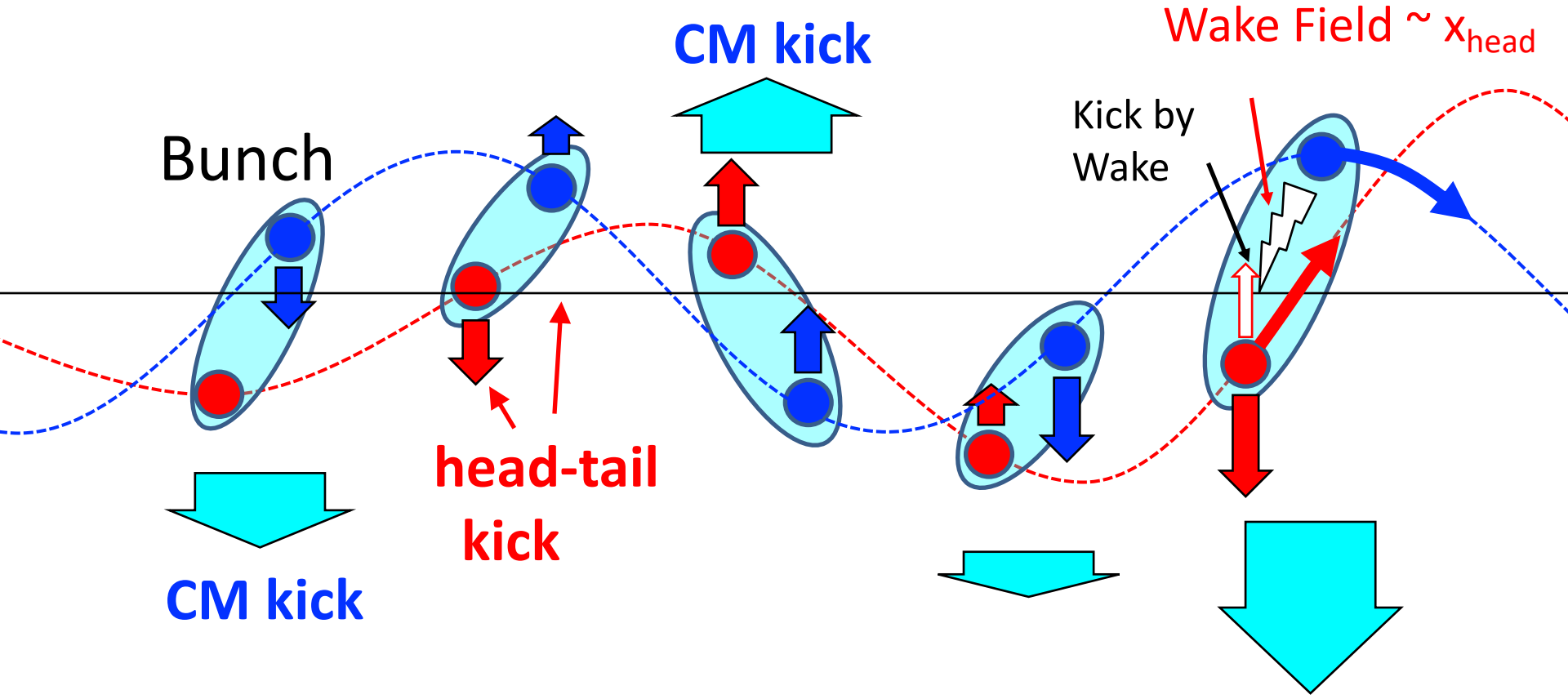
Single-bunch Instability

Bunch Head produces Wake => Kicks Bunch Tail

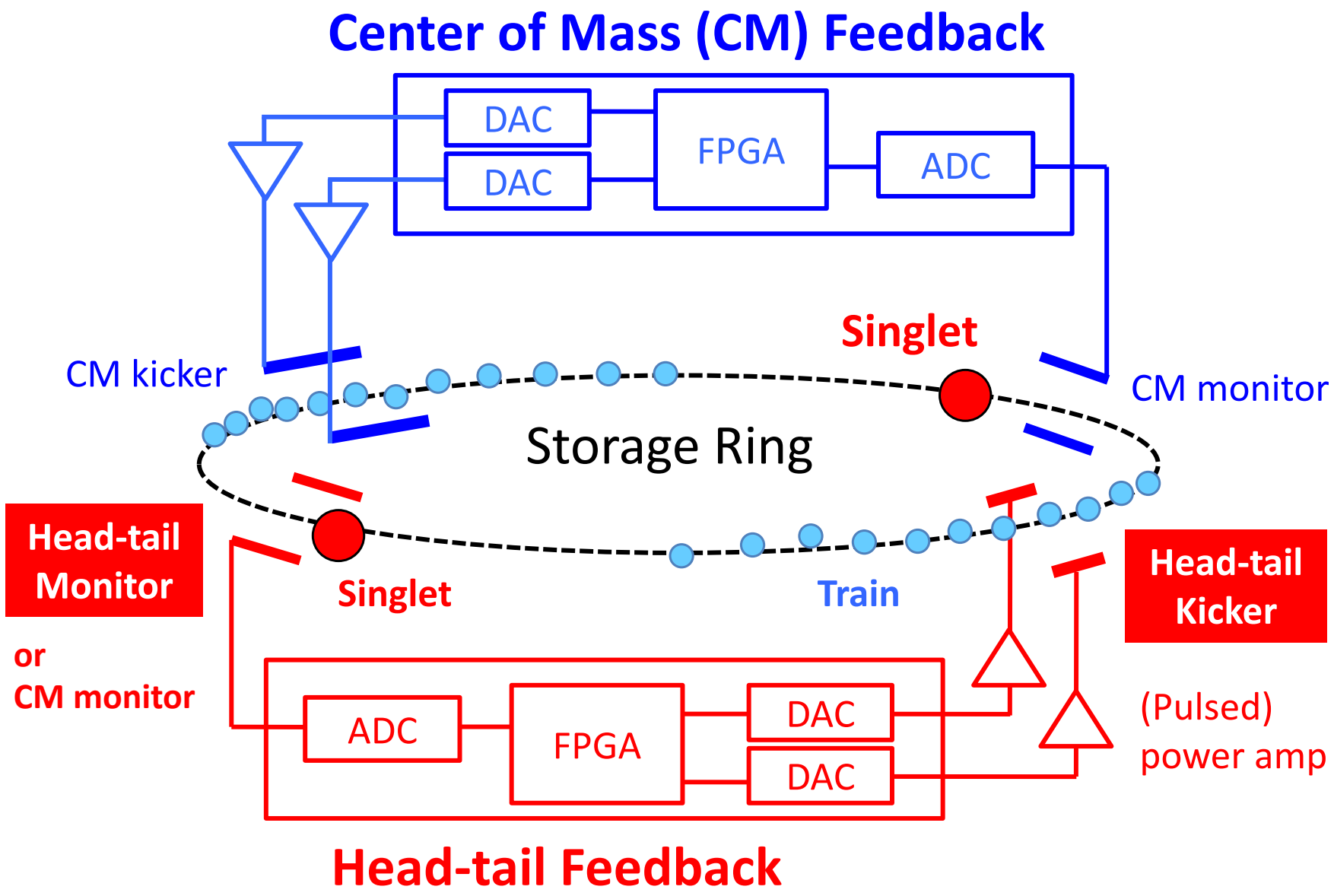
Head and Tail : Phase Difference

Two modes : head + tail Center of Mass (CM) feedback

: head - tail Head-tail feedback



Feedback For Single-bunch Instability



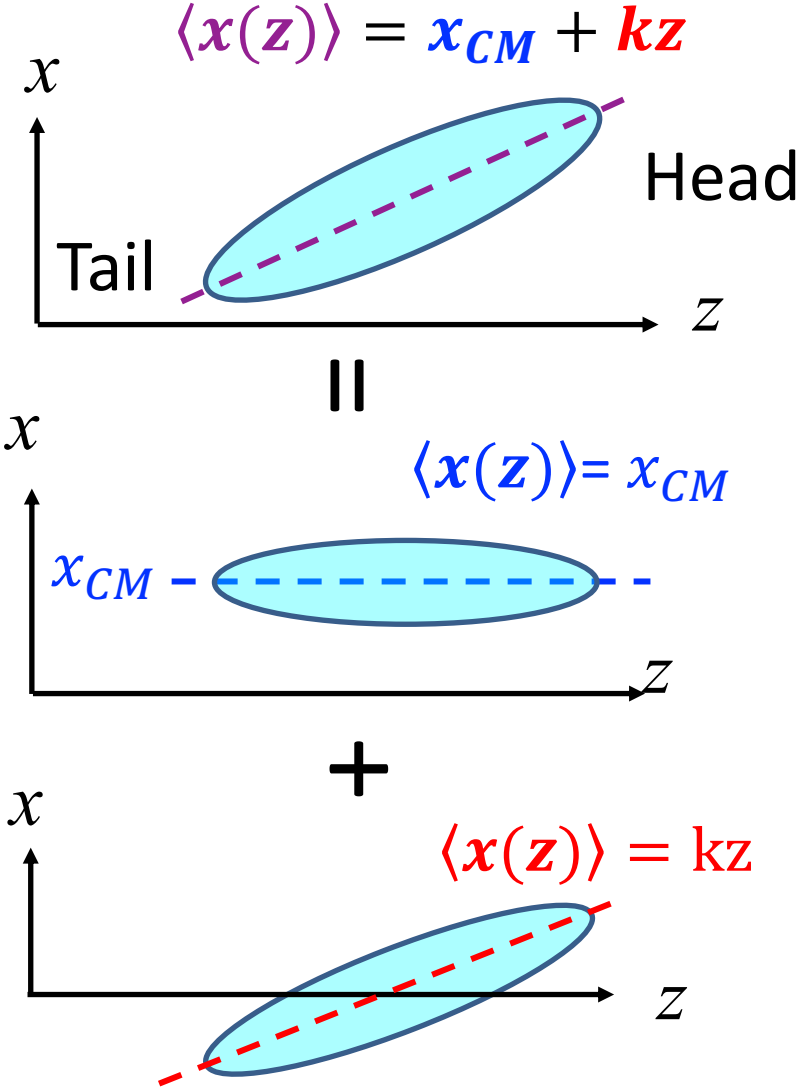
Head-tail monitor

Detection of Angle of bunch distribution

Transverse Position vs Longitudinal Position

$\langle x(z)\rangle$ =

CM motion + **Head-tail motion**



CM motion (position) :

$$\langle x(z)\rangle = x_{CM}$$

Head-tail motion (angle) :

$$\langle x(z)\rangle = kz$$

$$\langle x(z)\rangle = x_{CM} + kz$$

Head-tail monitor

2D Charge Distribution

Position x Current

Position

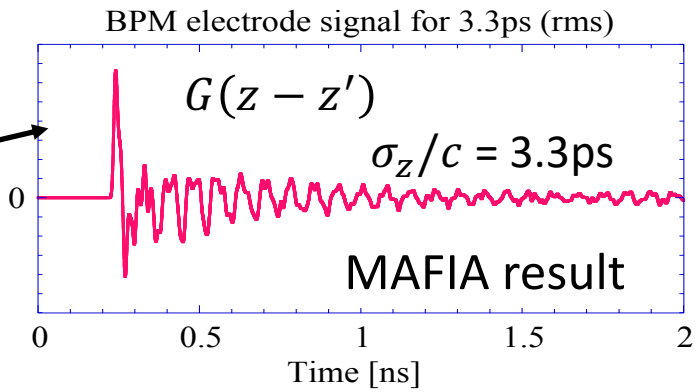
Angle

$$f(x,z) = \langle x(z) \rangle \rho(z) = x_{CM}\,\rho(z) + kz\,\rho(z)$$

BPM signal (A-B)

BPM response for $\delta(z')$

$$S(z=-ct) = \int f(x,z') G(z-z') dz'$$



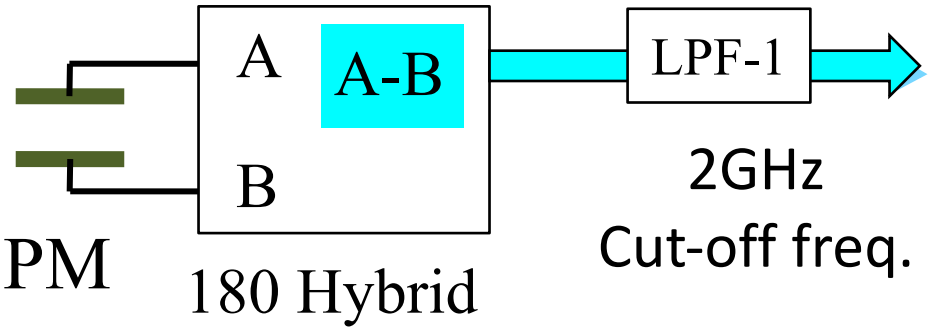
$$= x_{CM} \int \rho(z') G(z-z') dz' + k \int z' \rho(z') G(z-z') dz'$$

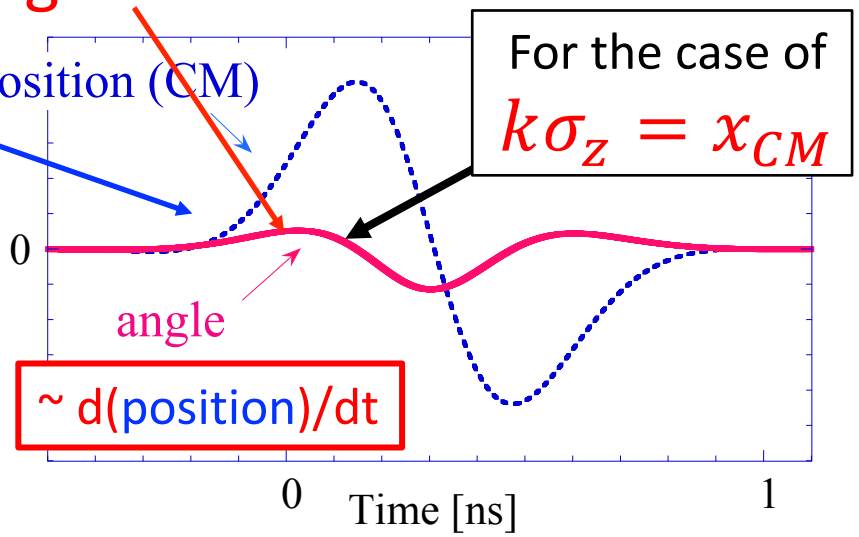
Position

Angle

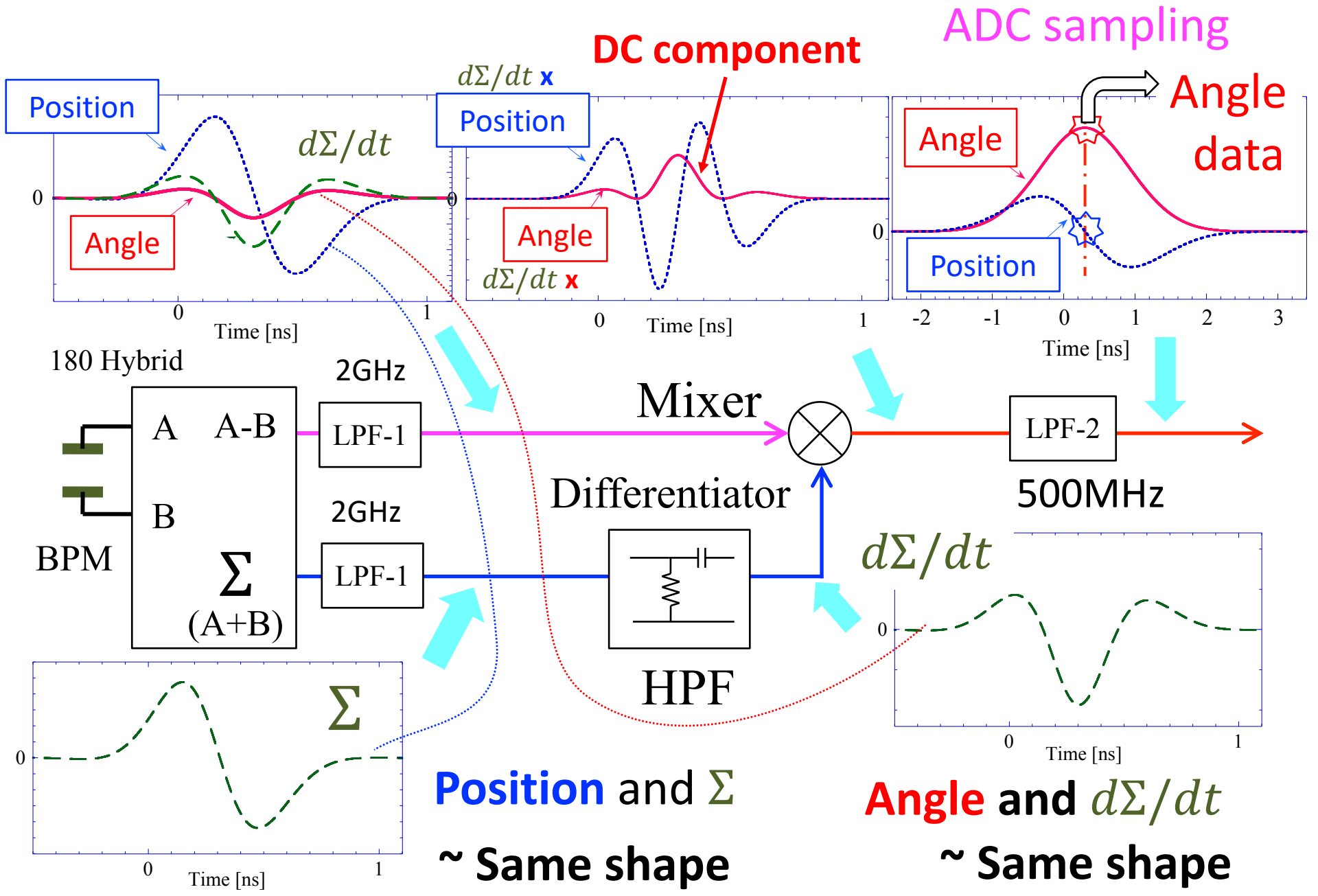
$\rho(z)$: Gaussian

σ_z/c = 24ps





Head-tail Motion Monitor



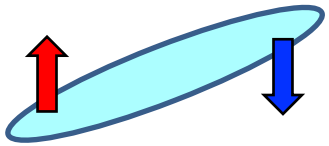
Head-Tail Kicker : Angle kick => **high dV_{kick}/dt**

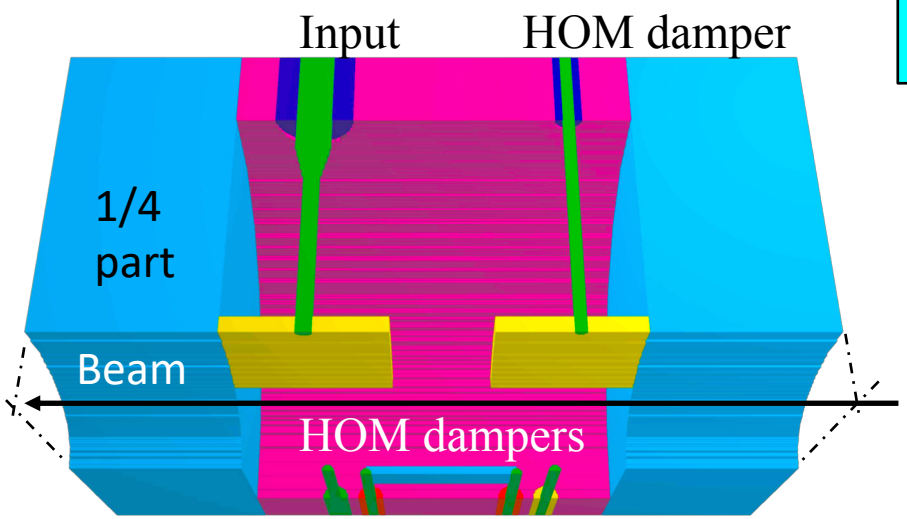
Resonant Kicker

Based on SPring-8 longitudinal kicker*

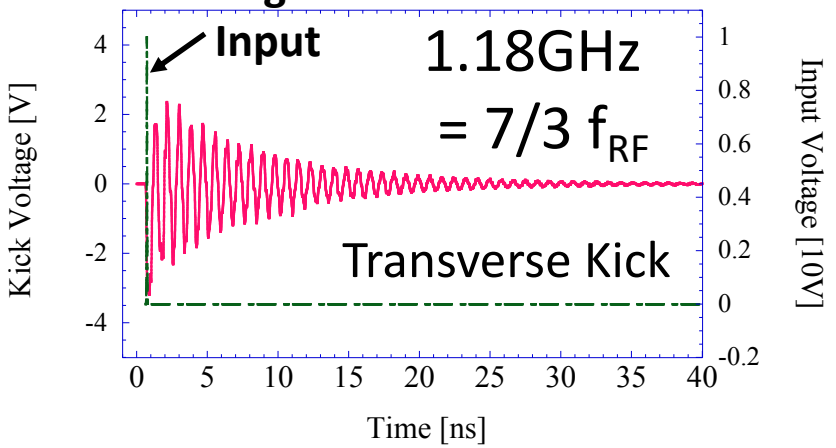
Different kick for head ant tail

High dV_K/dt



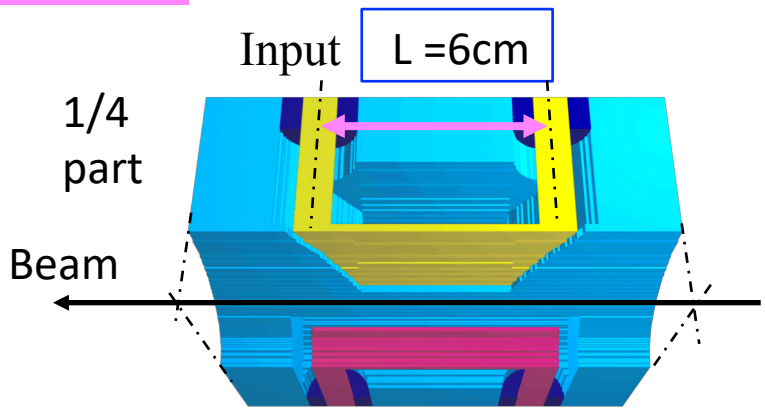


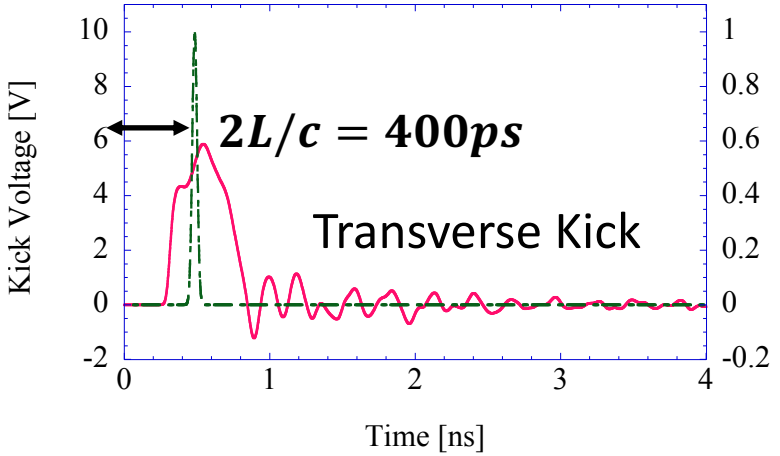
Single Pulse



Stripline

< For comparison >





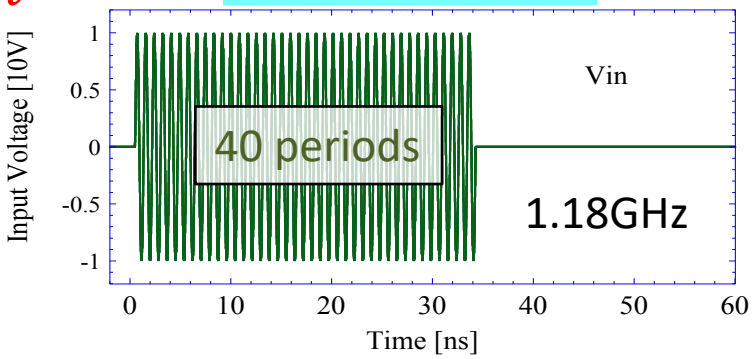
T. Nakamura, Proc. of The Physical Society of Japan, 2015 https://doi.org/10.11316/jpsgaiyo.70.1.0_547

* T. Nakamura, Proc. of IPAC11, MOPO007, M. Masaki, et al., Proc of IBIC13, TUPC18

Enhancement of Kick Voltage by Resonance

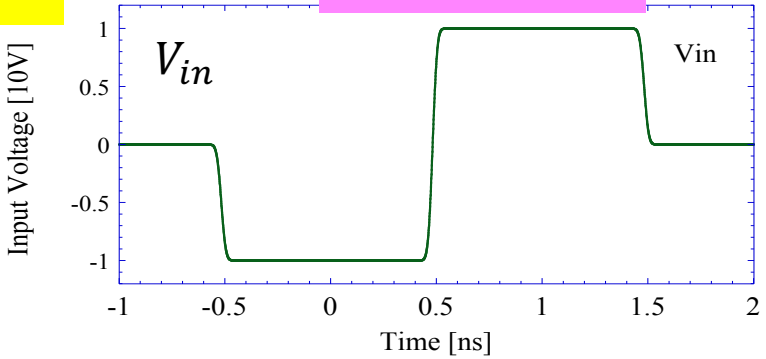
V_{in}

Resonant Kicker



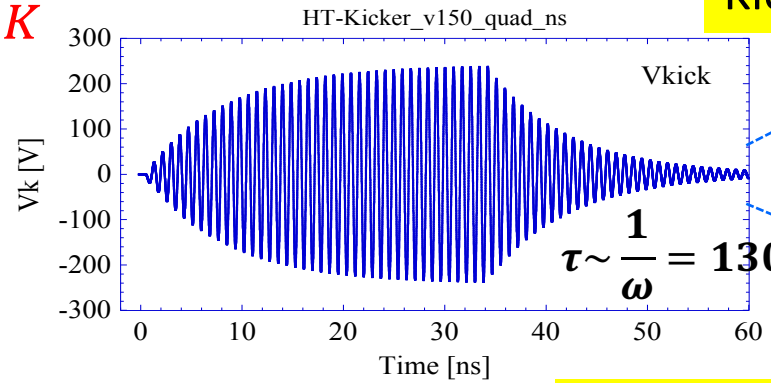
Input

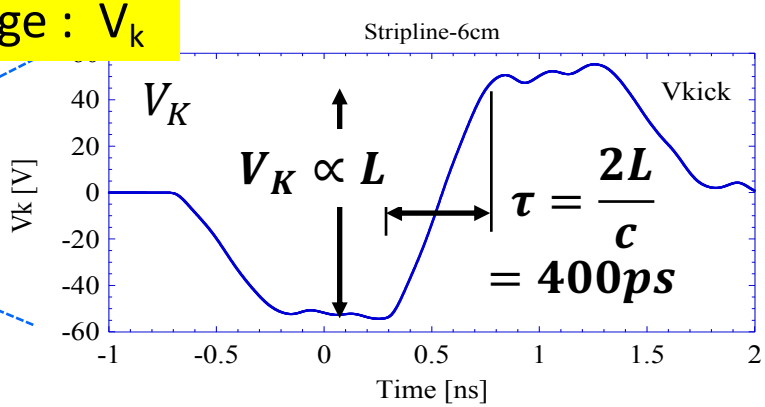
6cm Stripline



V_K

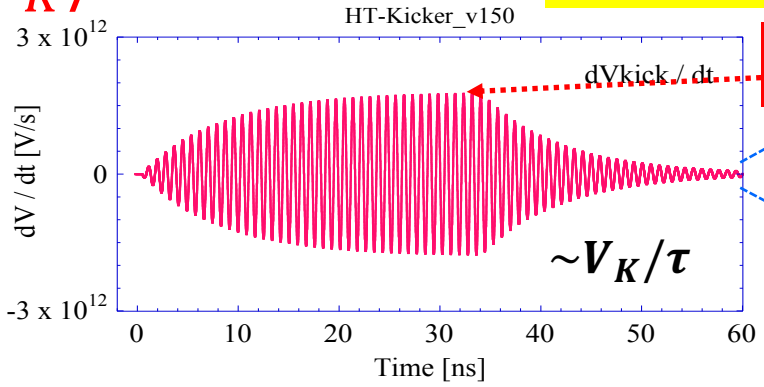
Kick Voltage : V_k



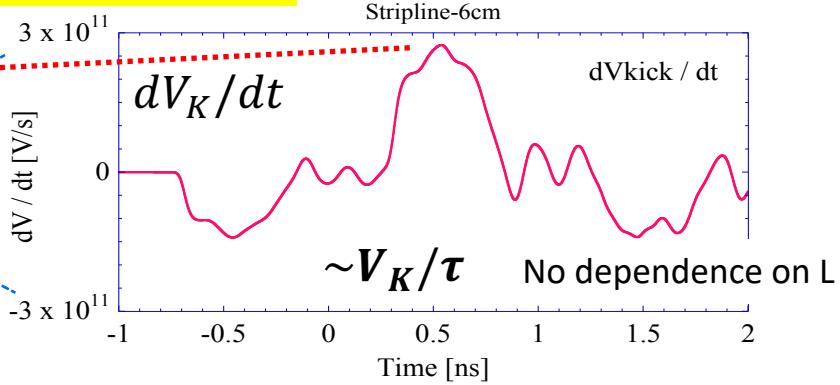


dV_K/dt

Time Gradient of Kick : dV_k / dt



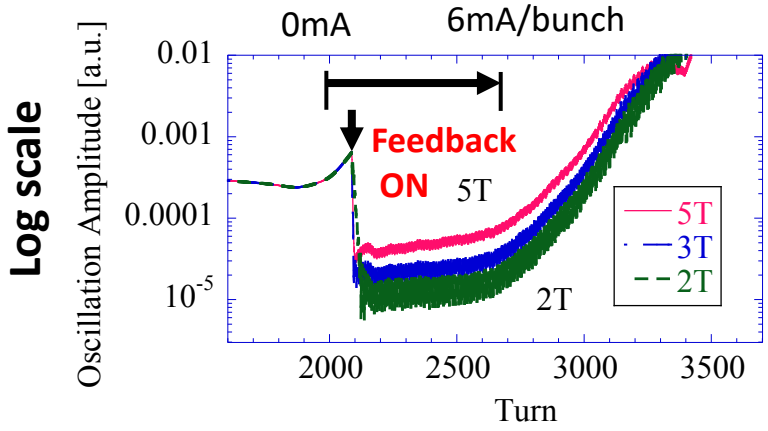
X 6



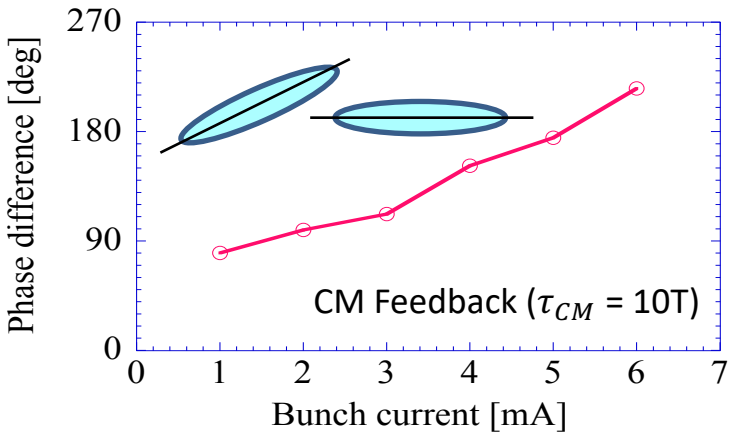
Simulation Results for Head-Tail Feedback

CM feedback

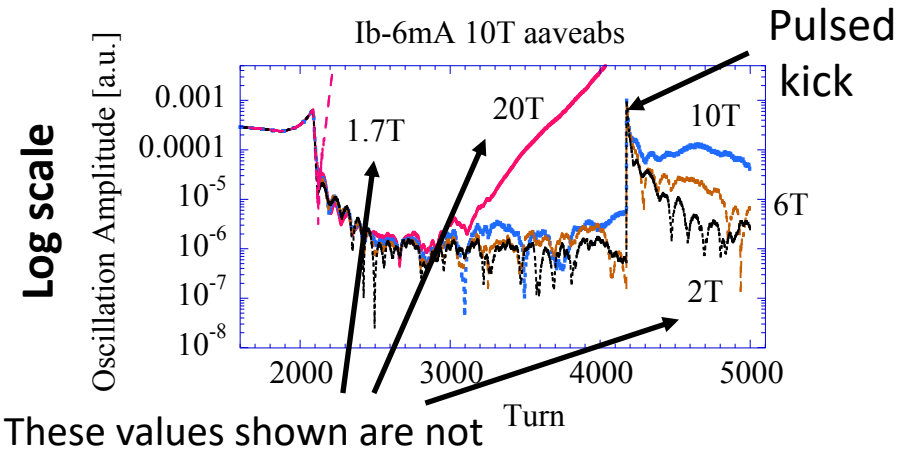
Feedback
Stability limit ~ 2T (T=turns)



Phase between **CM** and **Angle** Oscillations

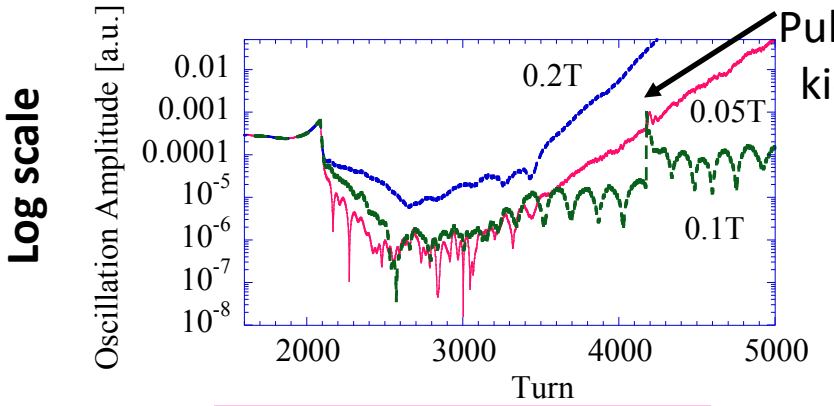


(Angle -> Angle Kick) + CM Feedback (τ_{CM} = 10T)



These values shown are not expected damping time (just gain parameters)

(CM position -> Angle Kick) + CM Feedback (τ_{FB} = 10T)



FIR phase is not optimized

Code : T. Nakamura, Workshop SAD2006, KEK (2006) ; http://acc-physics.kek.jp/sad/SAD2006/Doc/Slide/Nakamura.pdf

Summary

- New SPring-8 Feedback Processor
  in operation at SPring-8 since 2016
  - Multiple ADCs with bunch current controlled selector for hybrid filling
  - Kick pulse Stretcher, Switchyard, ~500MHz FIR
  - In-flight tune measurement
  - Multiple BPM feedback capability for stable high gain operation
  - Testing in SOLEIL, Installation to PLS-II in Feb. 2019
- Head-tail feedback for single-bunch instabilities
  - Bunch angle detection front-end with usual BPM and Angle kicker cavity are proposed
  - Further increase of bunch current is observed in simulation