Nhanced Semiconductor Pre-Irradiation Wafer Testing For HL-LHC Upgrade

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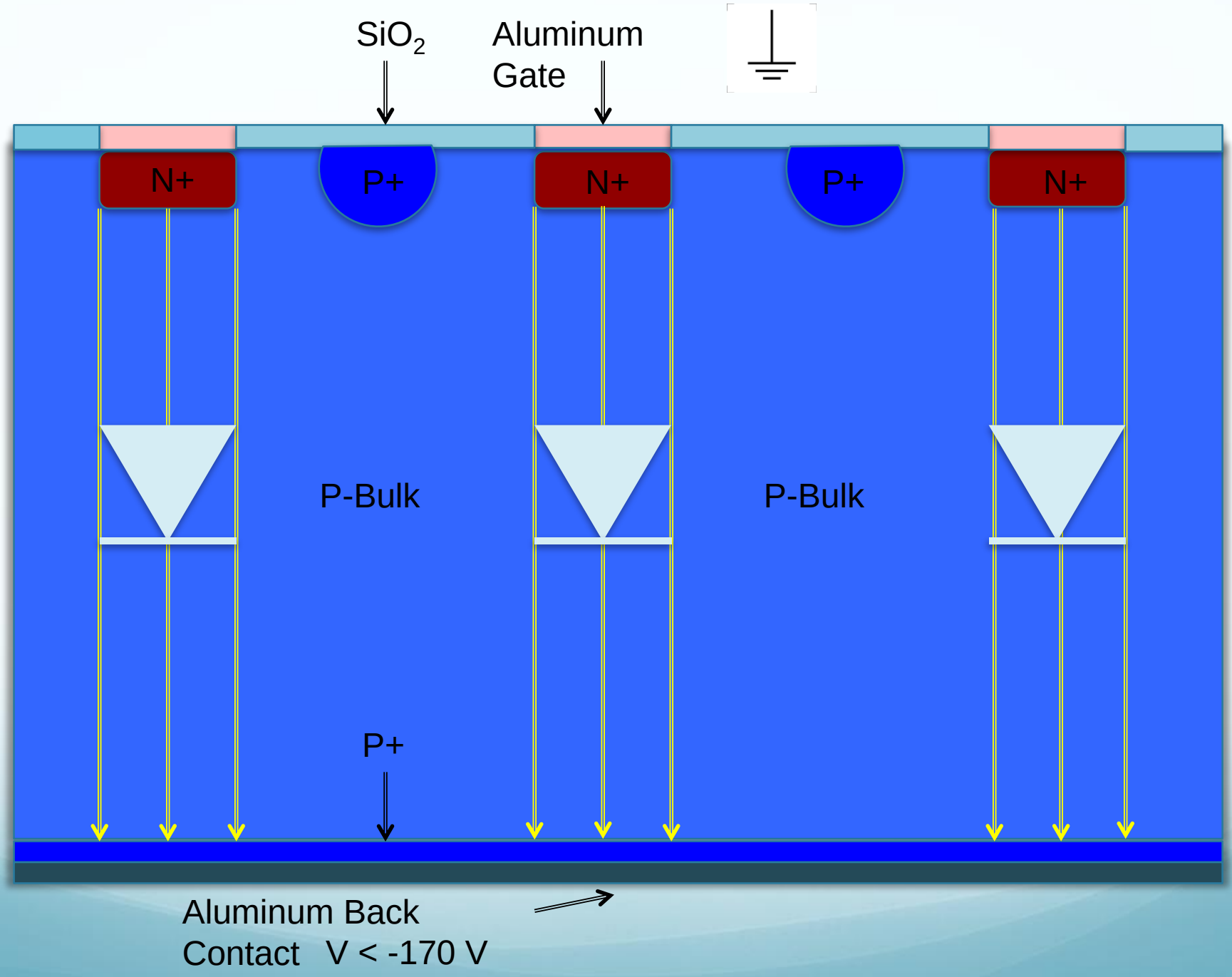
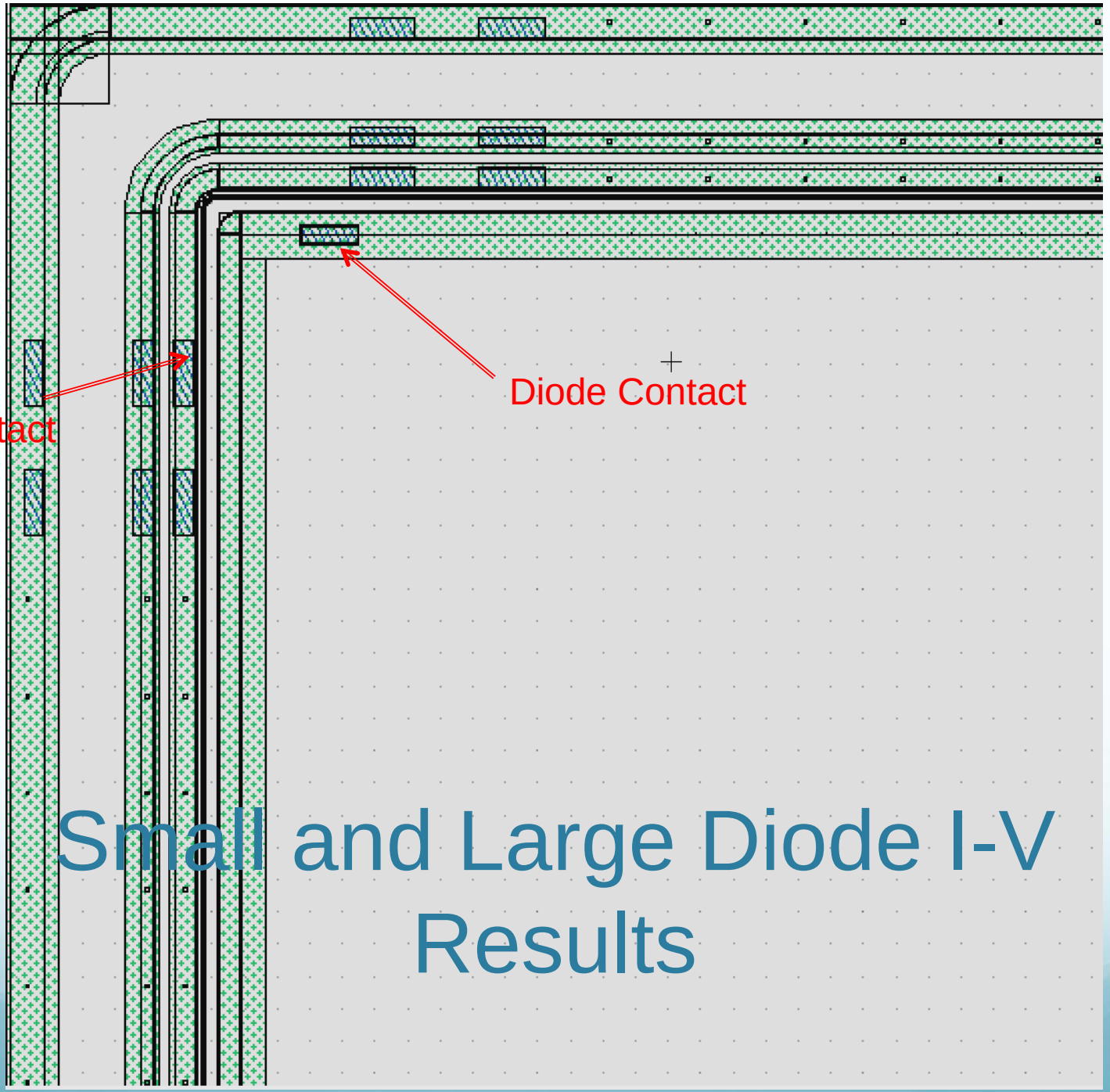
Underlying Principles

- Particles pass through the detector and collide with atoms in the silicon
- This collision ‘knocks out’ electrons from atoms
- These electrons traverse an electric field created by an applied potential (bias potential) inside the silicon wafer
- Finally, the electrons travel to outside circuitry, through amplifiers and shapers, to generate a signal for analysis

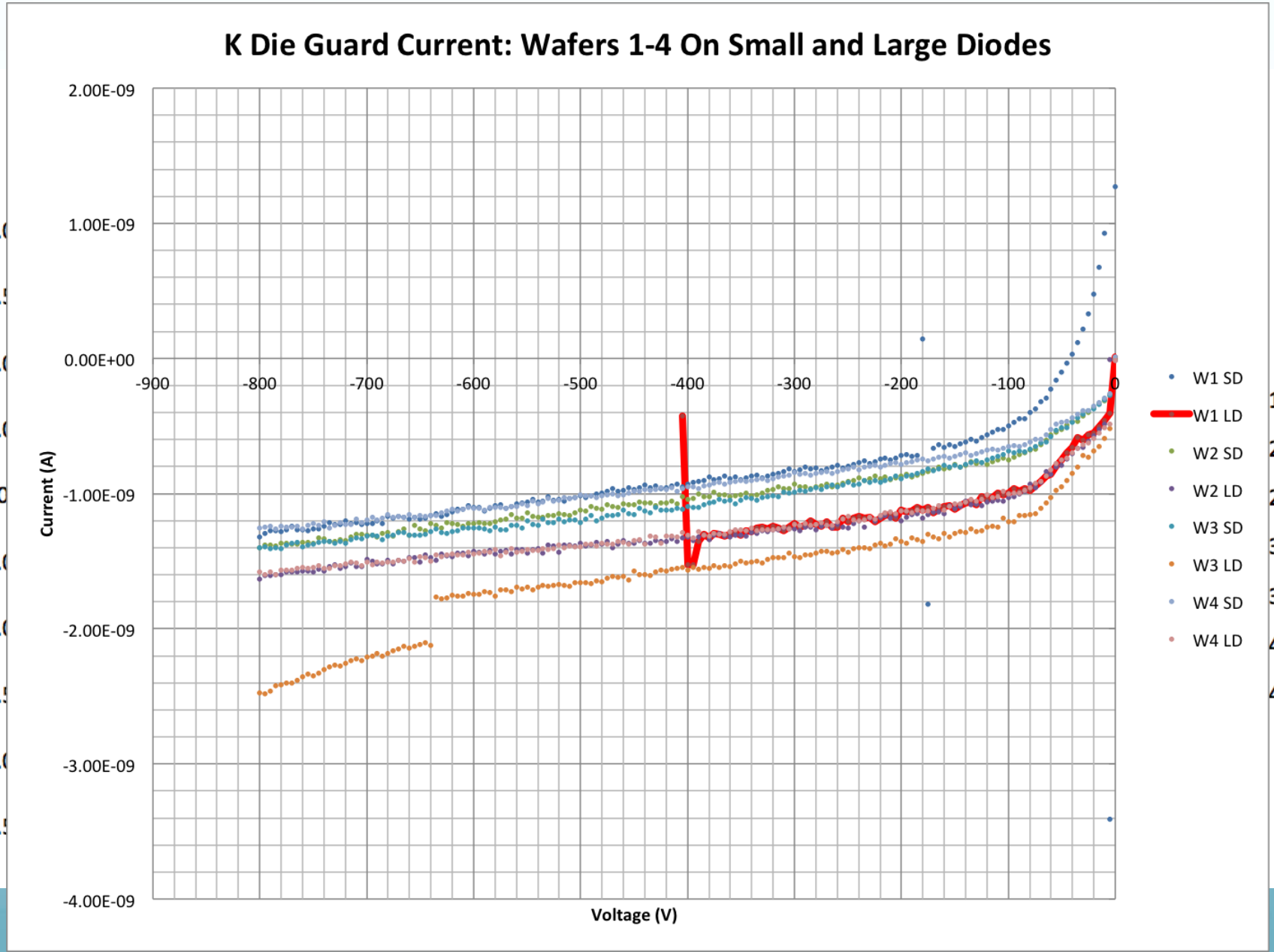

SiO_2
Aluminum
Gate
N+
P+
N+
P+
N+
P-Bulk
P-Bulk
P+
Aluminum Back
Contact V < -170 V

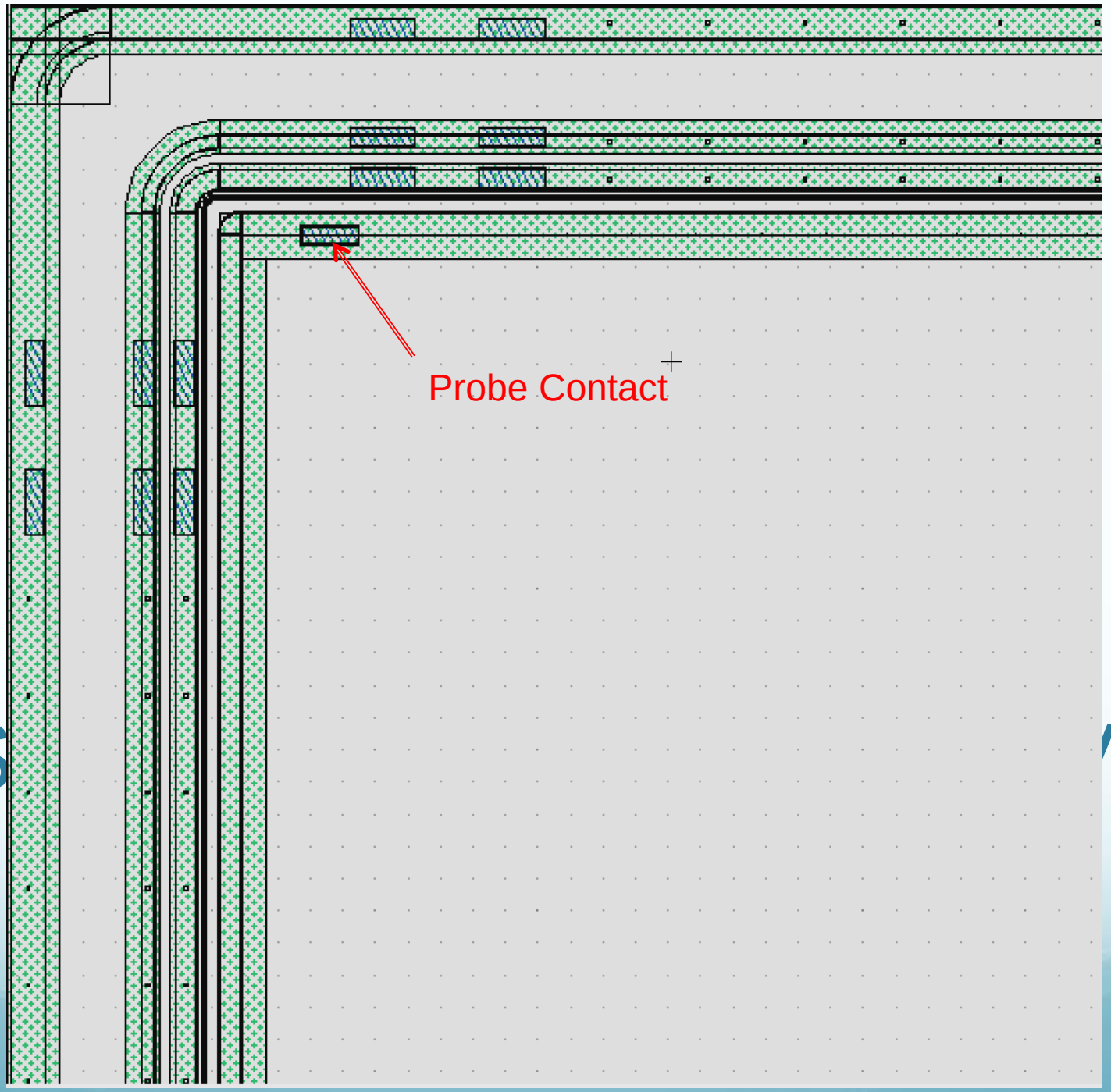
Nhanced Semiconductor Manufacturing Process and Production Goals

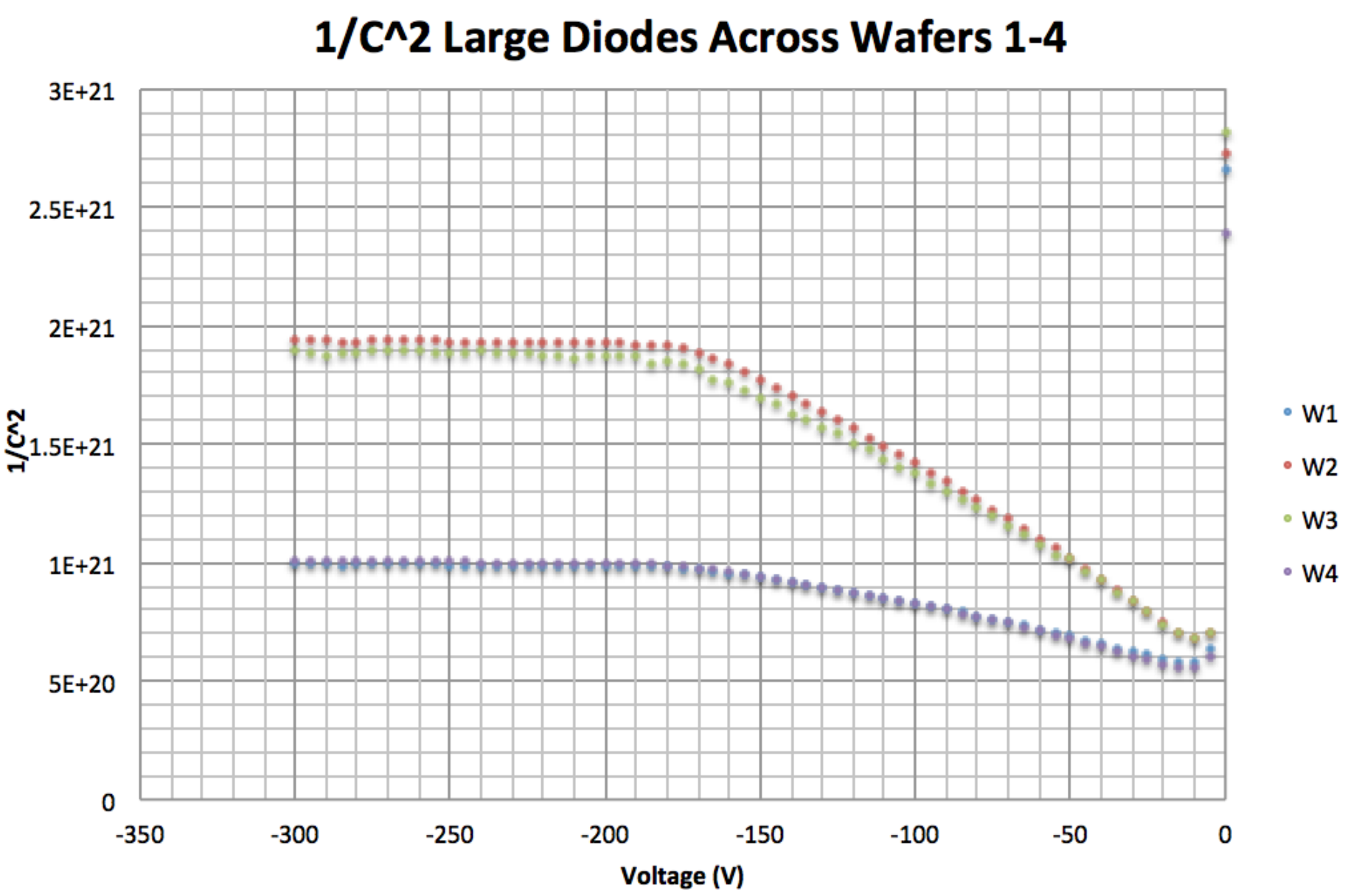
- Silicon On Insulator (SOI) technology enables a thinner wafer without breakage or damage to machinery
- First time the company has produced embedded polysilicon resistors. Goal is to create uniform resistances
- Demonstrate uniformity across wafers and structures.



Small and Large Diode I-V Results

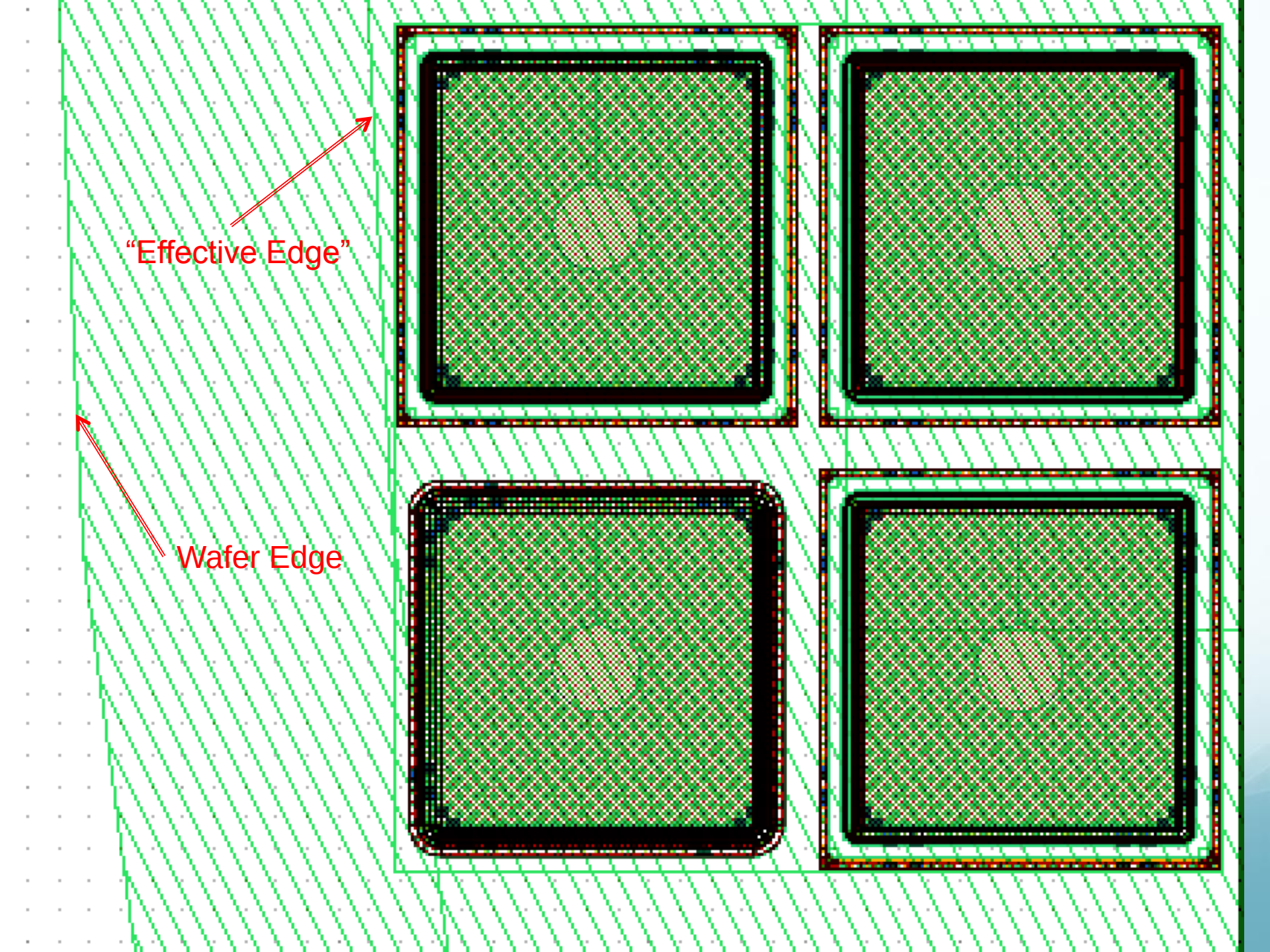

K Die Guard Current: Wafers 1-4 On Small and Large Diodes
Current (A)
2.00E-09
1.00E-09
0.00E+00
-1.00E-09
-2.00E-09
-3.00E-09
-4.00E-09
-900
-800
-700
-600
-500
-400
-300
-200
-100
0
Voltage (V)
W1 SD
W1 LD
W2 SD
W2 LD
W3 SD
W3 LD
W4 SD
W4 LD
1_SD
2_SD
2_LD
3_SD
3_LD
4_SD
4_LD


Probe Contact

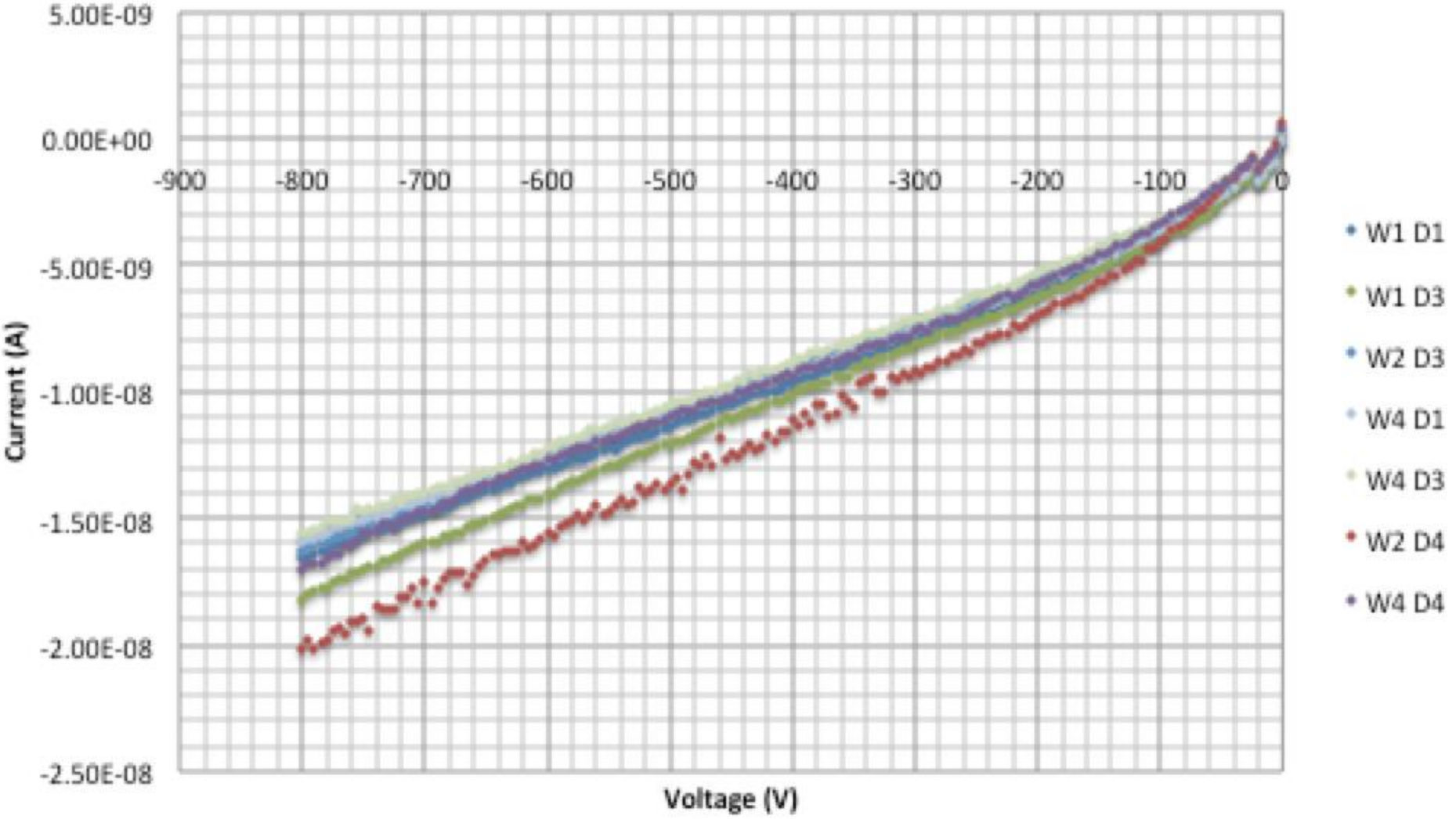

1/C^2 Large Diodes Across Wafers 1-4
3E+21
2.5E+21
2E+21
1.5E+21
1E+21
5E+20
0
1/C^2
-350
-300
-250
-200
-150
-100
-50
0
Voltage (V)
W1
W2
W3
W4

Small and Large Diode Conclusions

- Silicon resists breakdown across nearly all tested wafers indicating low levels of impurities
- Leakage currents are low indicating that the guard ring is providing good isolation
- C-V curve indicates full depletion at 170V-close to the expected value.

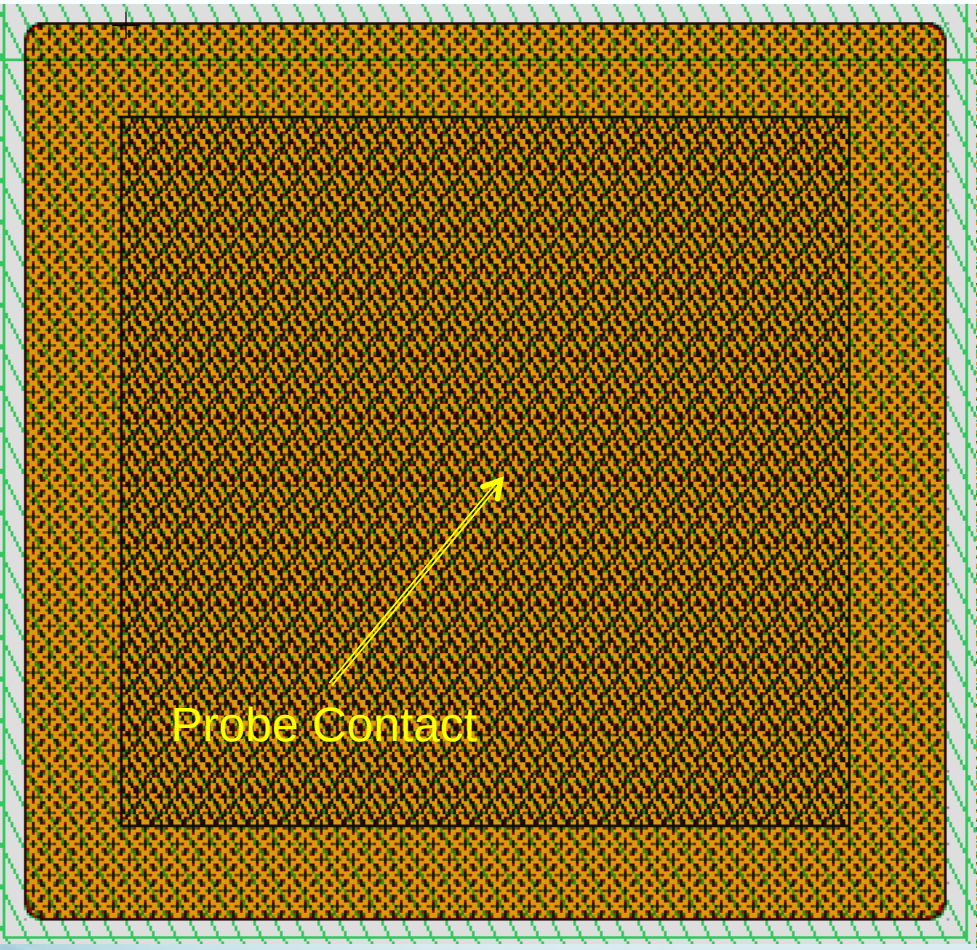

“Effective Edge”
Wafer Edge

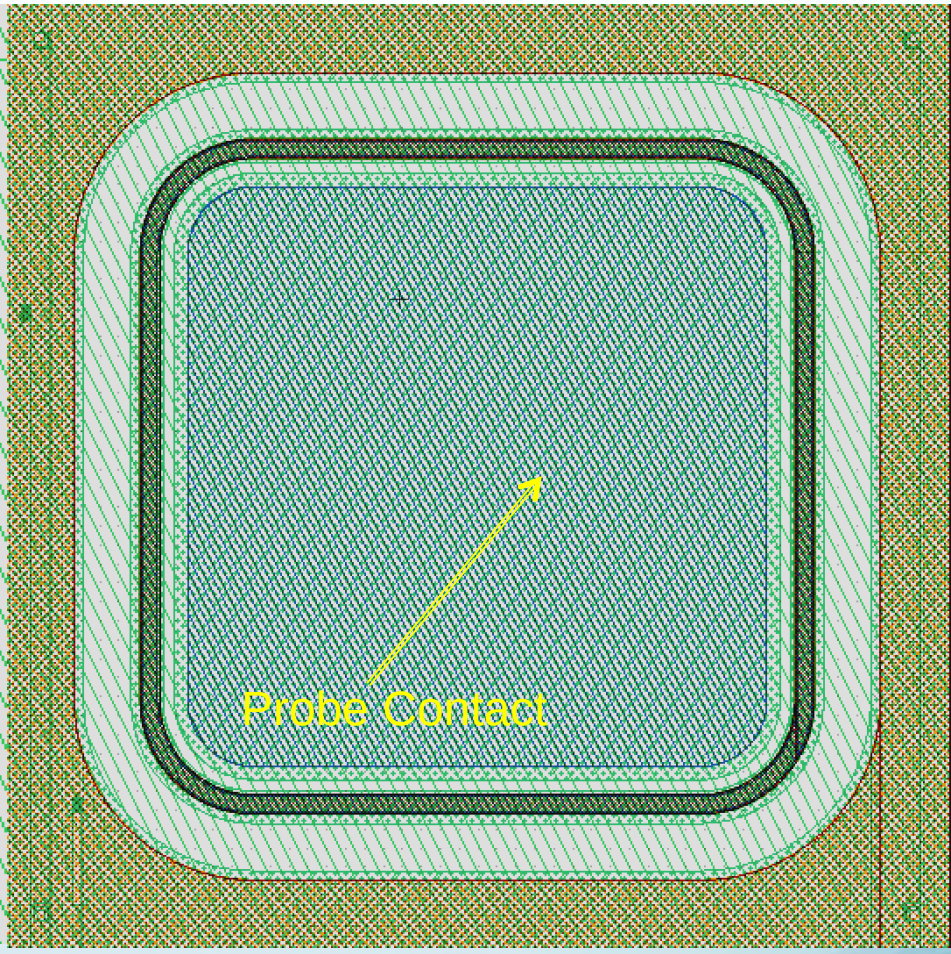
'Normal' IV Curves Wafers 1-4 Diodes 1-4



J Die Diode Conclusions

- I-V Curves show that a majority of diodes go into breakdown early, indicating that structures this close the edge are prone to the effects of edge currents
- Building structures this close to the ‘effective edge’ is not viable


Probe Contact


Probe Contact

MOS1: Oxide Thickness: 4 microns

Capacitance: 2.16 nanoFarad (.863 nF/cm^2)

MOS2: Oxide Thickness: 5 microns

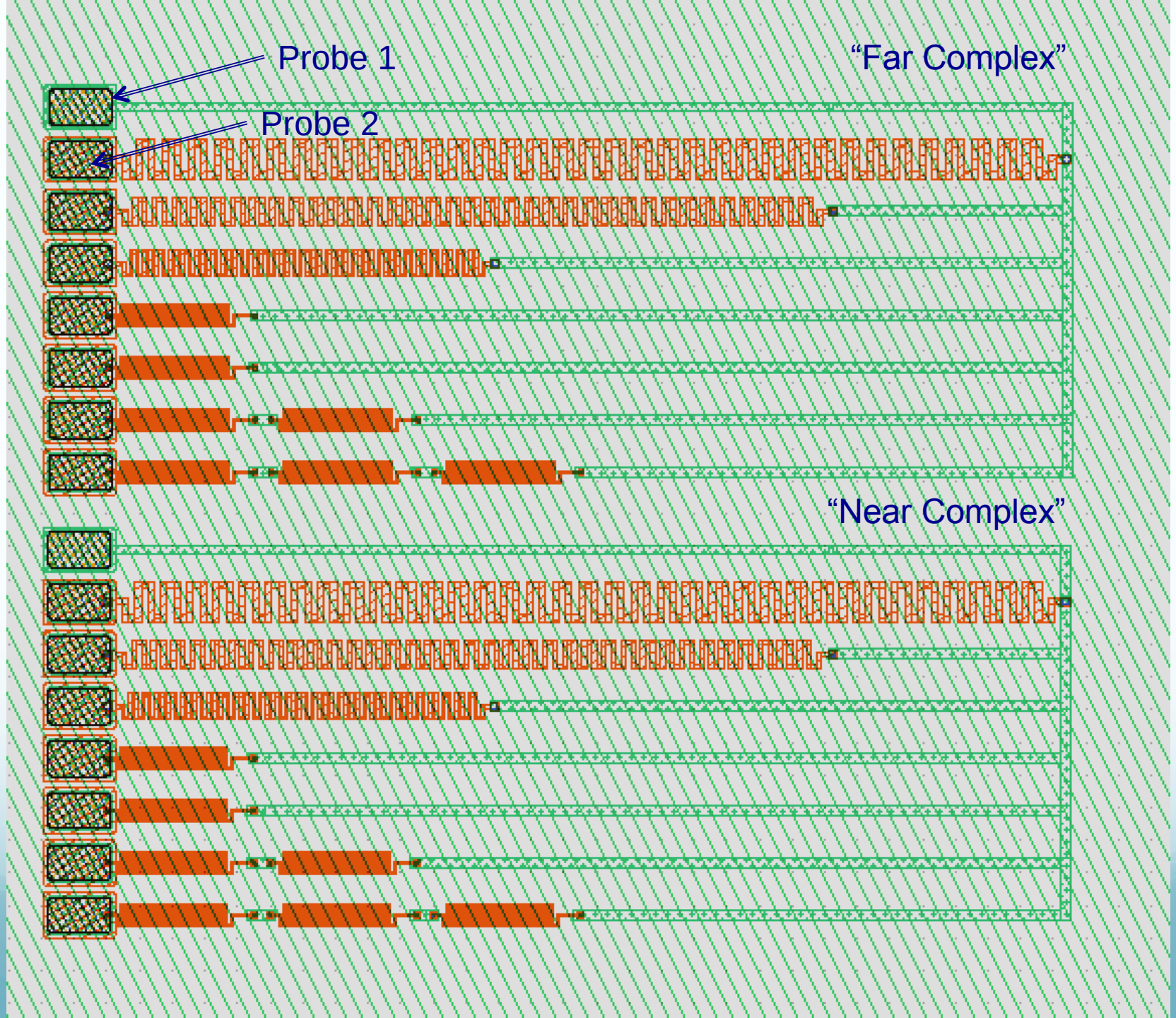
Capacitance: 2.5 nanoFarad (.690 nF/cm^2)

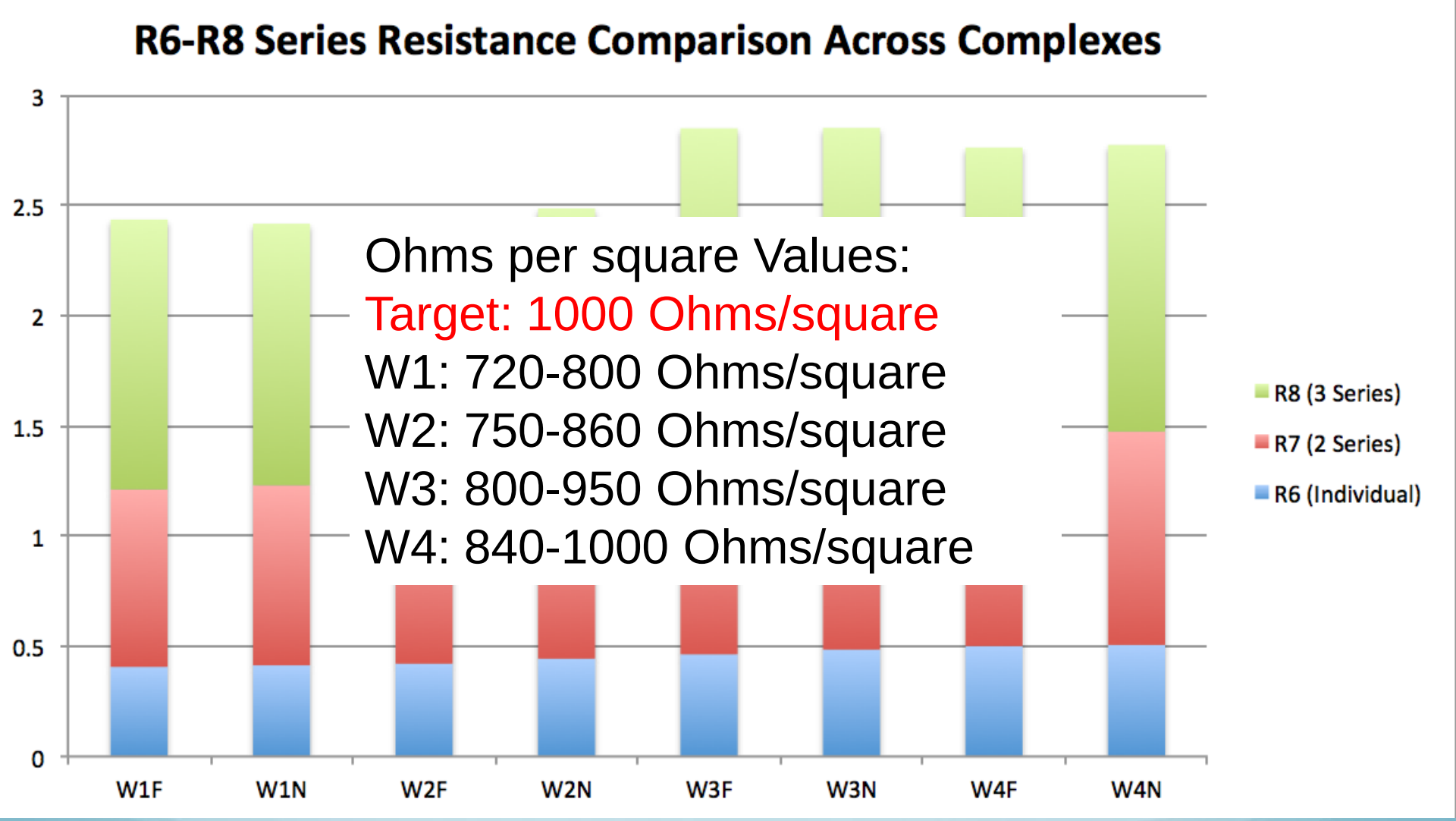
MOS3 Capacitance: 4.75 nanoFarad (21.6 nF/cm^2)

MOS3 Oxide Thickness: 0.17 microns

Expected MOS3: 5.30 nanoFarad (24 nF/cm^2)

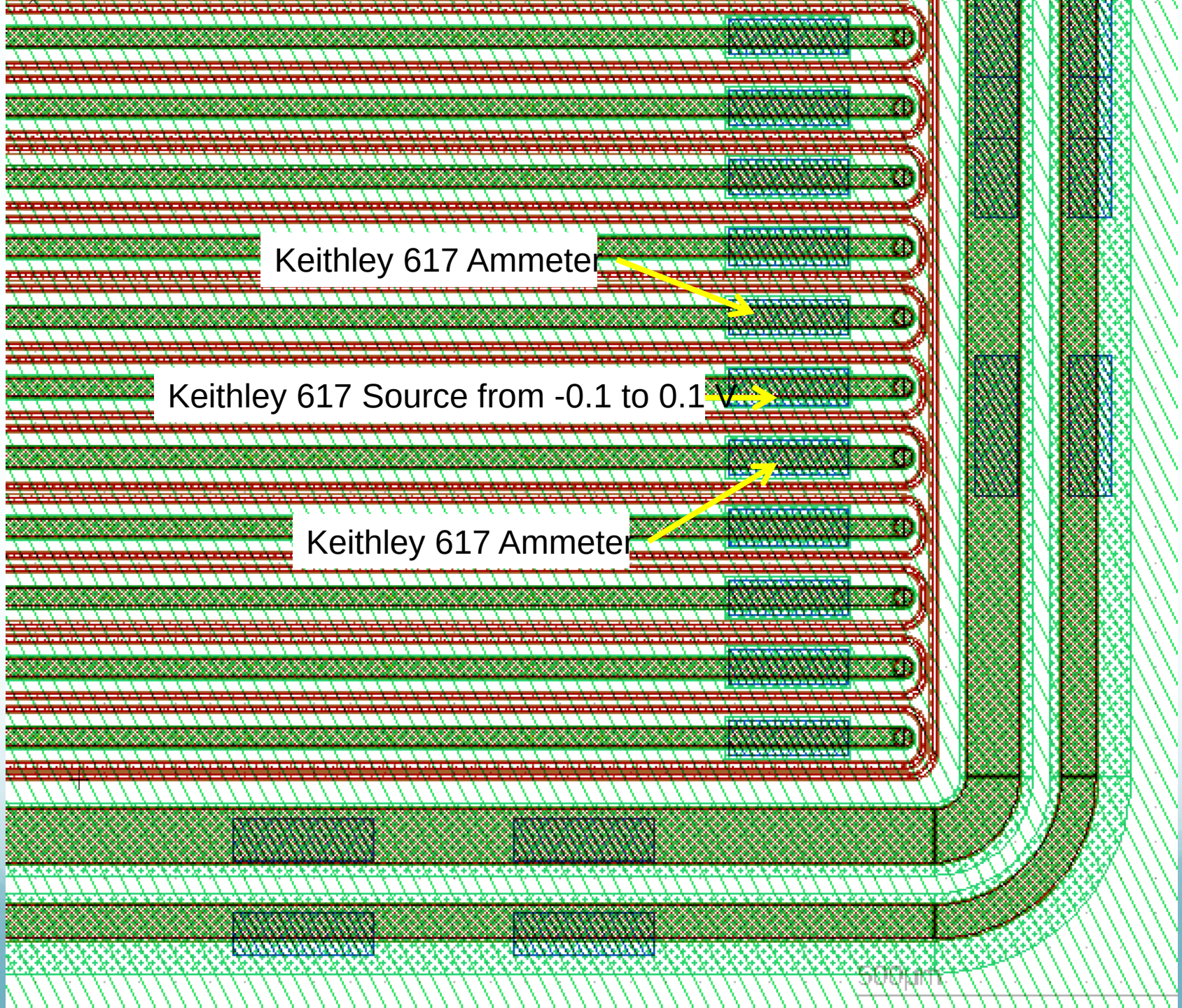
0.10 microns

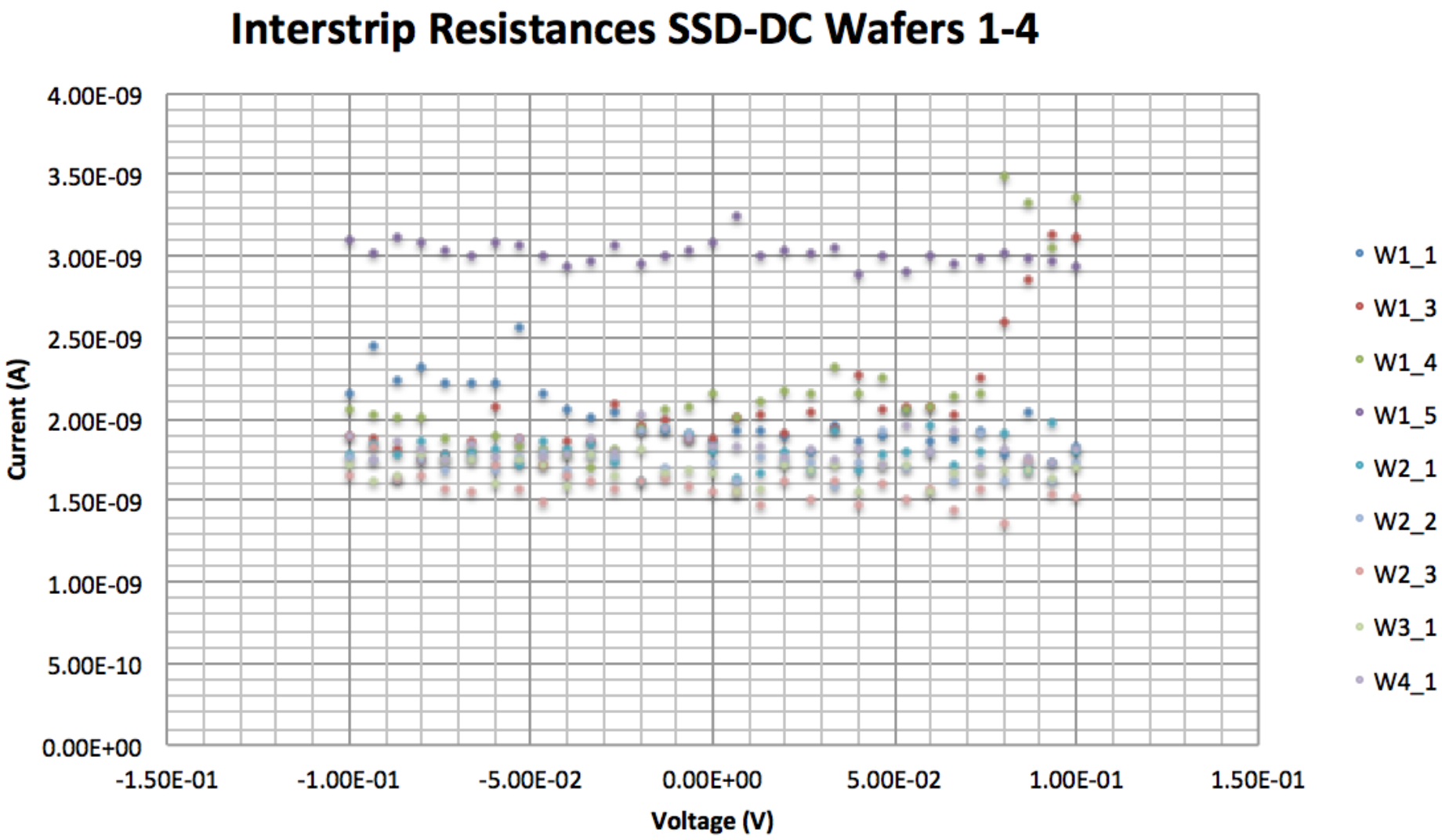

Probe 1
Probe 2
“Far Complex”
“Near Complex”


R6-R8 Series Resistance Comparison Across Complexes
3
2.5
2
1.5
1
0.5
0
W1F
W1N
W2F
W2N
W3F
W3N
W4F
W4N
R8 (3 Series)
R7 (2 Series)
R6 (Individual)
Ohms per square Values:
Target: 1000 Ohms/square
W1: 720-800 Ohms/square
W2: 750-860 Ohms/square
W3: 800-950 Ohms/square
W4: 840-1000 Ohms/square

Polysilicon Resistor Conclusions

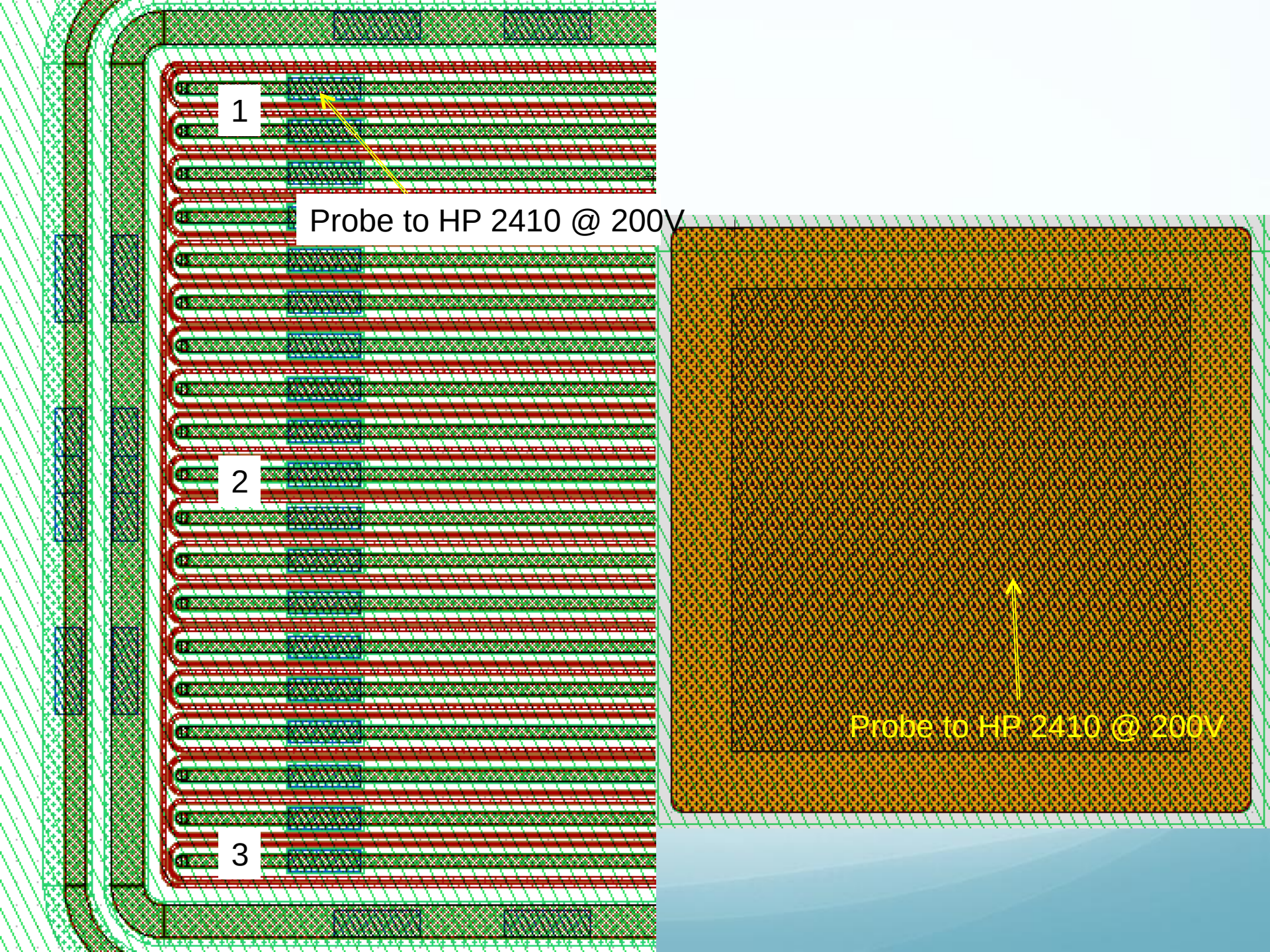
- Overall resistances are consistent between complexes on each wafer although less than expected
- Manufacturing differences have caused large variation between resistances on different wafers, this must be fixed before further use in AC coupled strip detectors
- Series resistances are somewhat inconsistent illustrating some difficulties with manufacturing

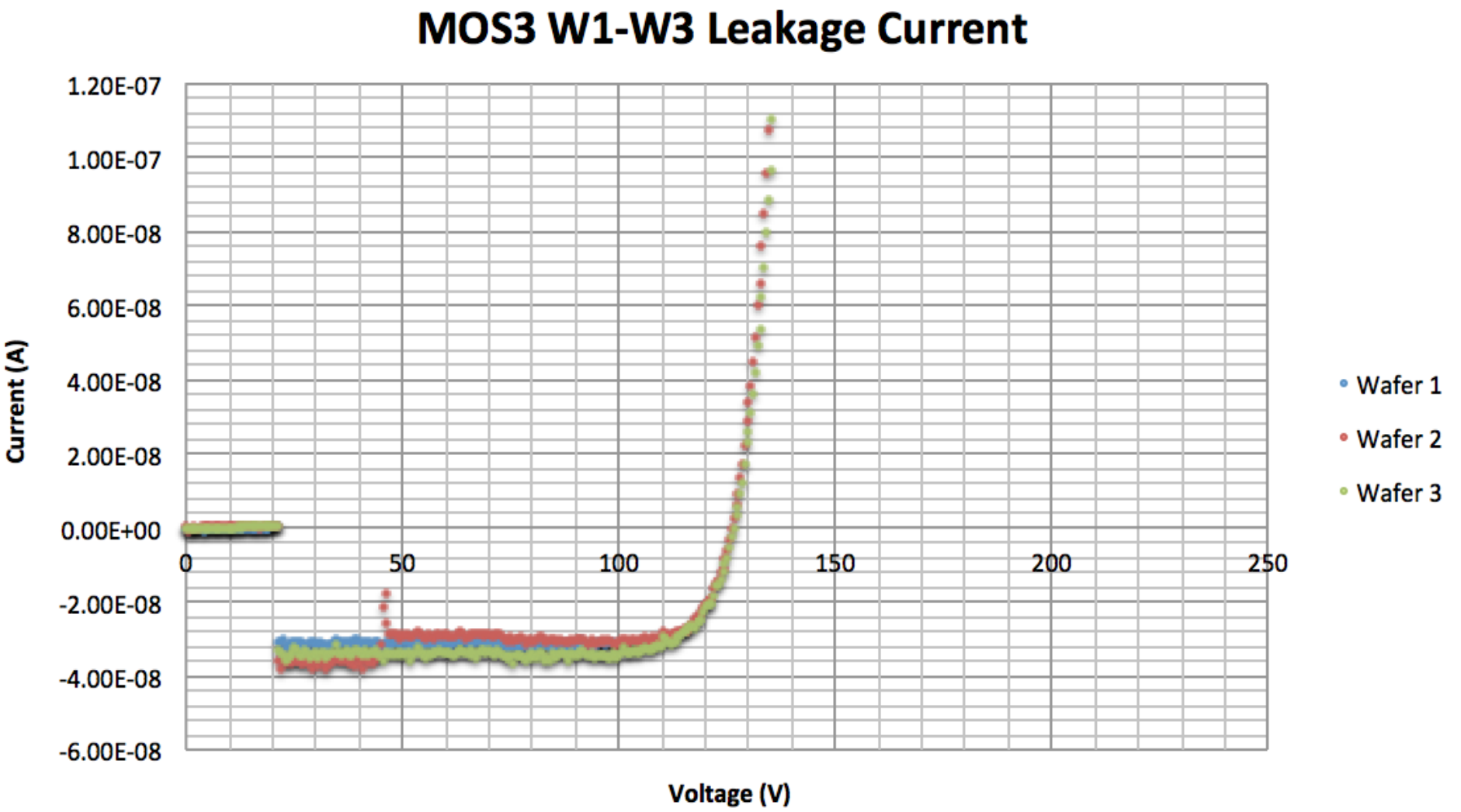

Keithley 617 Ammeter
Keithley 617 Source from -0.1 to 0.1 V
Keithley 617 Ammeter


Interstrip Resistances SSD-DC Wafers 1-4
4.00E-09
3.50E-09
3.00E-09
2.50E-09
2.00E-09
1.50E-09
1.00E-09
5.00E-10
0.00E+00
Current (A)
-1.50E-01
-1.00E-01
-5.00E-02
0.00E+00
5.00E-02
1.00E-01
1.50E-01
Voltage (V)
W1_1
W1_3
W1_4
W1_5
W2_1
W2_2
W2_3
W3_1
W4_1

Interstrip Resistance Conclusions

- P-stops are working correctly as resistances are >1 gigaOhm for wafers 2-4 and around 0.5 gigaOhm for wafer 1
- Further testing with a more accurate setup (lower humidity, measuring voltage drop with a current source) is required for truly accurate measurements


1
Probe to HP 2410 @ 200V
2
3
Probe to HP 2410 @ 200V


MOS3 W1-W3 Leakage Current
1.20E-07
1.00E-07
8.00E-08
6.00E-08
4.00E-08
2.00E-08
0.00E+00
-2.00E-08
-4.00E-08
-6.00E-08
Current (A)
0
50
100
150
200
250
Voltage (V)
Wafer 1
Wafer 2
Wafer 3

Breakdown Voltage Conclusions

- Breakdowns are expected with this test but the oxide layer held up surprisingly well, especially in the strip detector.
- This, and the higher breakdown voltages suggest a high uniformity of oxide thickness and good resistivity

Summary

- Small and Large Diodes are well constructed and underlying bulk silicon is high quality
- J-Die Diodes suffer from early breakdown, especially near the edge of the wafer. In general, detector pixels/strips must be further from the edge to avoid these effects
- Polysilicon Resistors function well, however ohms/square values don’t match up with each other or expected values.
- P-stops and guard rings function well
- Oxide Capacitances are at expected values, along with leakage currents

Thank you for listening!

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