Development of fast, monolithic silicon pixel sensors in a SiGe Bi-CMOS process for TOF-PET

Workshop for development and applications of fast-timing semiconductor devices (8th, December, 2018)

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on behalf of the TT-PET group

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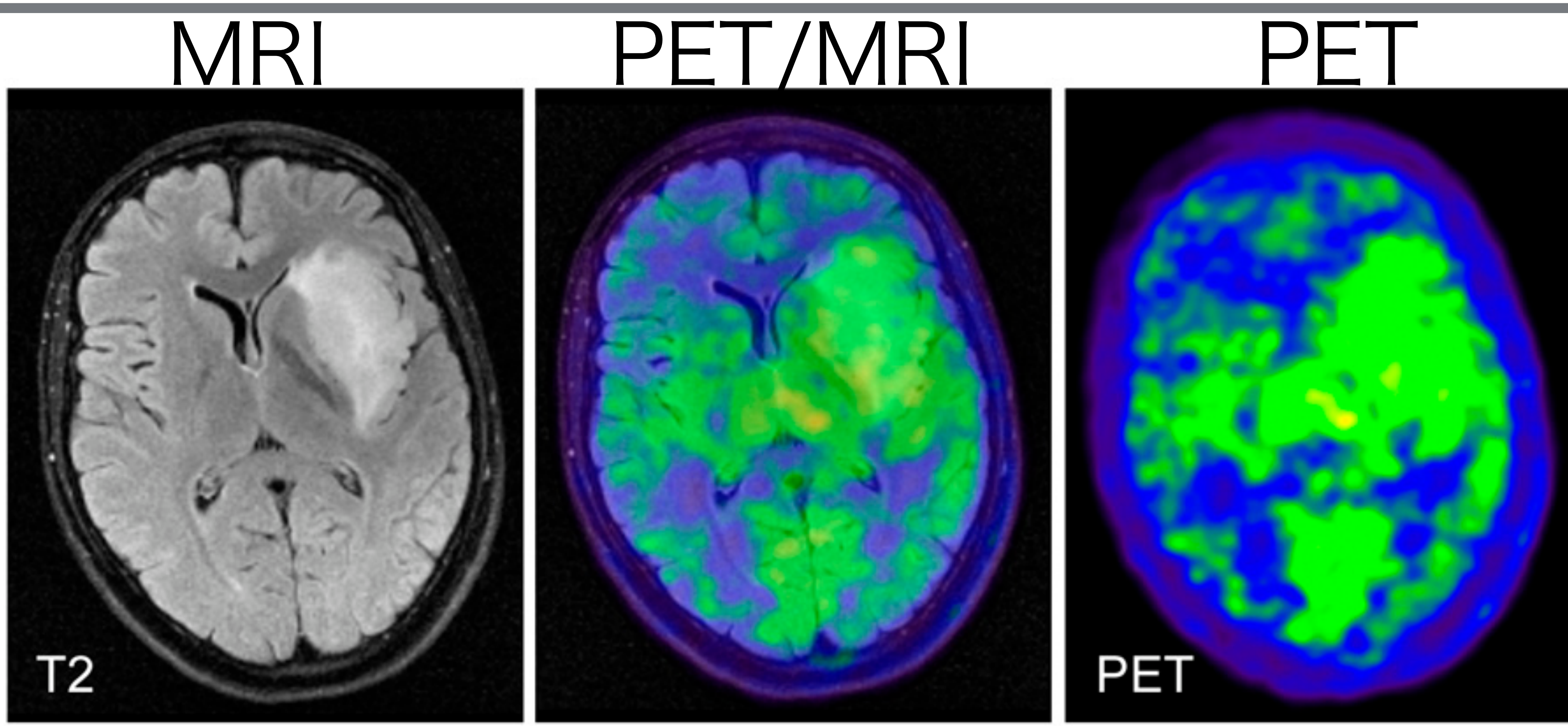
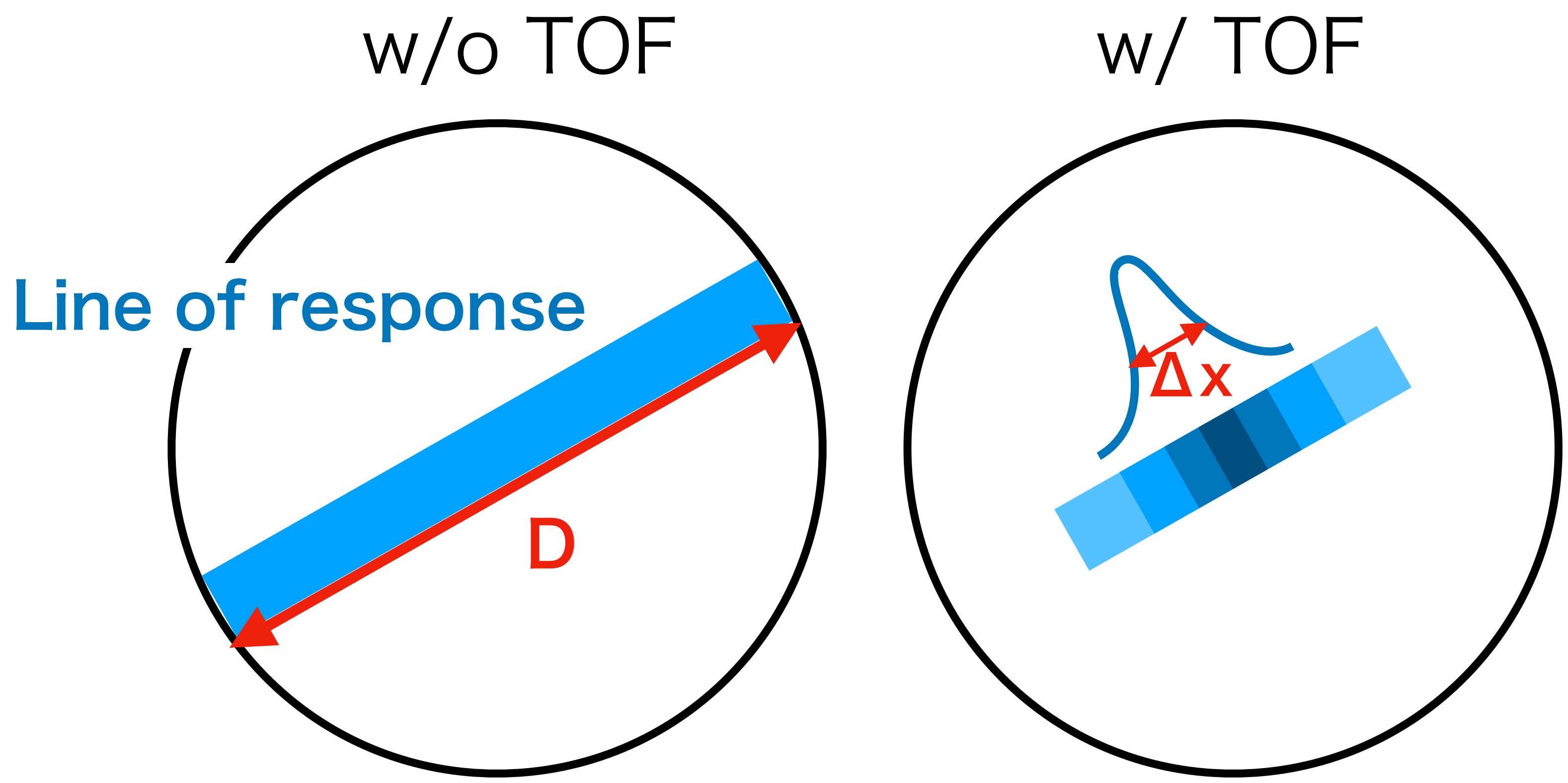
PET/MRI Imaging



(10.2967/jnumed.110.074773)

- Positron Emission Tomography (PET)
  - Positrons from a radionuclide introduced in a body annihilate with the nearby tissue, emitting two back-to-back photons
  - The photons are detected in coincidence, tracking a line of response
- Hybrid PET-MRI Imaging
  - Combining functional Image by PET and morphological image by MRI

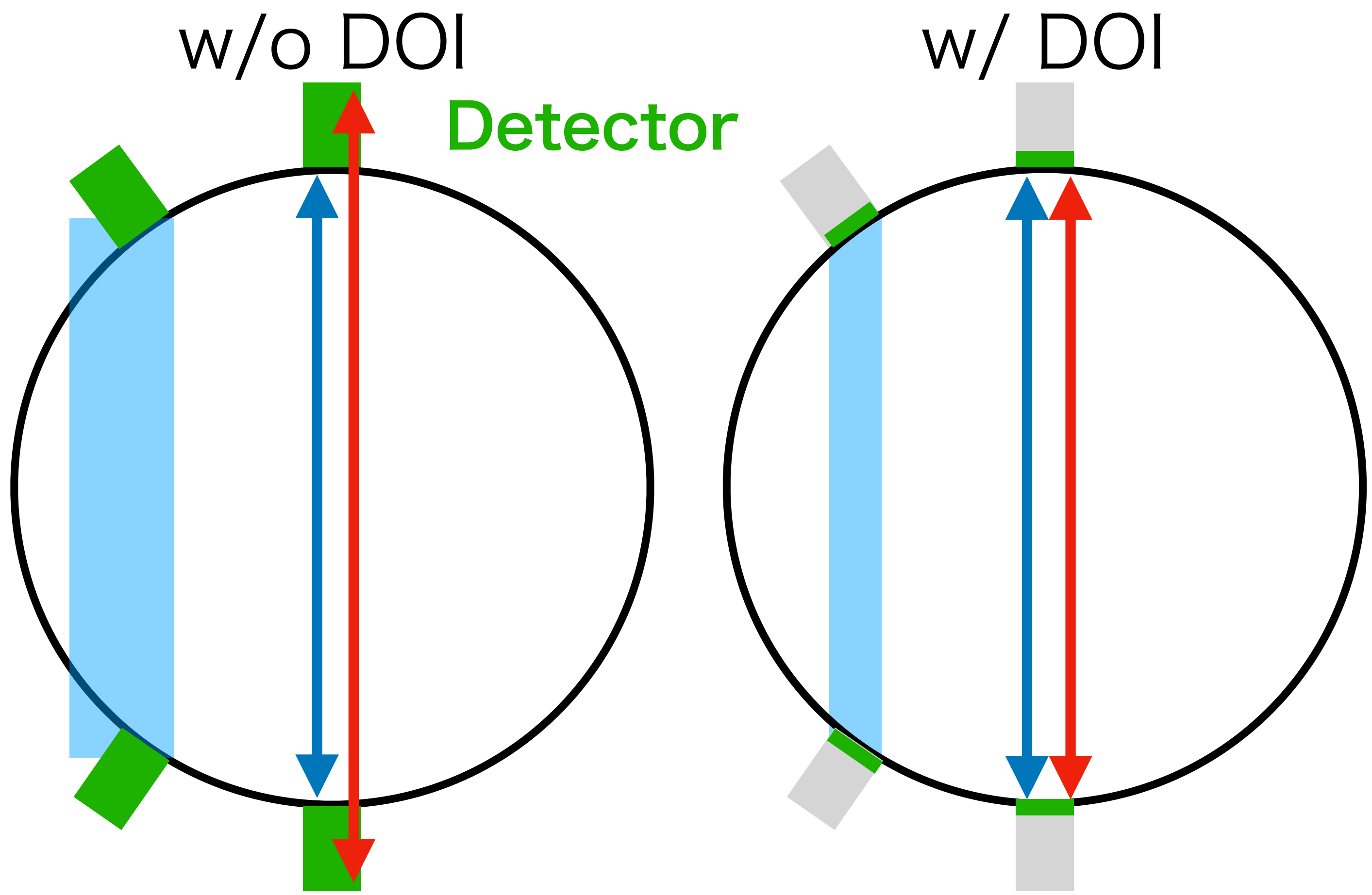
Time-of-Flight (TOF)



- TOF information improves the signal-to-noise ratio (SNR) of reconstructed images

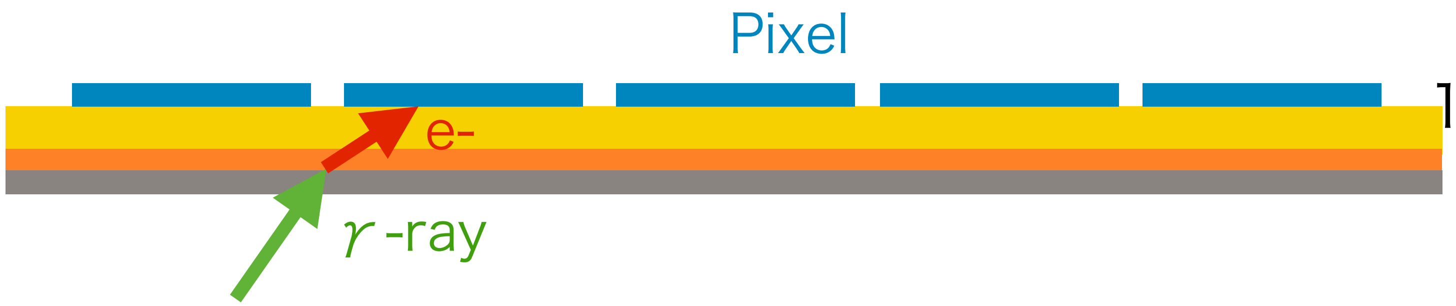
$$\frac{\mathrm{SNR}_{\mathrm{TOF}}}{\mathrm{SNR}_{\mathrm{CONVENTIONAL}}} = \sqrt{\frac{D}{\Delta x}}$$

Depth-of-Interaction (DOI)



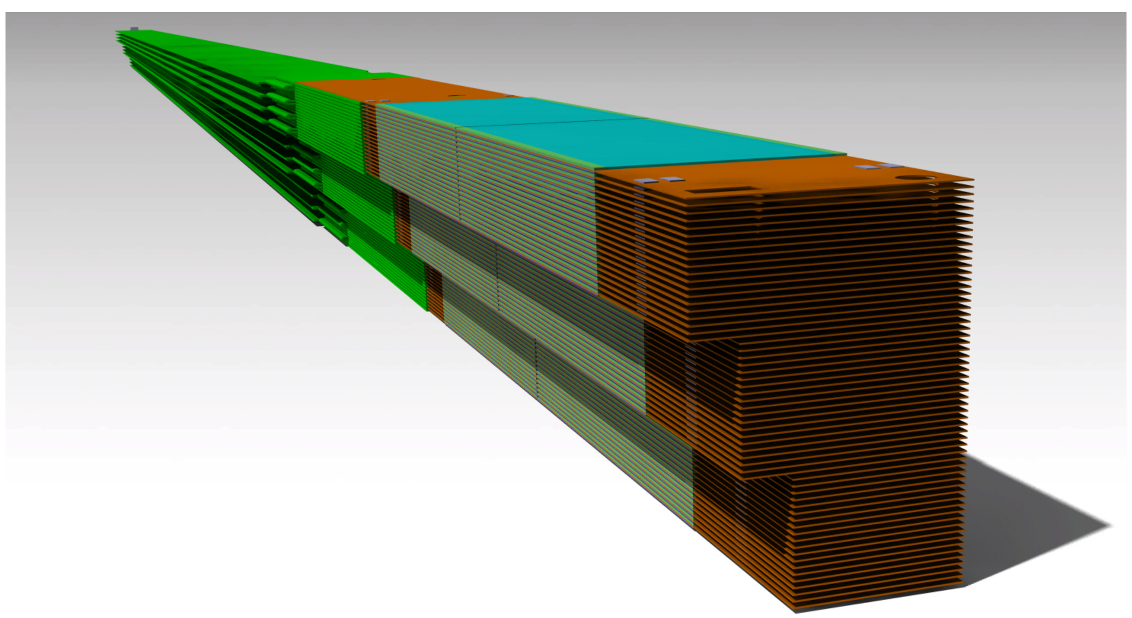
- Sensitivity for photon depth of interaction improves the spatial resolution across the whole view of the scanner
- It also reduces the error of TOF measurements

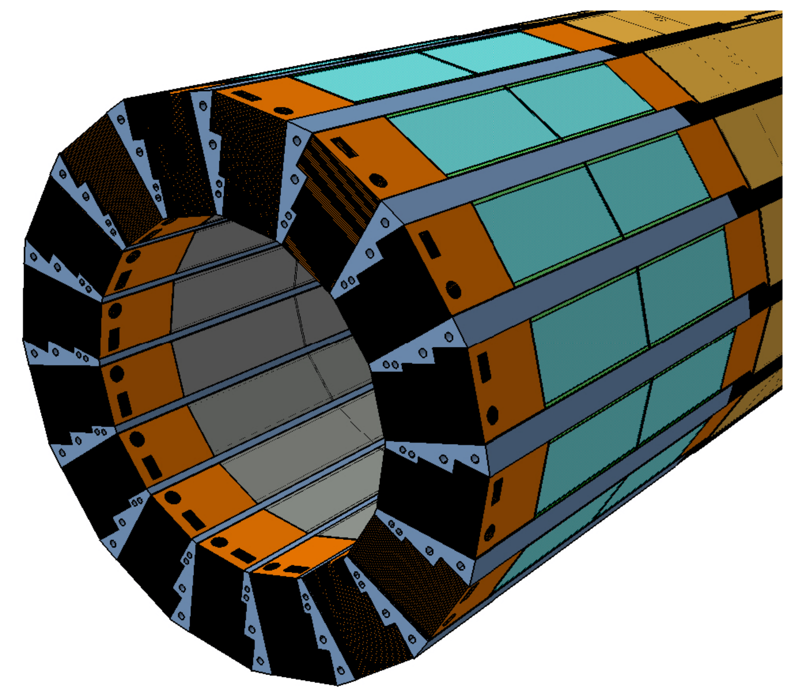
The TT-PET Scanner



- We are developing silicon monolithic pixel sensors with **30 ps** time resolution for electrons
  - corresponding to <u>100 ps time resolution for MIPs</u>

$$\sigma_t \sim \frac{\text{rise time}}{S/N}$$

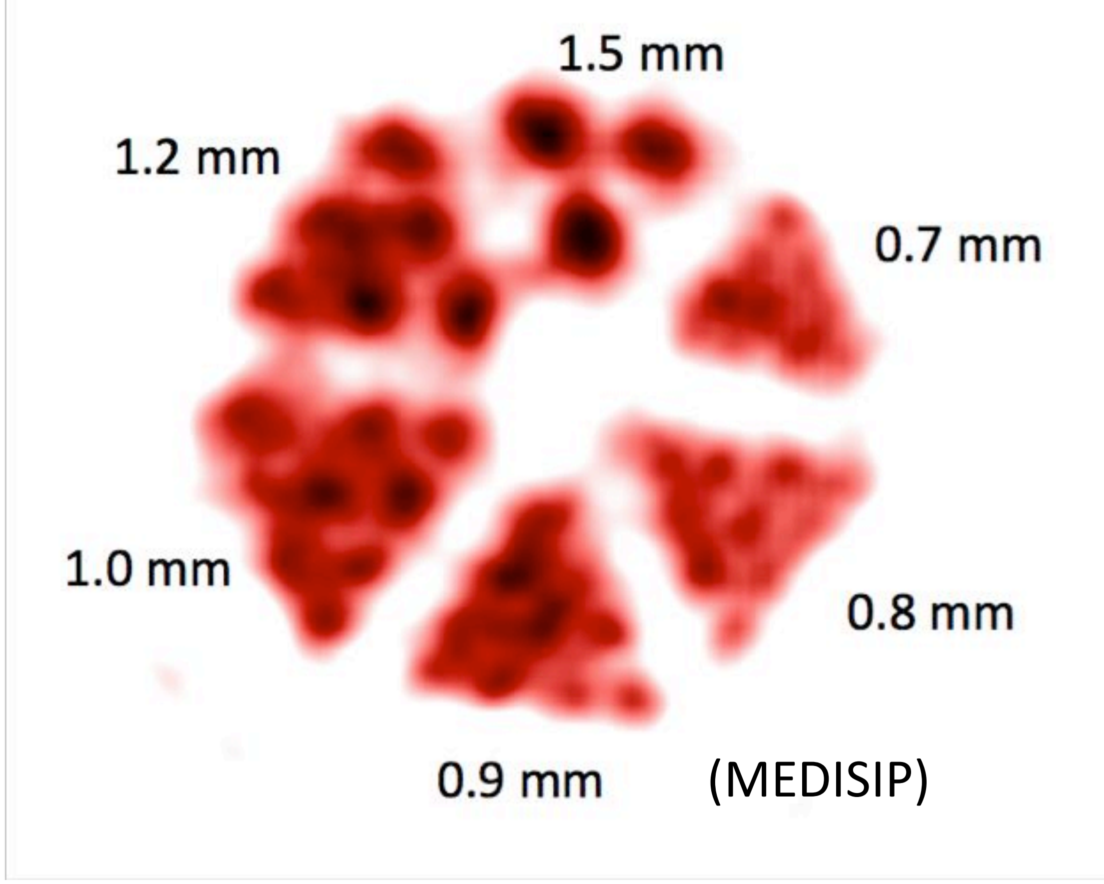




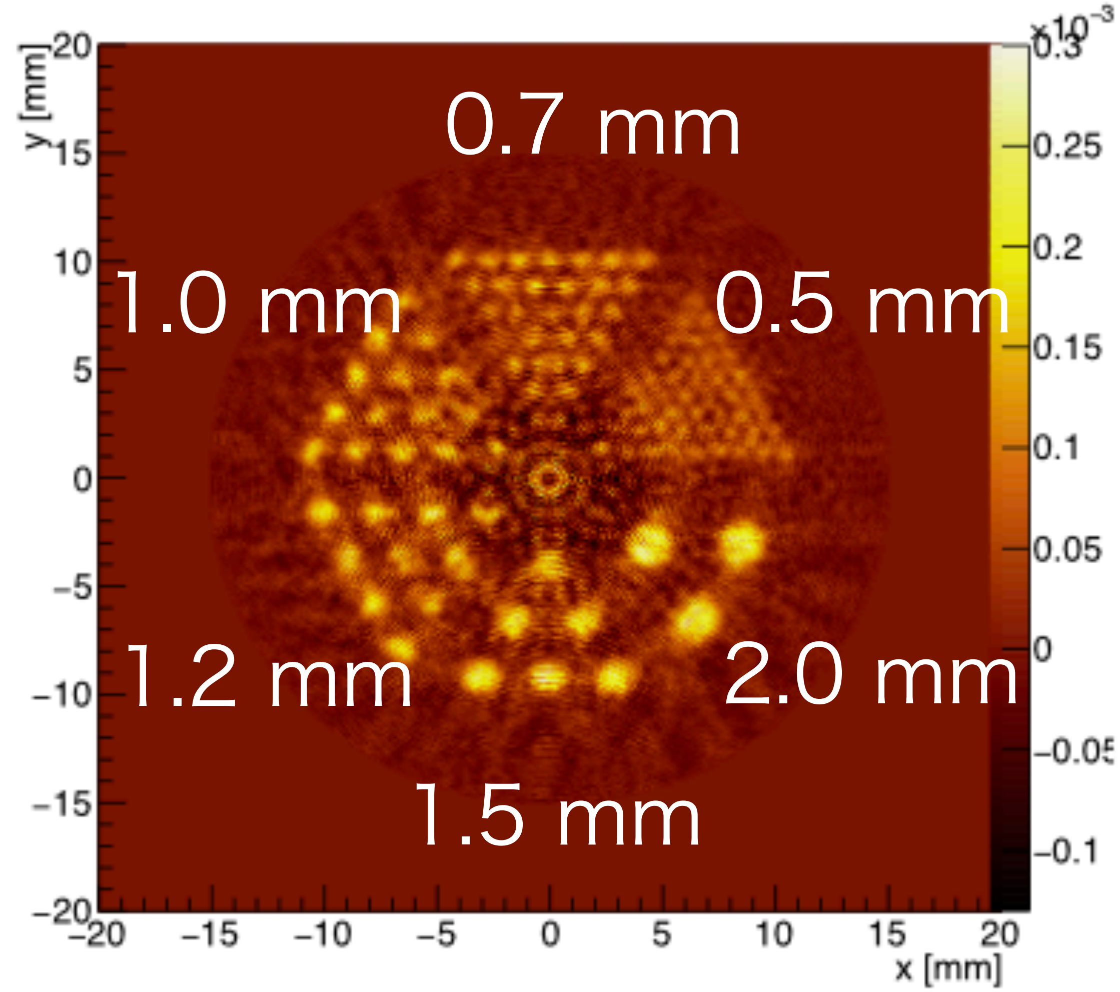
- A wedge is composed of 60 layers
- Total thickness of the wedge is 1.2 cm
- 16 wedges in a ring structure with cooling blocks
- The scanner is meant to be inserted in an existing MRI in Geneva Hospital (HUG)

Expected Performance of the TT-PET Scanner

Typical performance of a TOF PET scanner for small animals

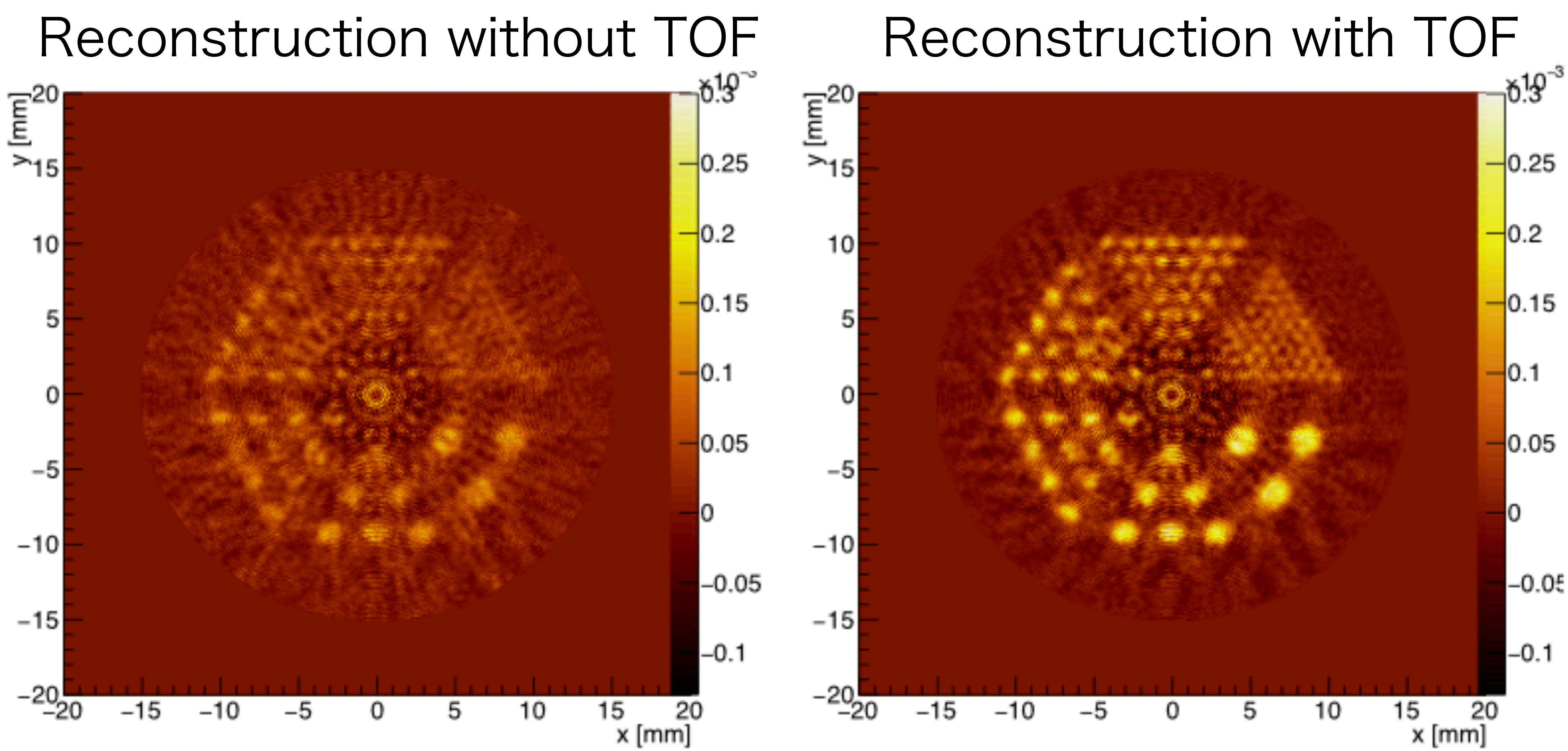


Reconstruction with TOF



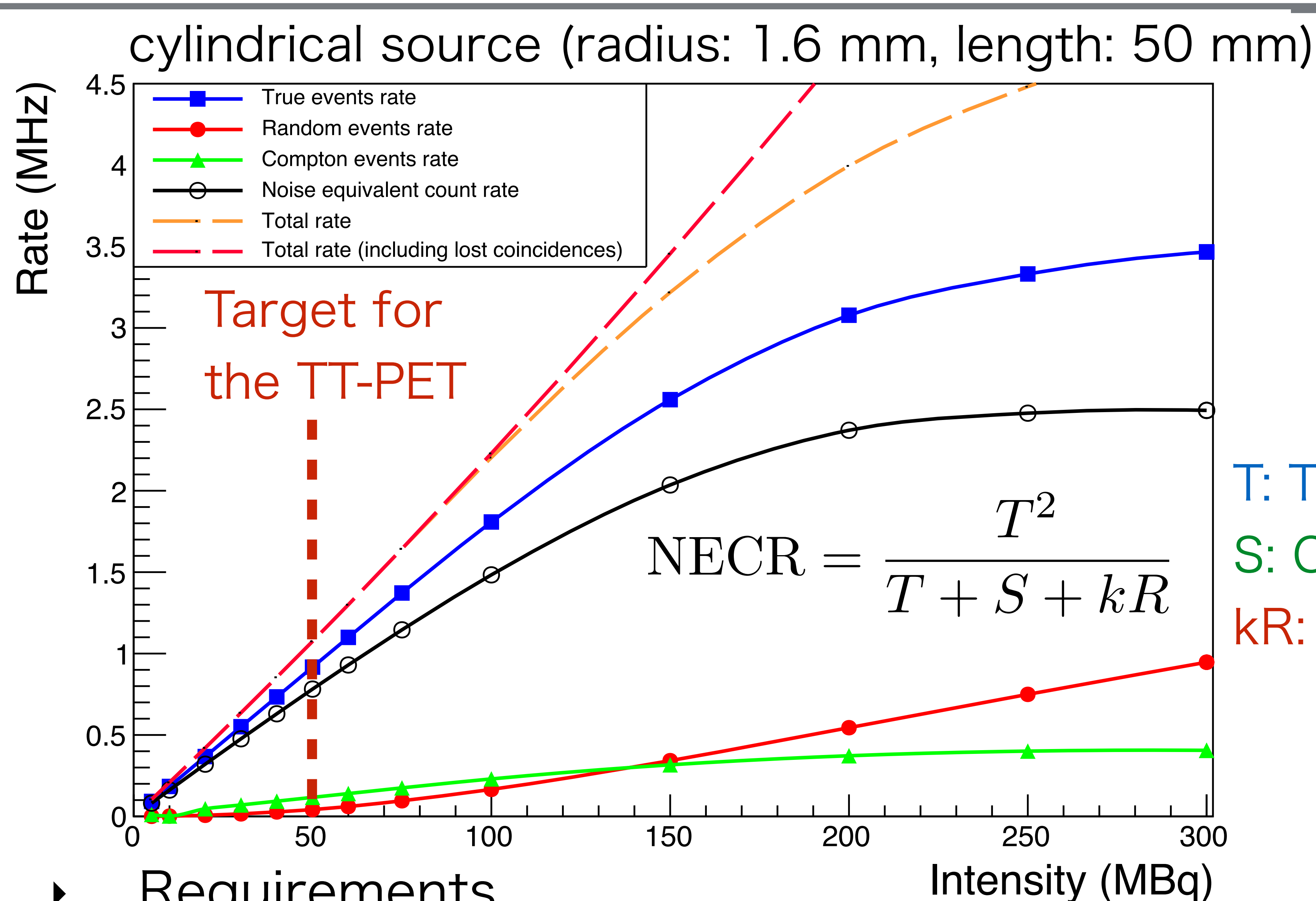
- Detector simulation performed with Geant4 shows excellent performance of the TT-PET scanner
- The spatial resolution (average: 650 μm) does not degrade on the border of the scanner thanks to the depth sensitivity

Expected Performance of the TT-PET Scanner



- The SNR of the reconstructed image is improved thanks to the TOF measurement

Noise Equivalent Count Rate (NECR)



$$\mathrm{NECR} = \frac{T^2}{T + S + kR}$$

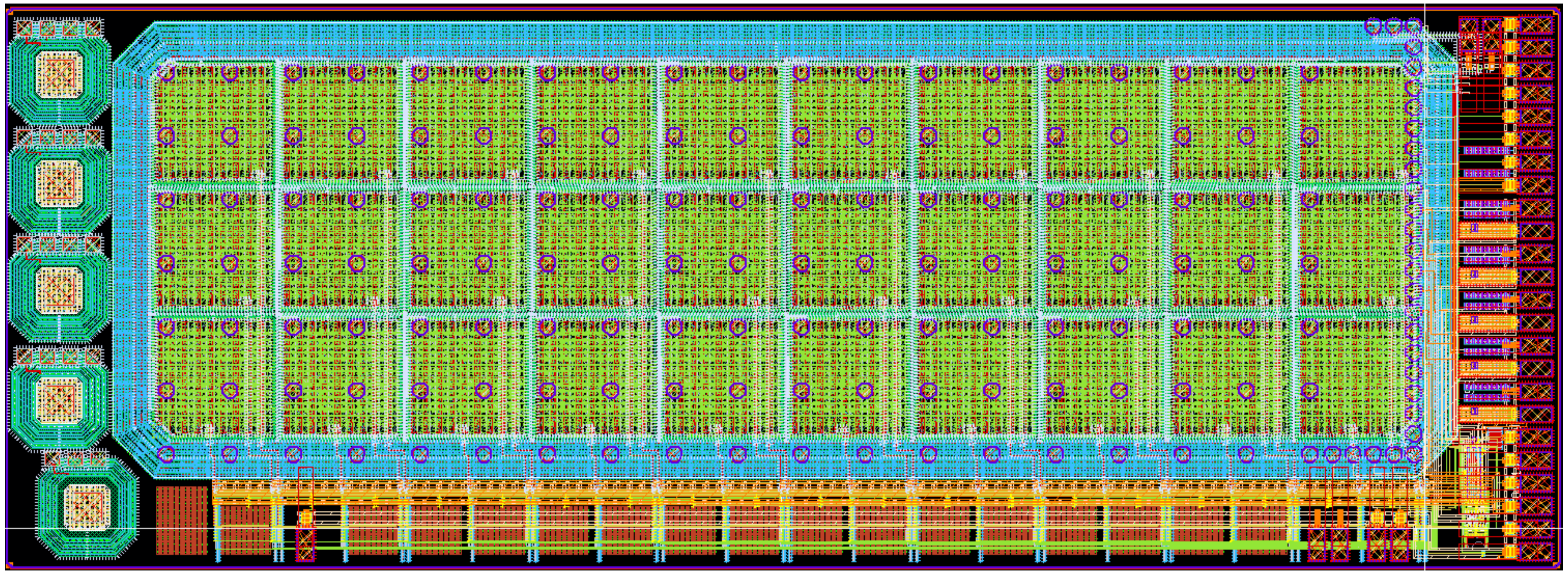
T: True

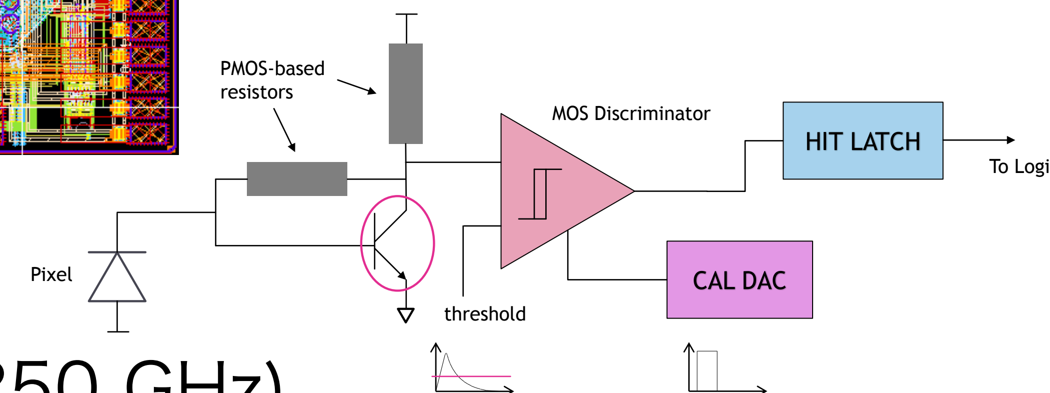
S: Compton Scattering

kR: Random

- Requirements
  - Coincidence window: 500 ps
  - The LOR intercepts the phantom
  - The energy deposits in the both pixels are larger than 20 keV
- Less than 0.1% count loss at 50 MBq

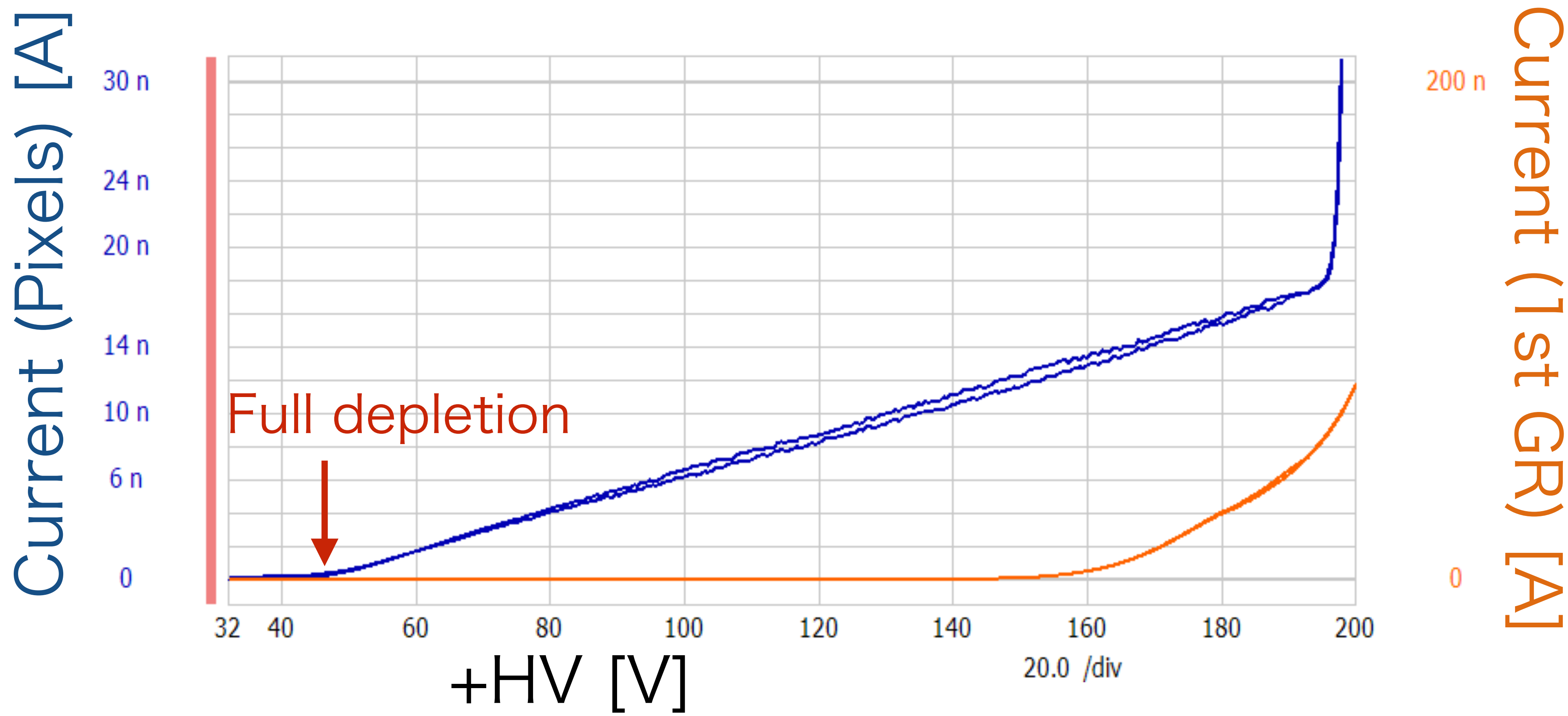
ASIC Prototype





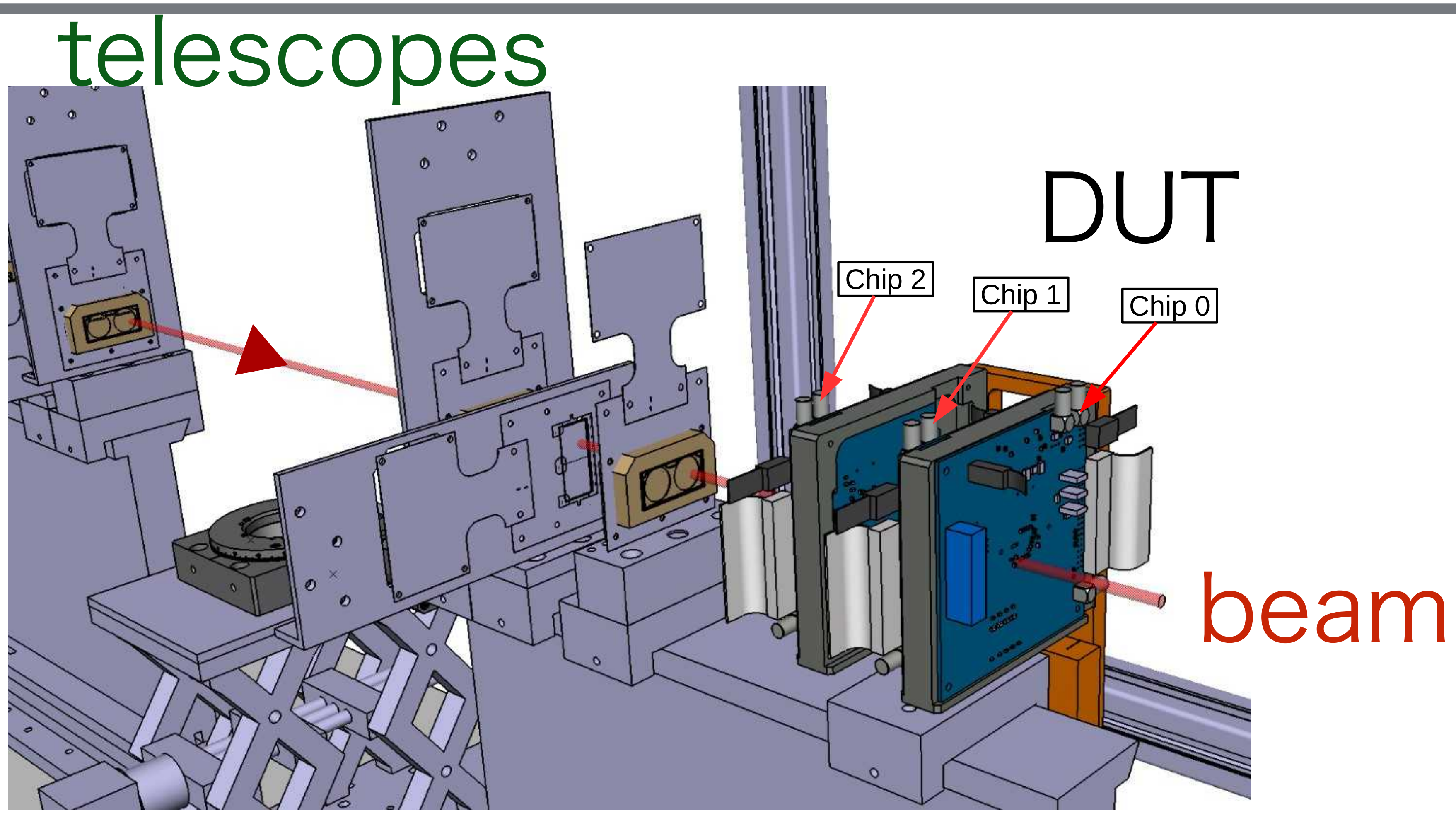
- ASIC Prototype in 130 nm IHP SiGe-HBT technology ($\beta = 900$, $f_T = 250$ GHz)
  - 30 pixels, size: 450 × 450 μm^2
  - Amplifier, discriminator, 50 ps binning TDC, logic and serializers
    - ✦ The output of the discriminator is sent to a fast-OR chain, which preserves TOT and TOA
  - Thinned to 100 μm with backplane metallization
  - 1500 Ω*cm resistivity (full depletion voltage: ~ 45 V)
    - ✦ Confirmed by laser TCT measurement (see backups)

I-V Measurement



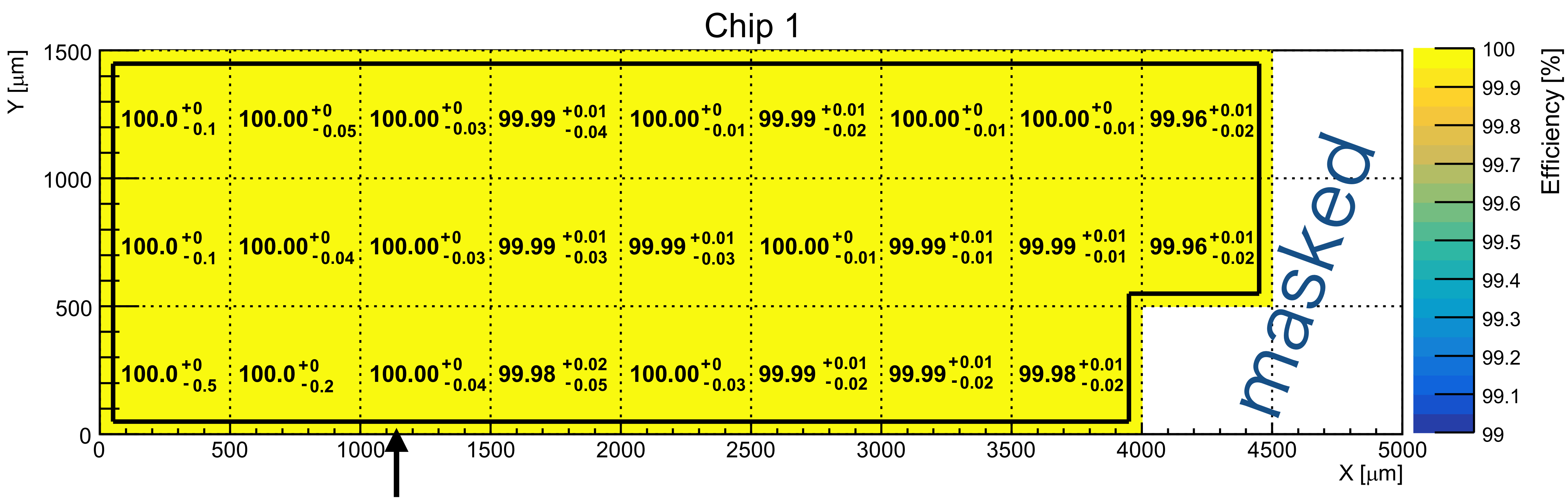
- Ground reference: backplane
- Small leakage current from pixels due to the backside implantation process
  - Negligible impact on the chip performance

Testbeam Measurement



- Testbeam facility at CERN SPS (MIPs)
    - 6 tracking telescopes
    - Readout system developed at the DPNC with custom FPGA firmware
        - ASIC operation
        - External trigger from telescopes
    - Applied 180 V to the pixels

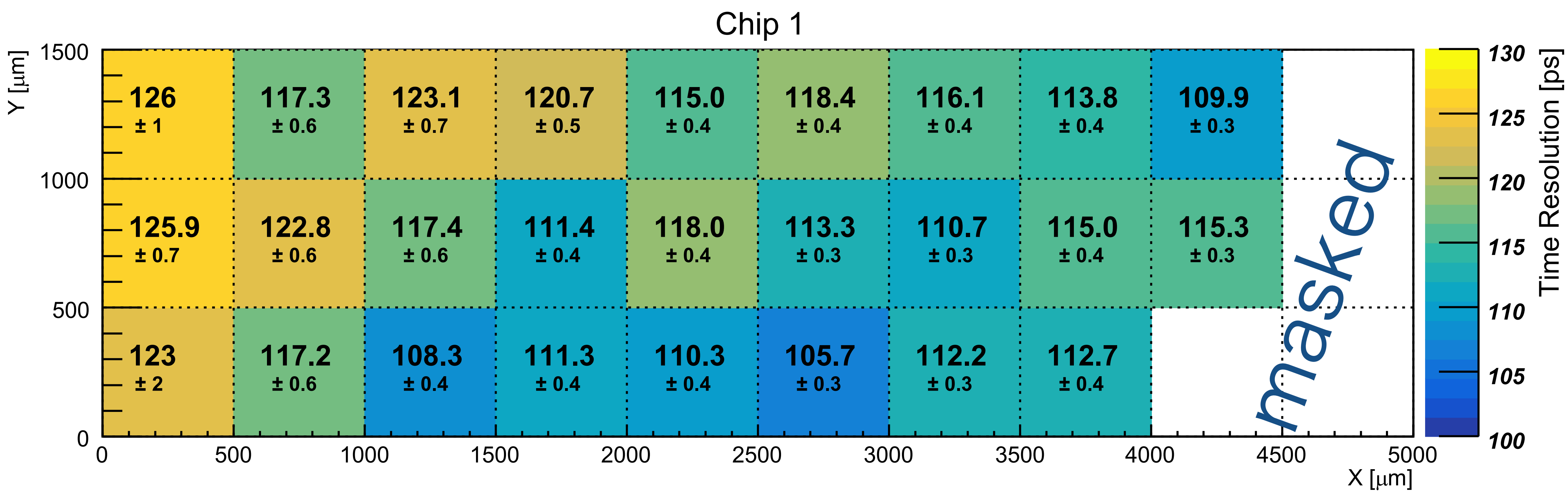
Efficiency Map



Region of interest for efficiency calculation

- Greater than **99% efficiency** was observed for 26 pixels
  - 4 pixels were masked on hardware due to noise induced from signal-ended clock line
  - The region defined by the continuous lines shows the area used for efficiency calculation

Time resolution



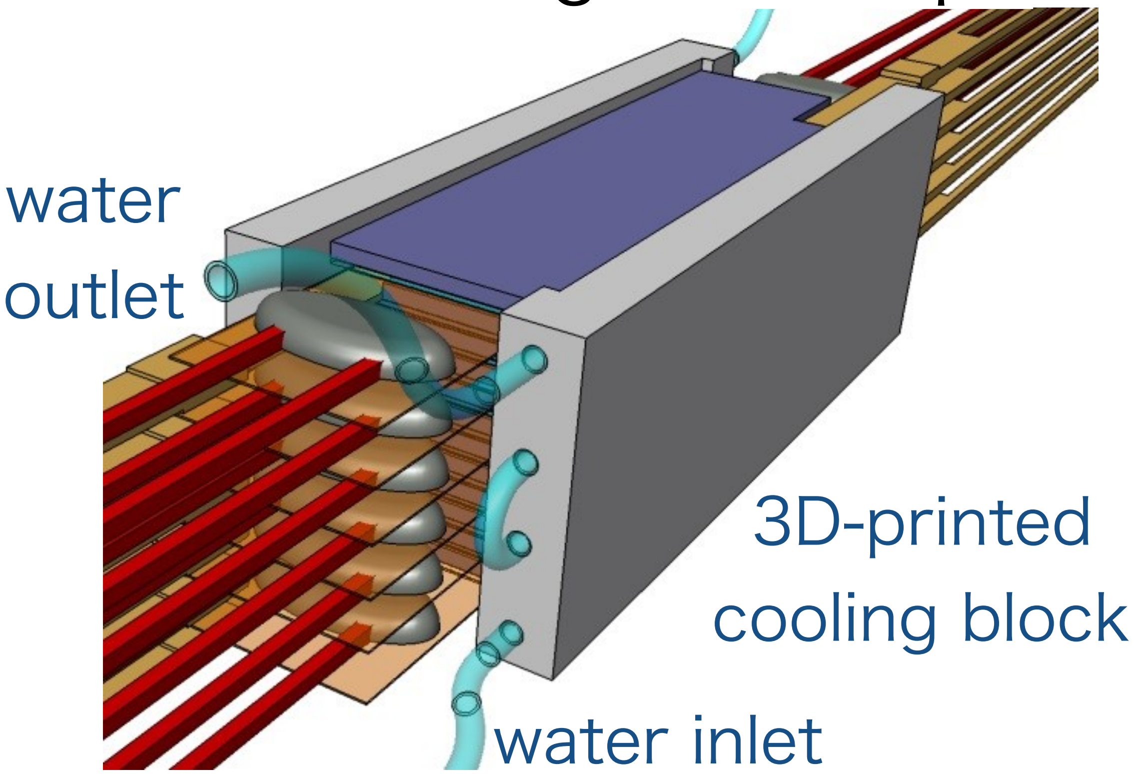
	Time resolution [ps]	
	low-power	high-power
$\sigma_{t,\ chip\ 0}$	**127.3 ± 0.2**	**111.3 ± 0.1**
$\sigma_{t,\ chip\ 1}$	**134.2 ± 0.2**	**116.7 ± 0.1**
$\sigma_{t,\ chip\ 2}$	**127.2 ± 0.2**	**111.2 ± 0.1**

- **110 ps RMS** was measured at high-power consumption working point
  - **130 ps RMS** at low-power consumption working point (compatible with the power-budget of the TT-PET scanner)
- Details of the analysis will be discussed in Pixel 2018!
  - **10.12 (Mon.) 11:35 ~ , L. Paolozzi, ID: 82**

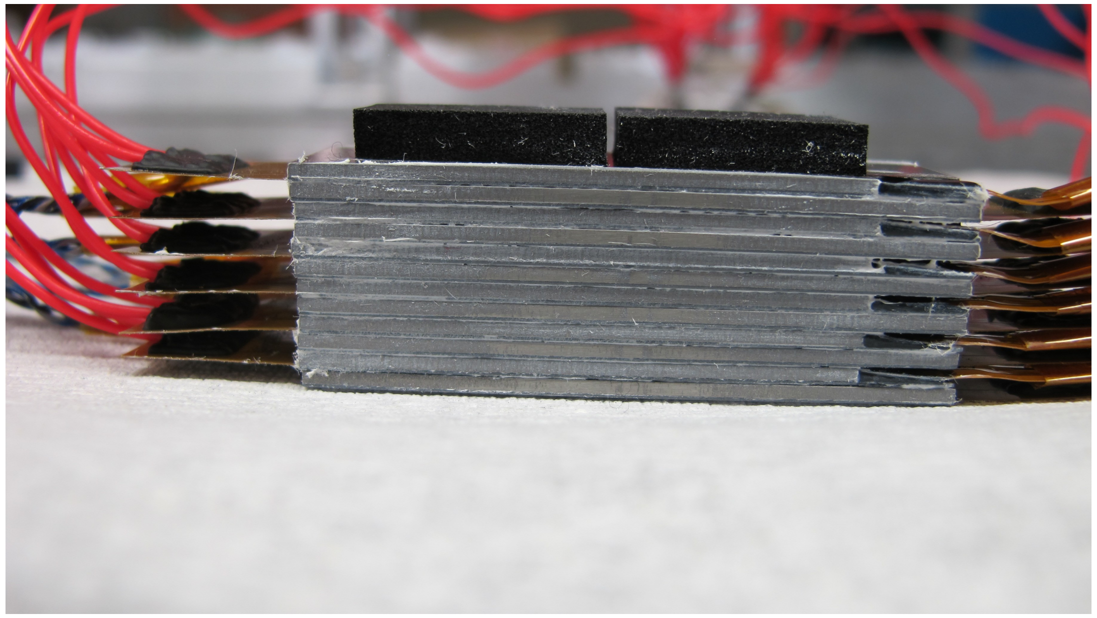
arXiv: 1812.00788

Thermal Measurement

CAD design of setups

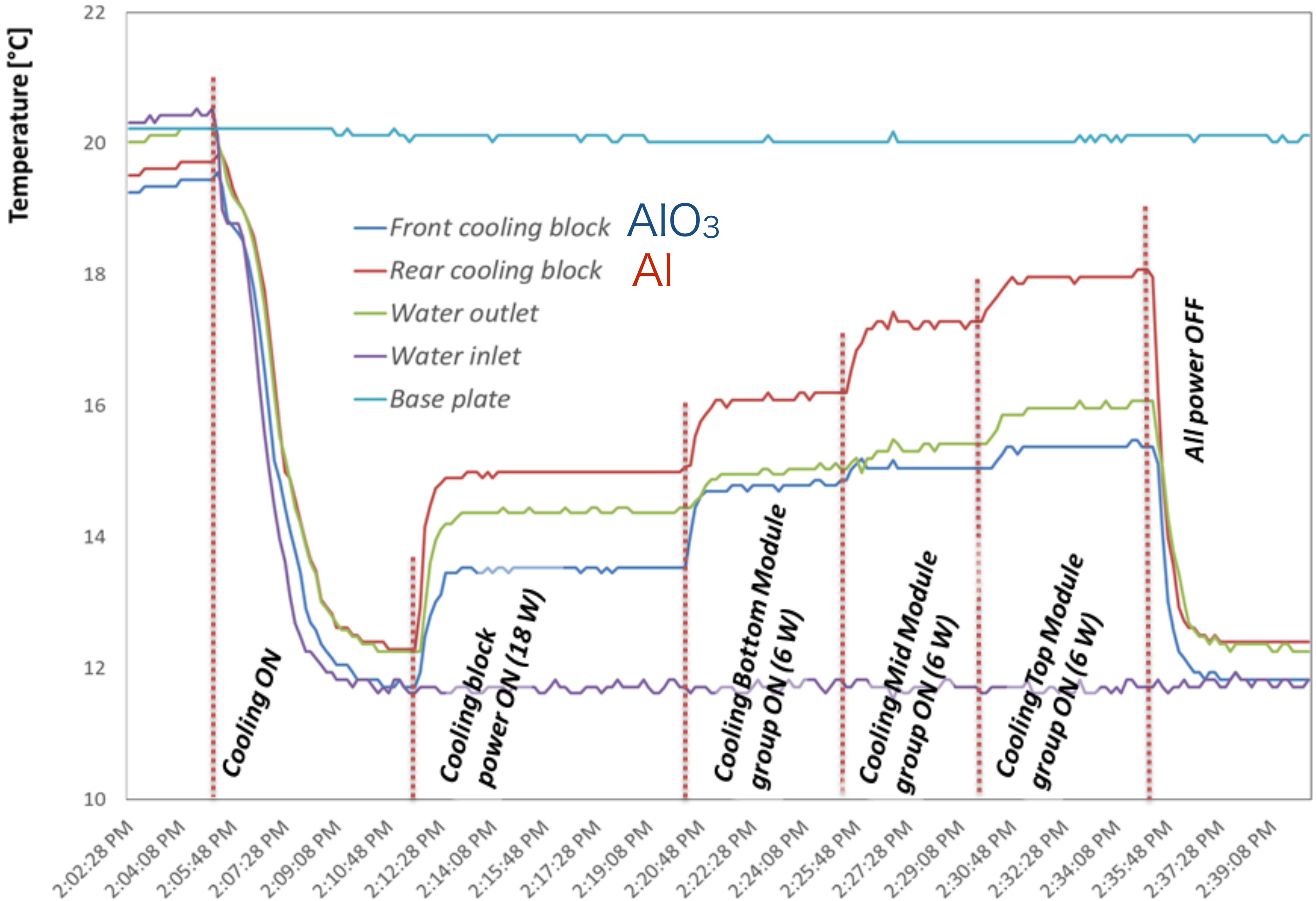


Thermal mock-up



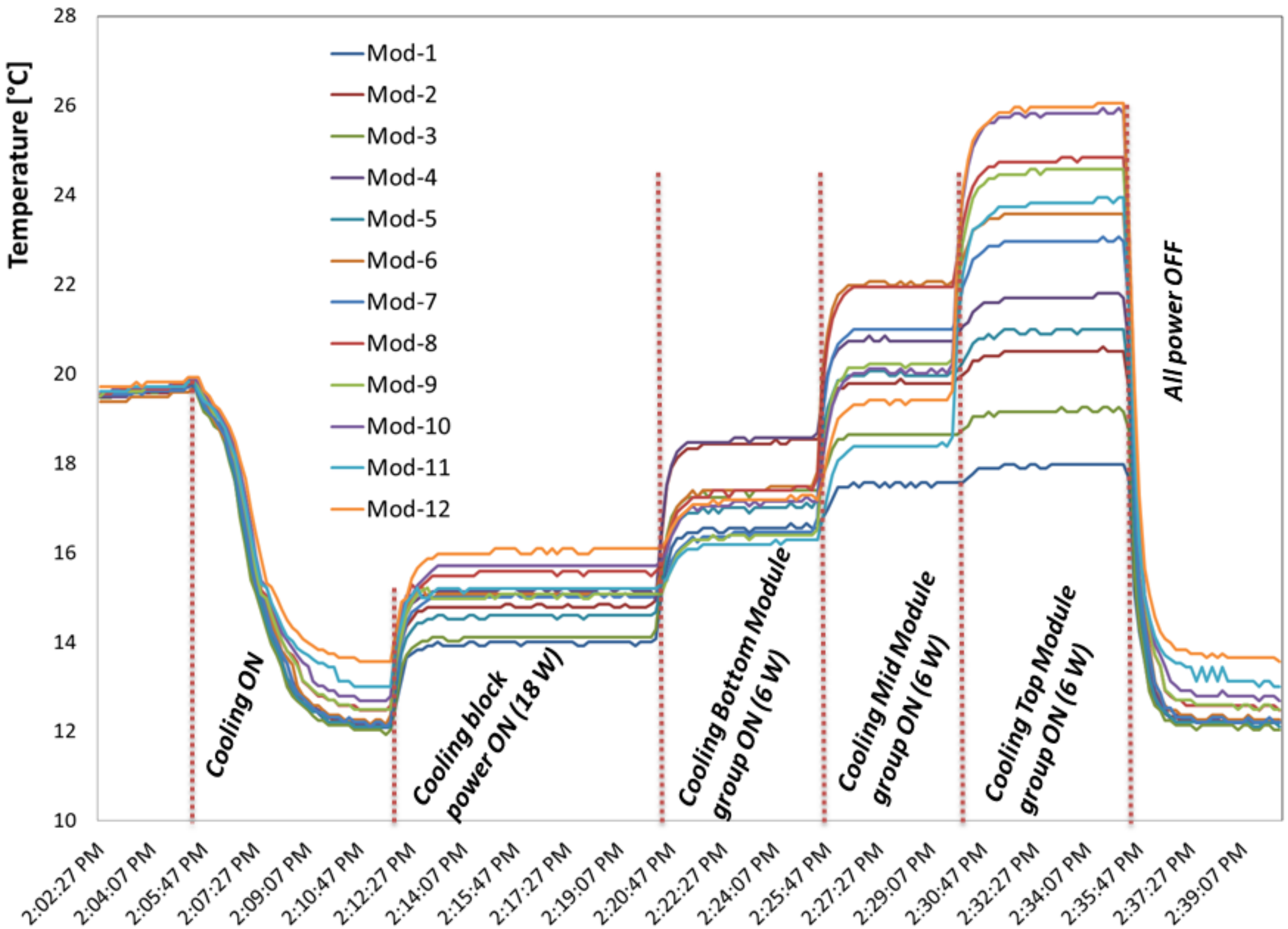
- Need to dissipate 36W within a very compact detector (~ 10 cm^3)
- Two different types of cooling blocks were produced
  - Aluminum oxide ceramic (AlO_3) and Aluminum
- Thermal mockup (power: 36 W total)
  - 18 W to the two heater pads of the cooling blocks
  - 6 W to the top/middle/bottom super-module groups
- Target: maximum temperature of 40 ℃

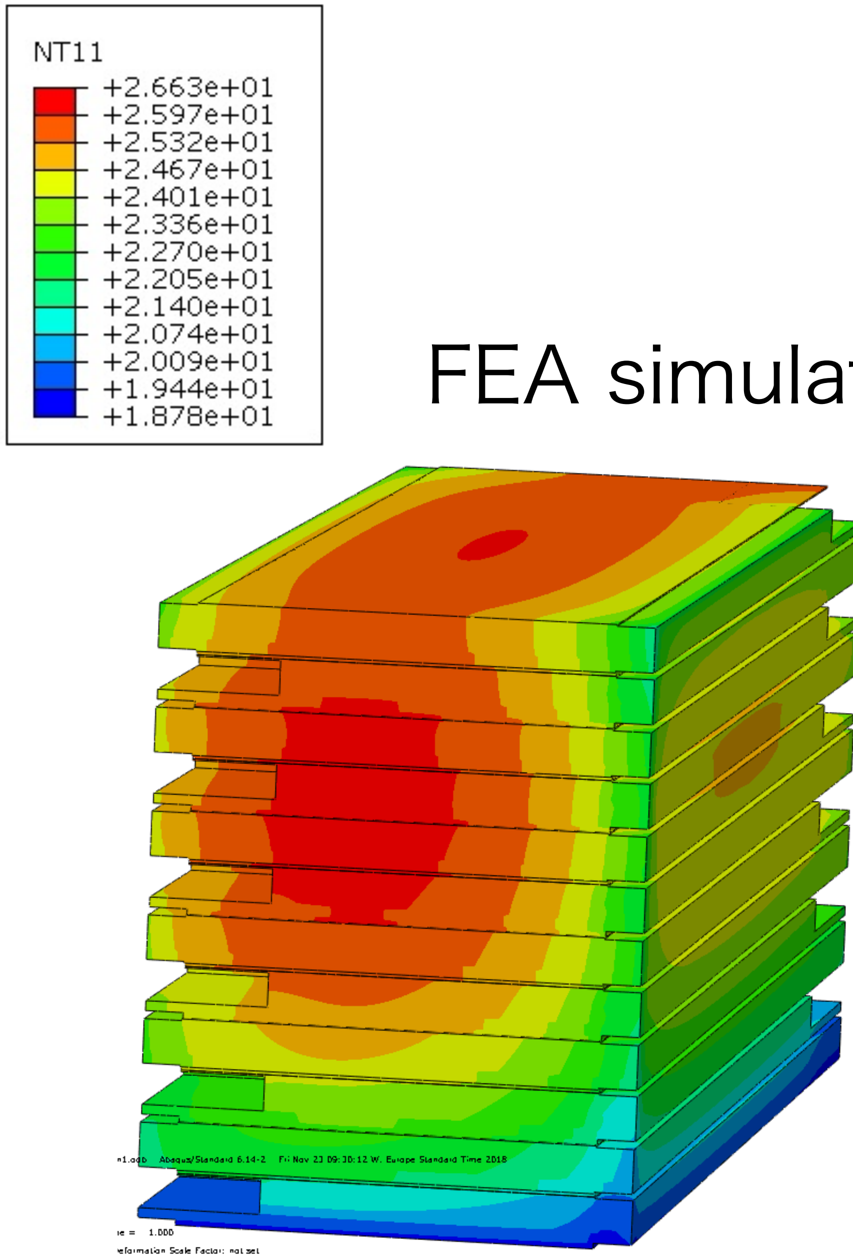
Thermal Measurement



- Cooling and power configuration

Thermal Measurement





FEA simulation

- Temperature of 12 super-modules was measured in the range between 18℃ and 26℃ at full power of the heaters
- Compatible with FEA result

Conclusions

- **The TT-PET scanner**, which aims at the construction of a small TOF-PET scanner, was designed to obtain the ability of **Time-of-Flight (TOF)** and **Depth-of-Interaction (DOI)** measurement and to be insertable existing MRI
- Excellent performance of the TT-PET scanner was expected by Geant4 simulation and image reconstruction
- ASIC Prototype with silicon monolithic pixels was fabricated in **IHP SiGe-HBT technology**
- **More than 99% efficiency** and **110 ps (high power consumption)/130 ps (low power) time resolution** were observed at CERN SPS testbed facility
- Thermal setup was found to be capable dissipating the power produced by the scanner

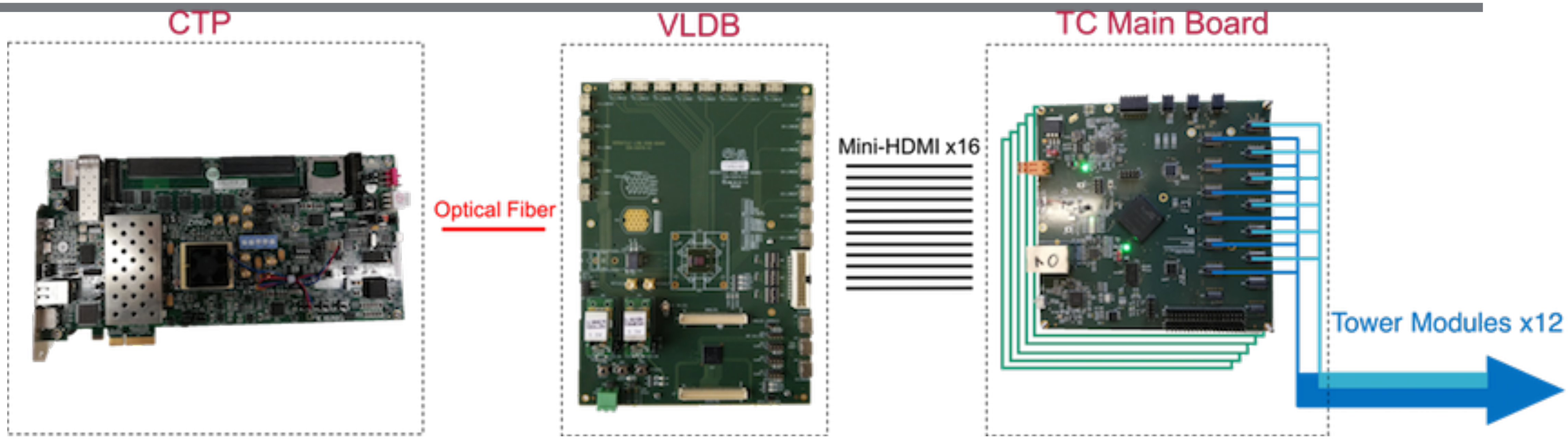
Backups

Collaboration Institutes

- DPNC, University of Geneva
- LHEP, University of Bern
- INFN of Rome Tor Vergata
- IHP Microelectronics
- Hôpitaux Universitaires Genève (HUG)
- CERN
- Stanford University

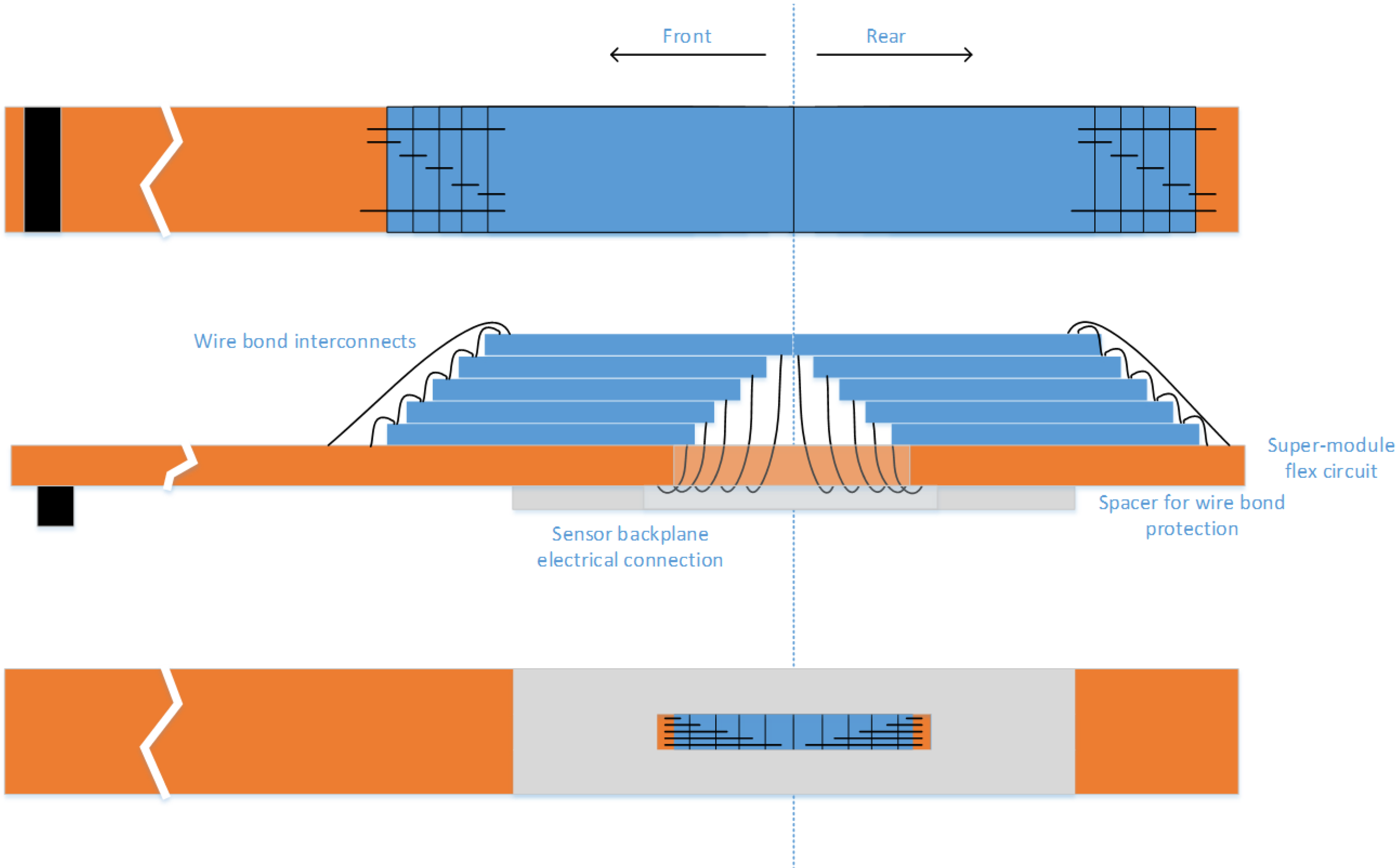
- Supported by Swiss National Science Foundation (SNSF)

Design of the DAQ System

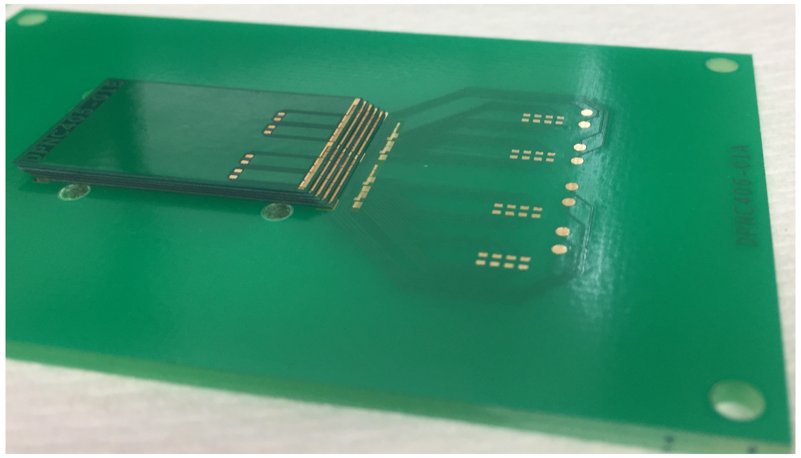


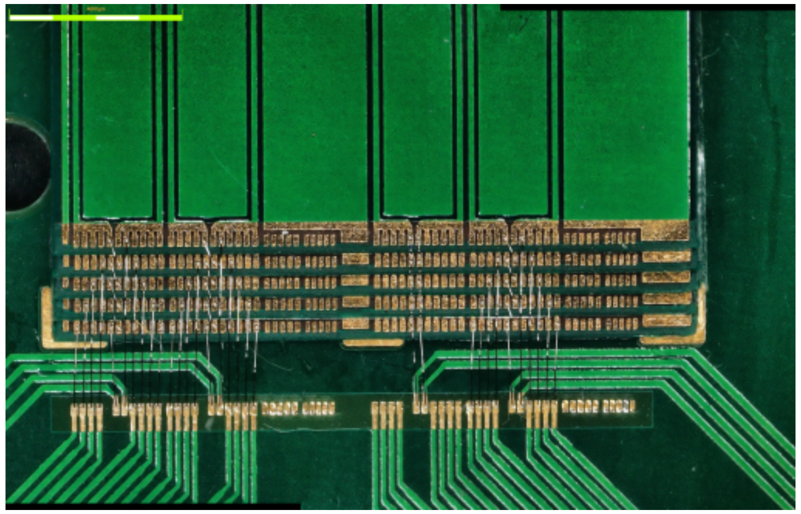
- TC Main boards (x16)
  - Custom FPGA boards
  - HV/LV operation, temporary data storage/suppression, 8b10b encoding, data aggregation
- Versatile Link Demo Board (VLDB)
  - A multiplexer board: multiplex electrical signals from TC boards to a single bitstream
- Central Trigger Processor (CTP)
  - A large powerful commercial FPGA board (Xilinx VC709)
- Designed to work with radioisotope activity up to 50 MBq

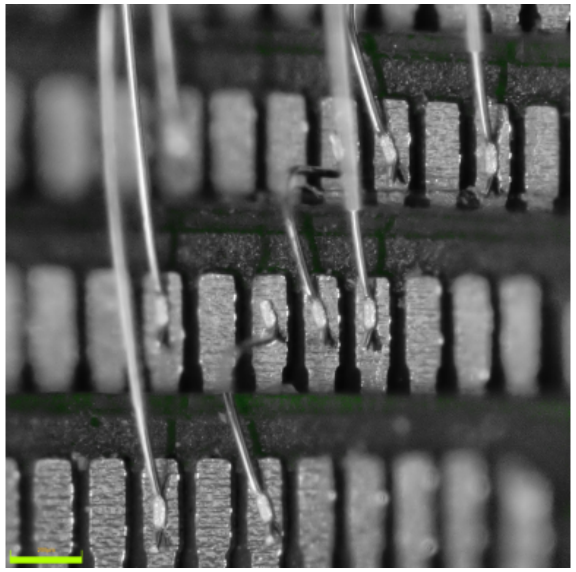
Electrical Interfaces



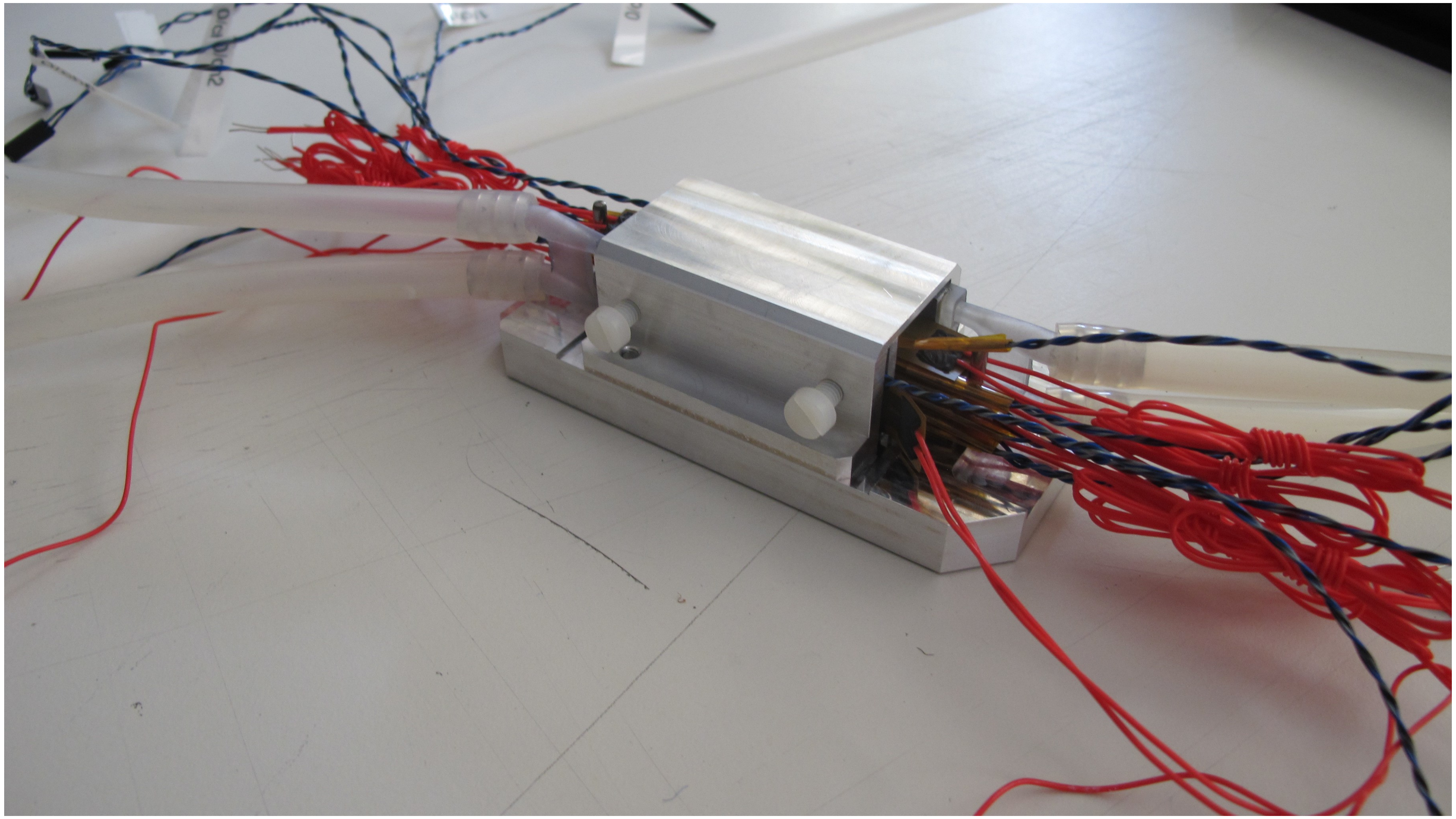
Wire-bonding Test







Thermal mock-up

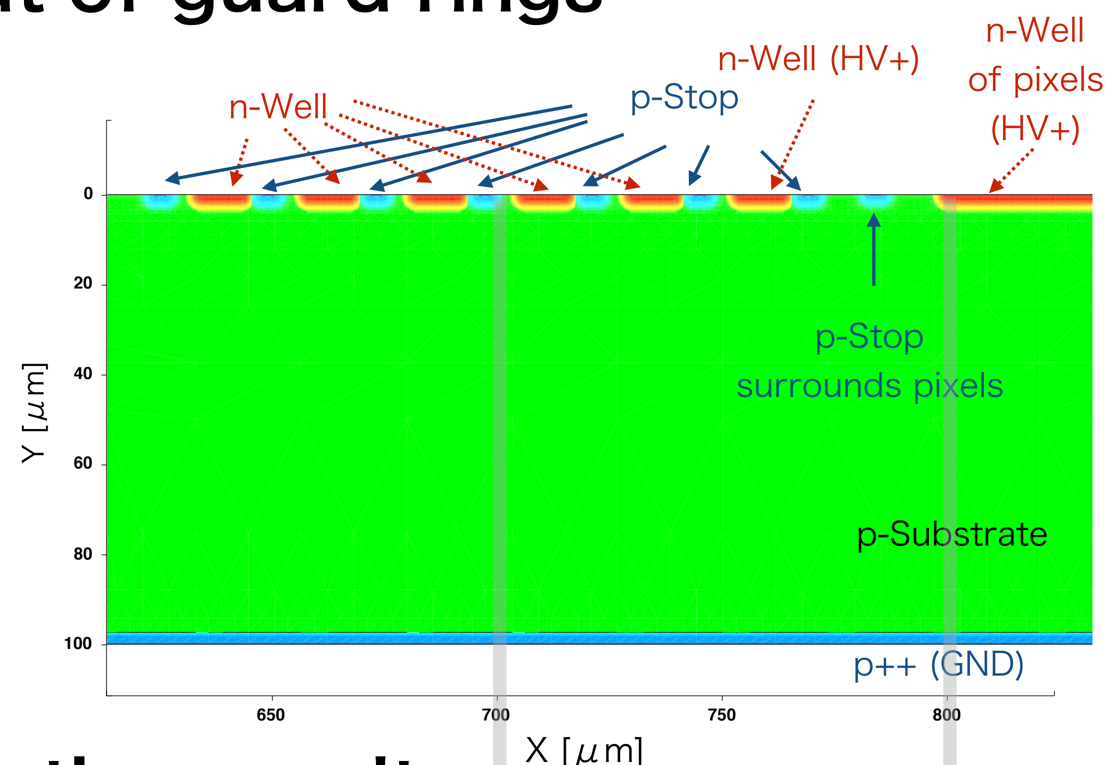


Comparison with FEA

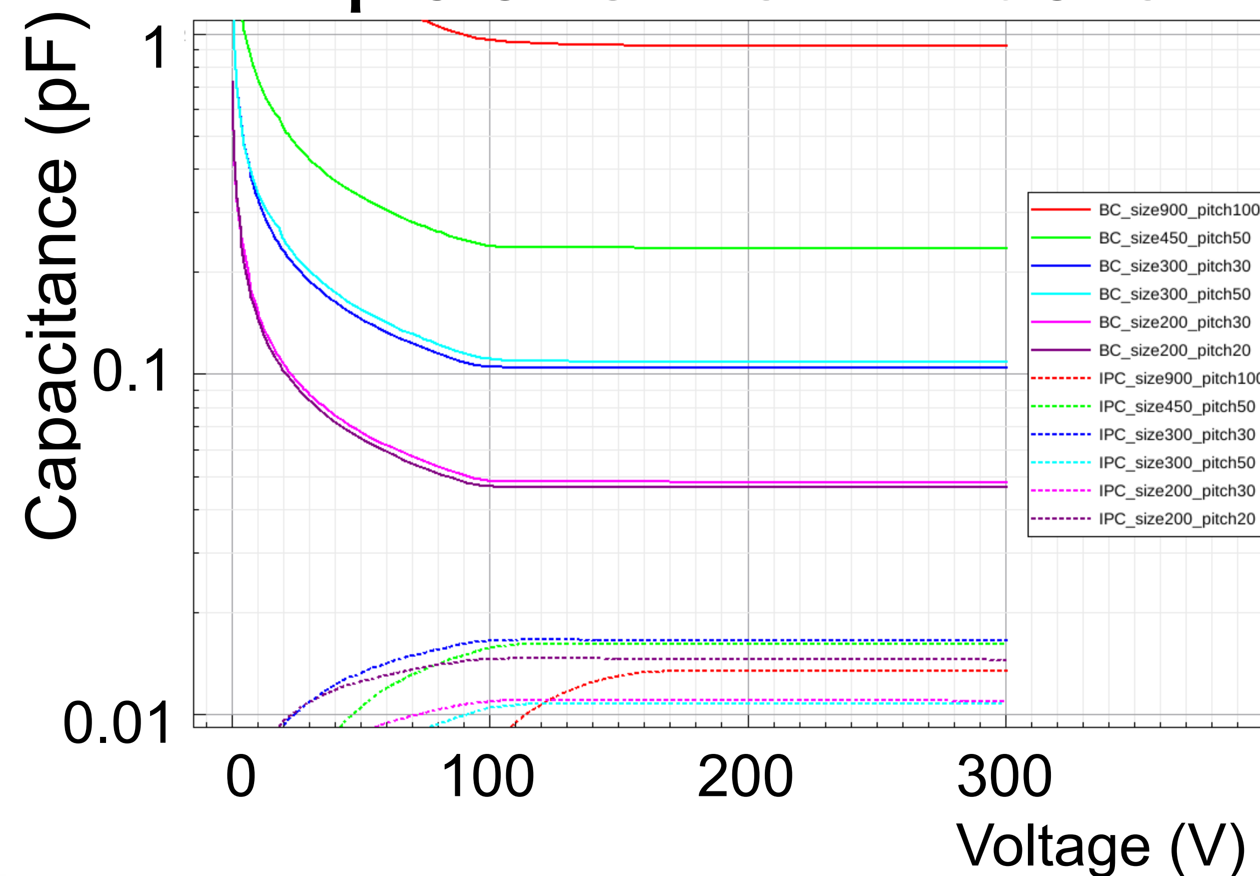
MOD #	Meas. Temp (°C)	FEA results (°C)	Var. %
MOD1	**18.0**	**19.6**	*8*
MOD2	**20.5**	**20.6**	*1*
MOD3	**19.3**	**22.5**	*14*
MOD4	**21.8**	**22.9**	*5*
MOD5	**21.0**	**24.0**	*12*
MOD6	**23.6**	**24.3**	*3*
MOD7	**23.1**	**24.8**	*7*
MOD8	**24.8**	**24.8**	*0*
MOD9	**24.6**	**25.0**	*2*
MOD10	**25.6**	**24.8**	*-3*
MOD11	**24.0**	**25.0**	*4*
MOD12	**26.0**	**24.6**	*-6*

Design/Simulations of the Pixel Sensor

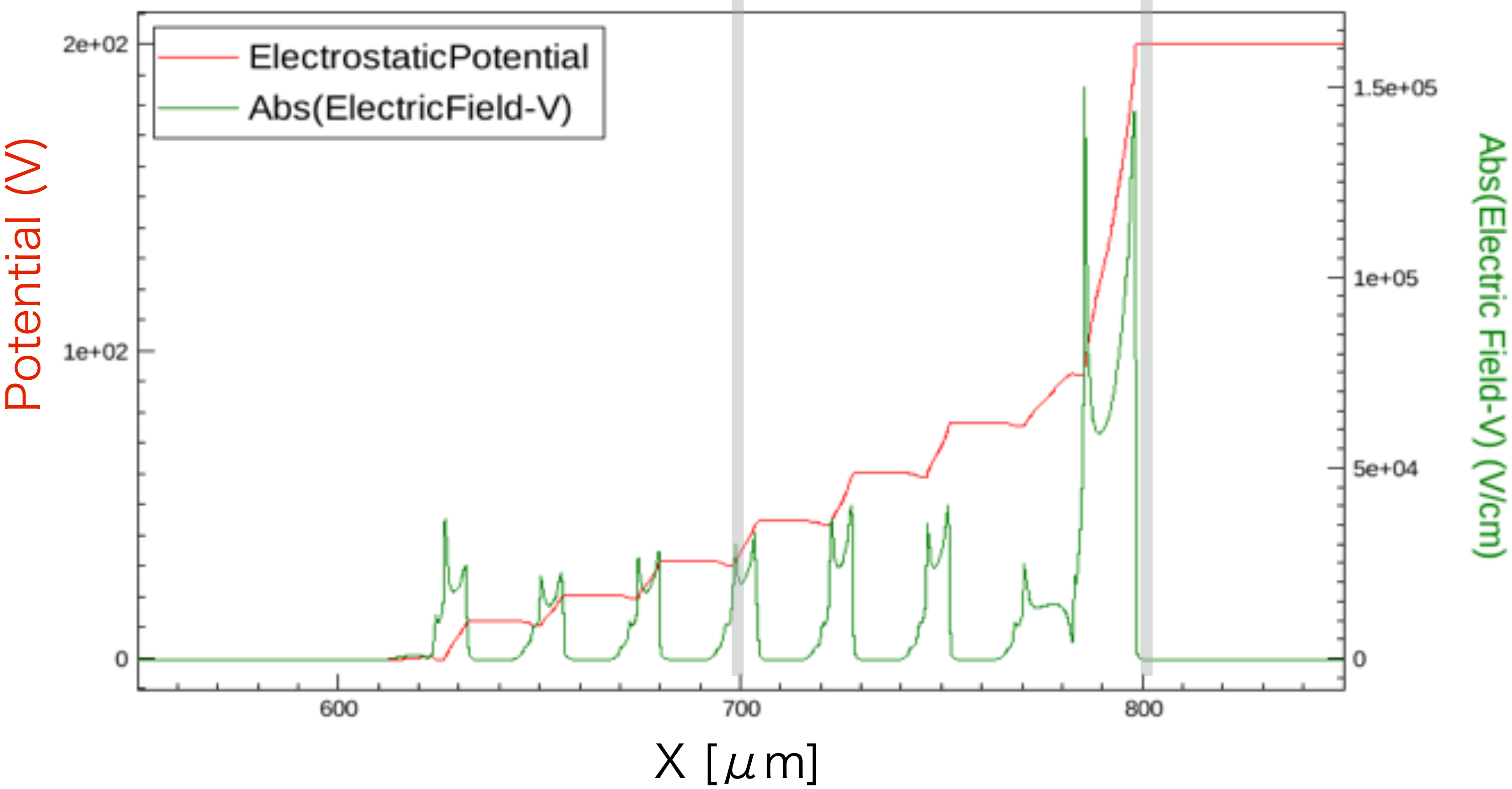
Layout of guard rings



Example of C-V simulations



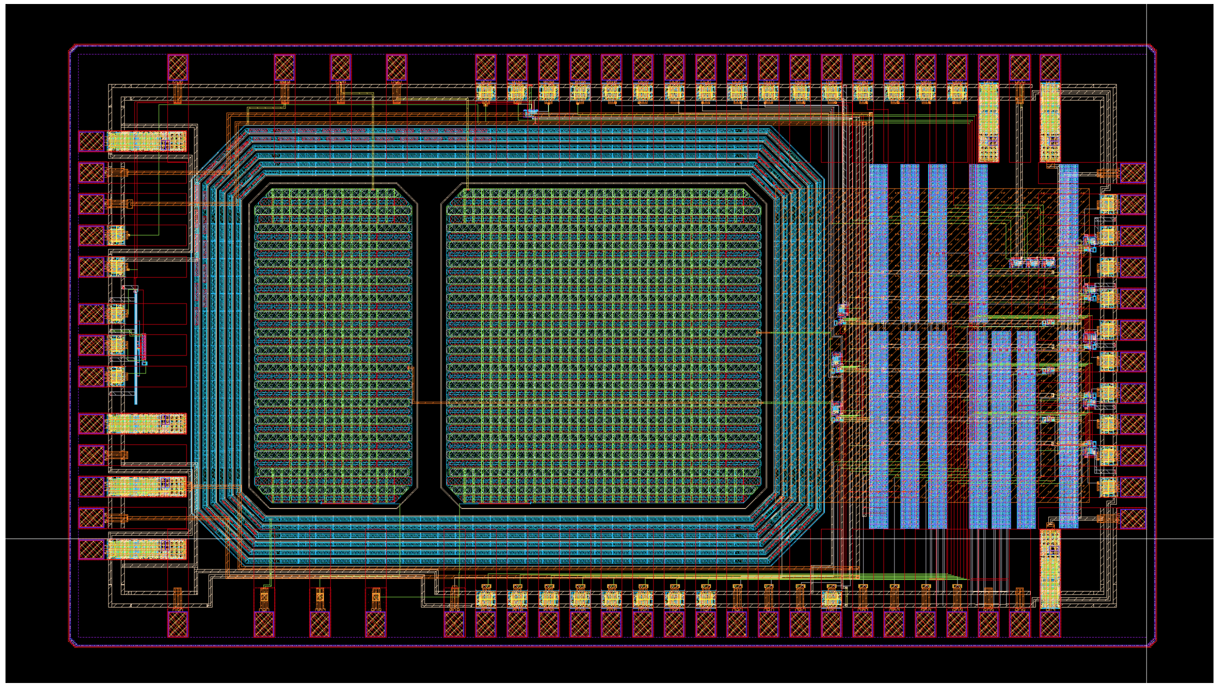
Simulation results



- Technology CAD (TCAD) simulation was performed to design guard rings to avoid high critical electric field (2×10^5 V/cm)
- C-V simulations were performed to estimate total capacitance of the pixel sensors

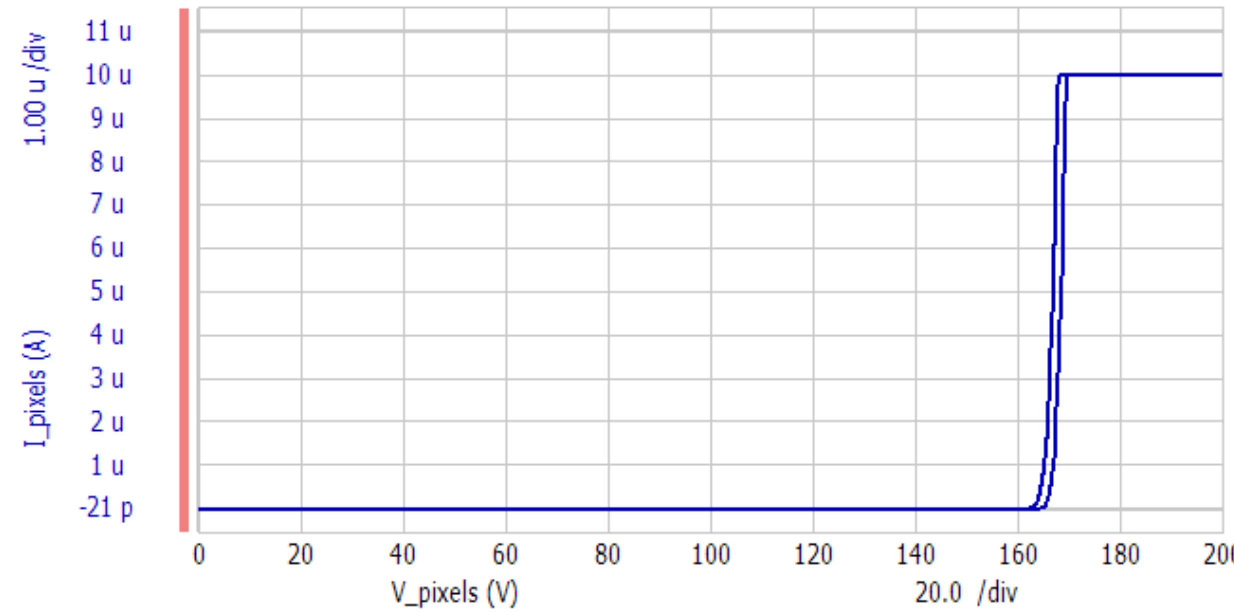
First Prototype

Layout of the first prototype



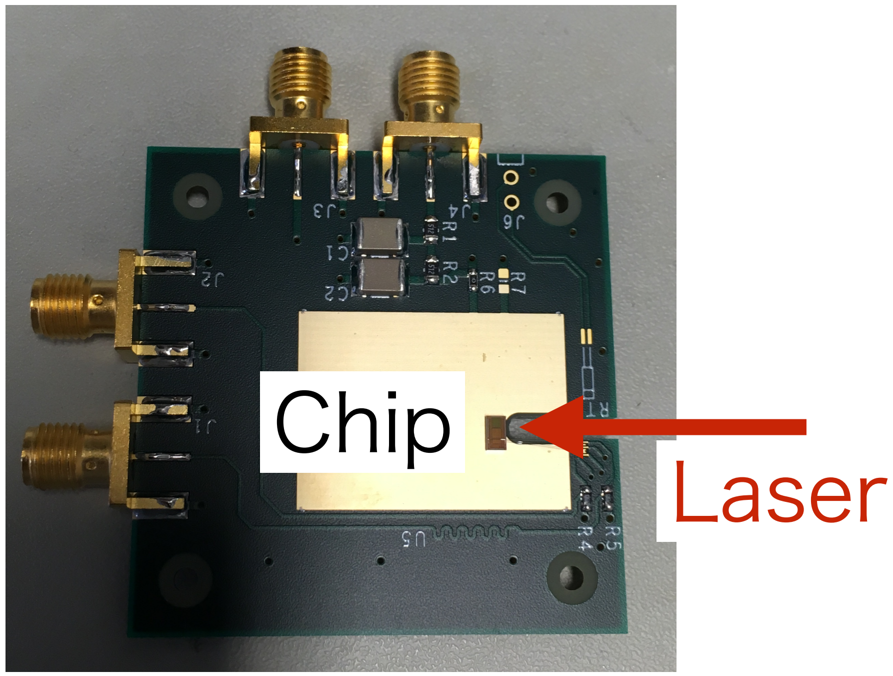
- Two pixels, amplifier, discriminator in 130 nm IHP process
- Pixel size: 900 × 900 μm^2 and 900 × 450 μm^2
- High wafer resistivity
- Un-thinned (700 μm)

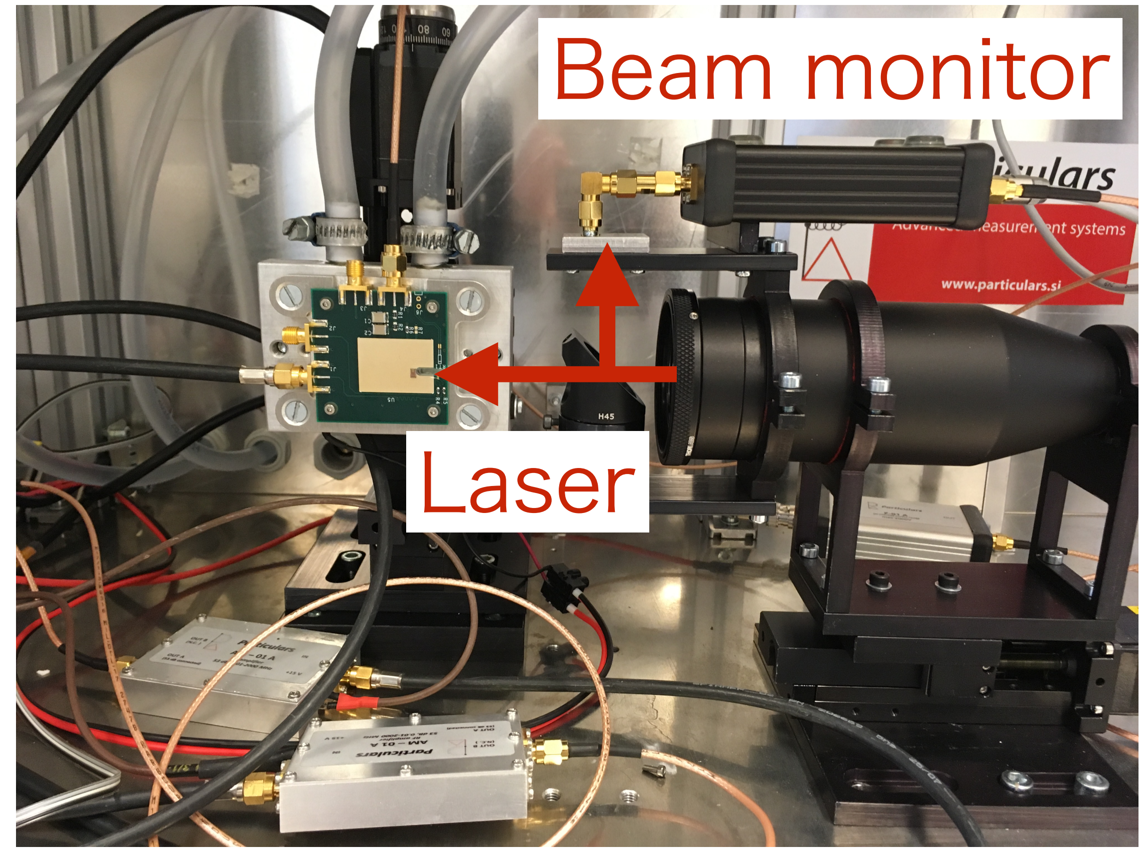
I-V Measurement at DPNC probe station

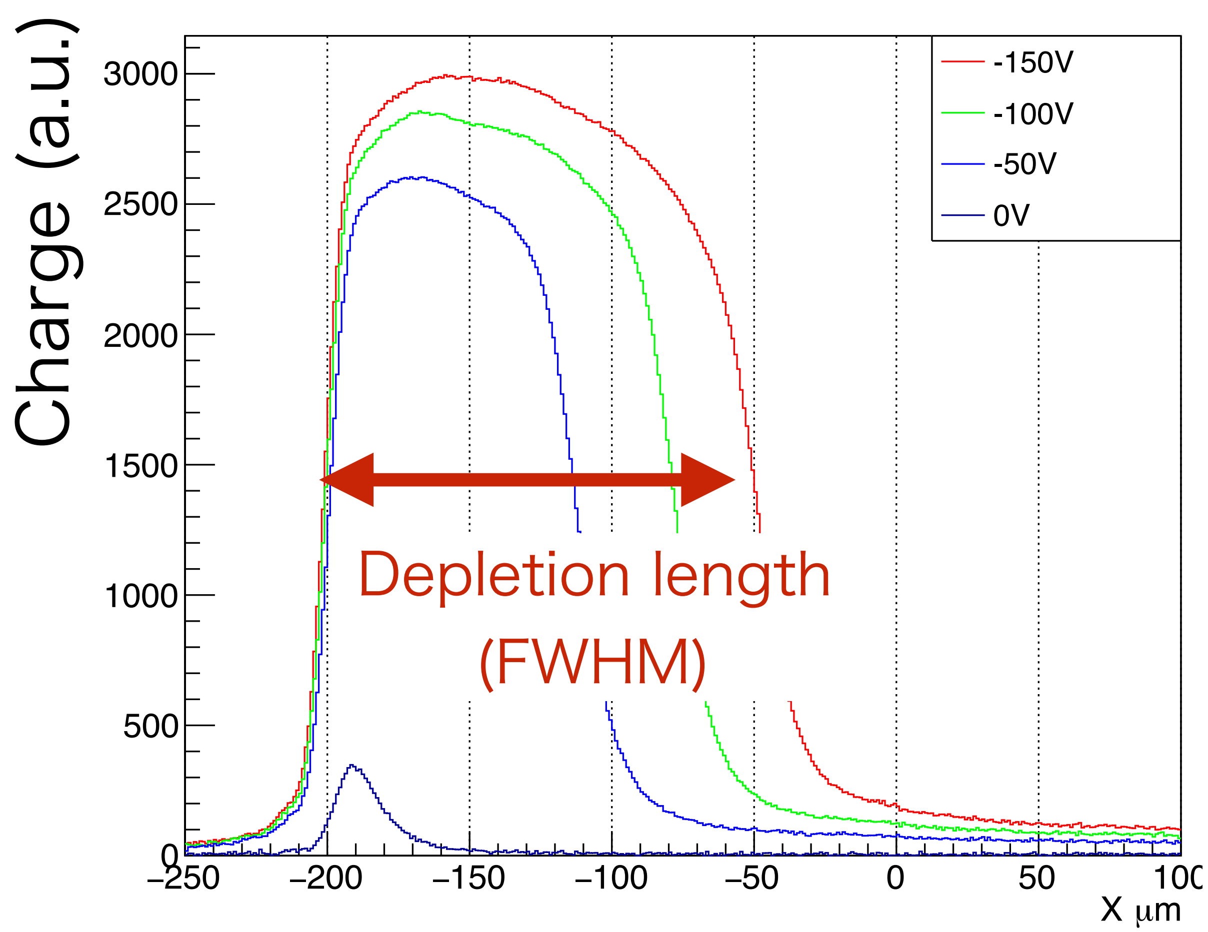


- Shows the correct functionality of the guard ring up to a bias potential of 160 V applied to the pixels

Laser Edge-TCT Measurement



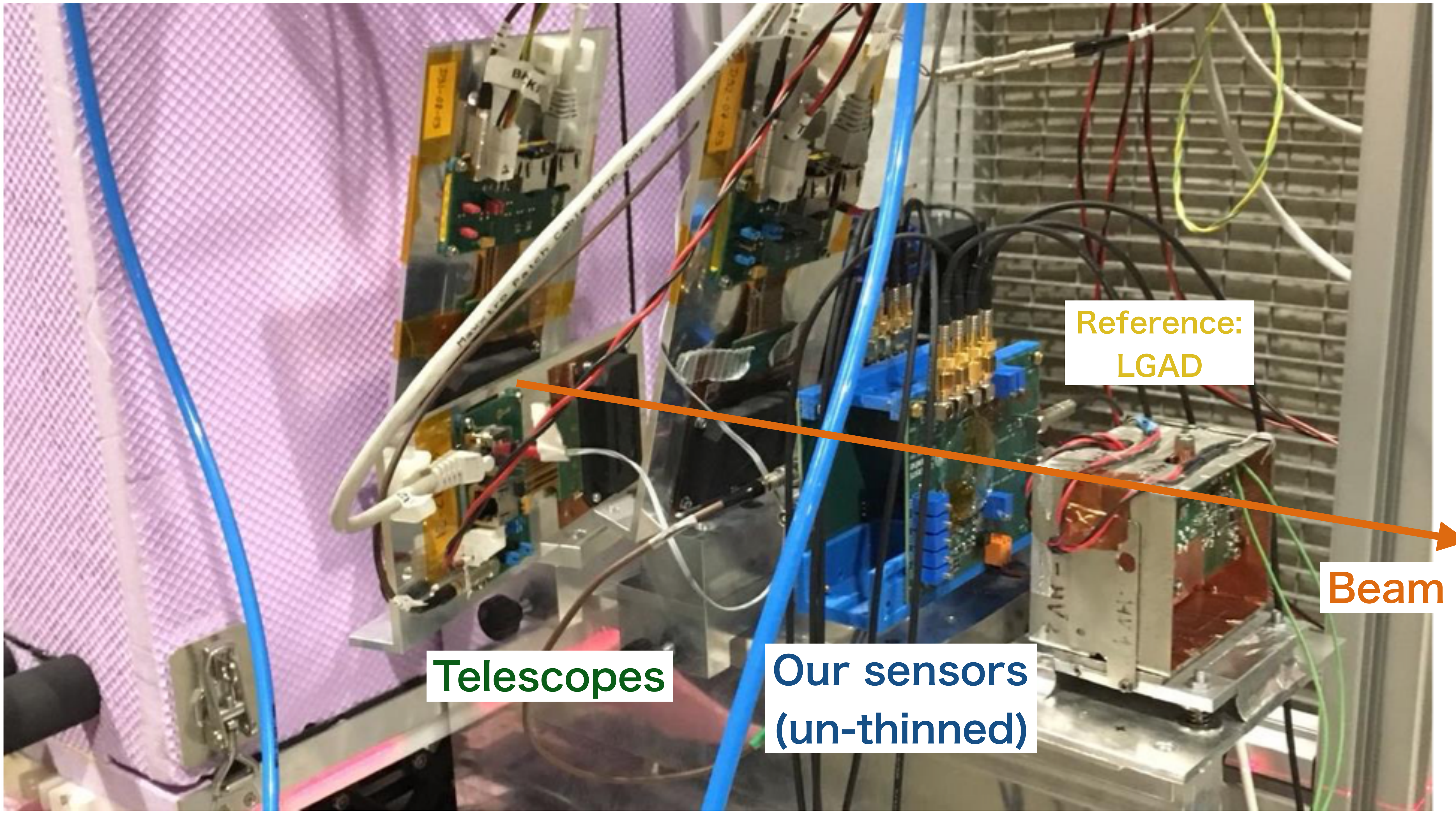




- Laser edge-TCT measurement at DPNC
  - Depletion lengths correspond to <u>1500 Ω*cm resistivity</u>

Testbeam Measurements at CERN SPS

Publication: JINST 13 (2018) P04015



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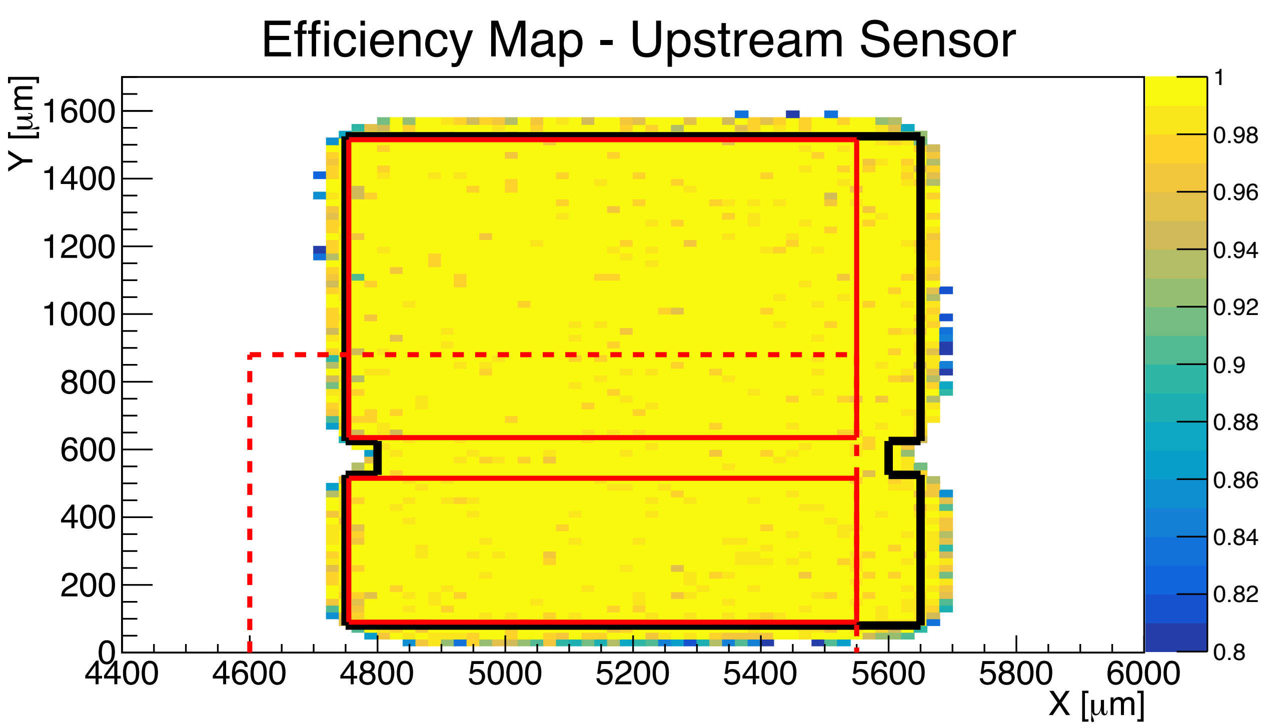

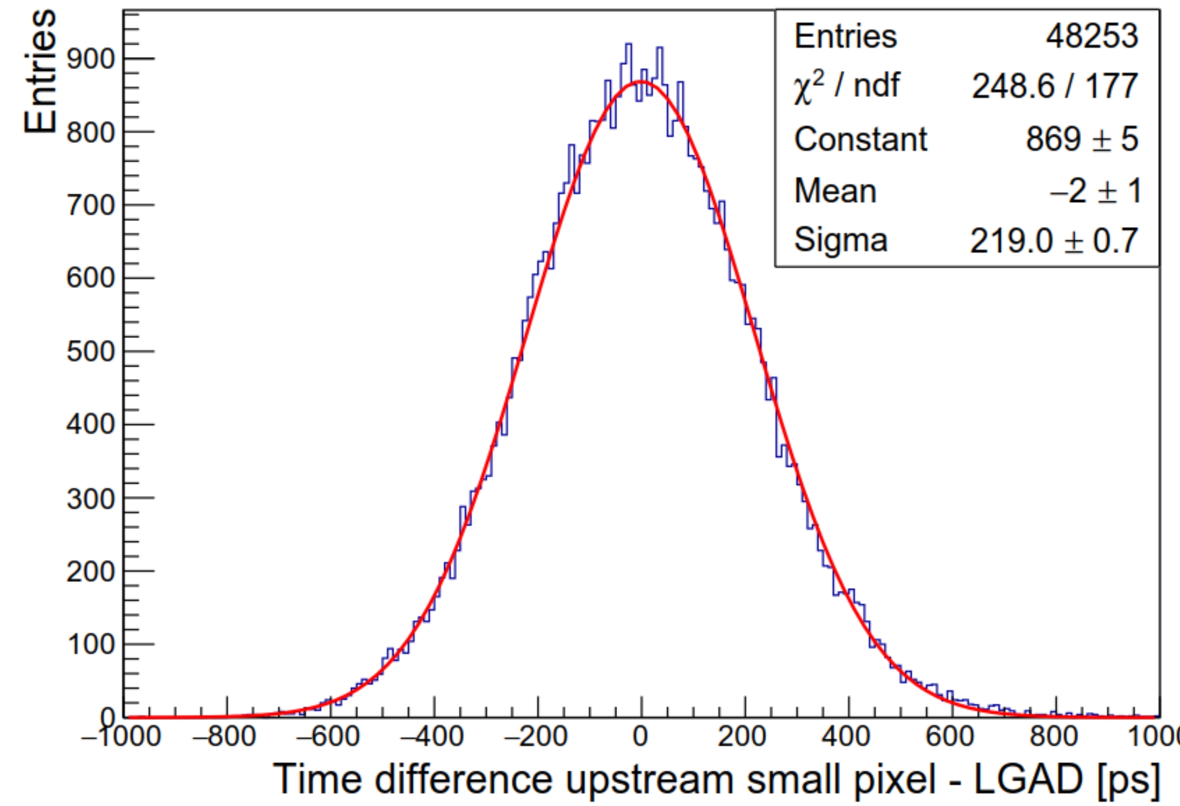

- The detector shows an efficiency **greater than 99.8 %**
- The time resolution for MIPs: **~200 ps** for pixels with 0.8 pF capacitance despite the absence of wafer thinning and backplane metallization (target: 100 ps for MIPs, corresponds to 30 ps for PET)

^{22}Na Setup