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OUTLINE

- Motivation and performance requirements
- Technologies
- Status of the proposal, project structure and engagement



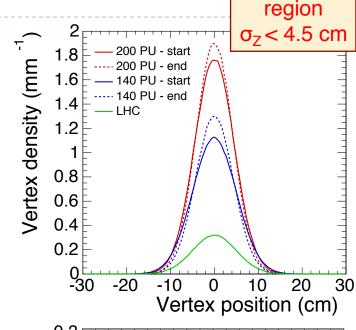
Motivation

HL-LHC: upgrade of LHC and injectors

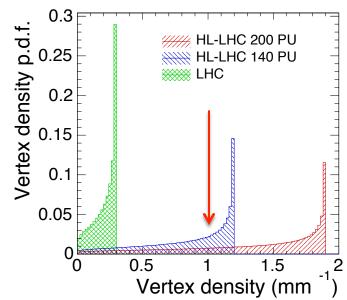
- Baseline:
 - $L_{inst} = 5.0 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1} \text{ (140 pileup)}$
- Ultimate:
 - $L_{inst} = 7.5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1} \text{ (200 pileup)}$
 - Luminosity leveling: trade-off between integrated luminosity (amount of data) and experiment performance

CMS event reconstruction dependent on *track assignment* to vertices

- Substantial pileup contamination at vertex densities > 1 event/mm
- Maintaining 50 PU performance at high pileup benefits the full CMS program at the HL-LHC



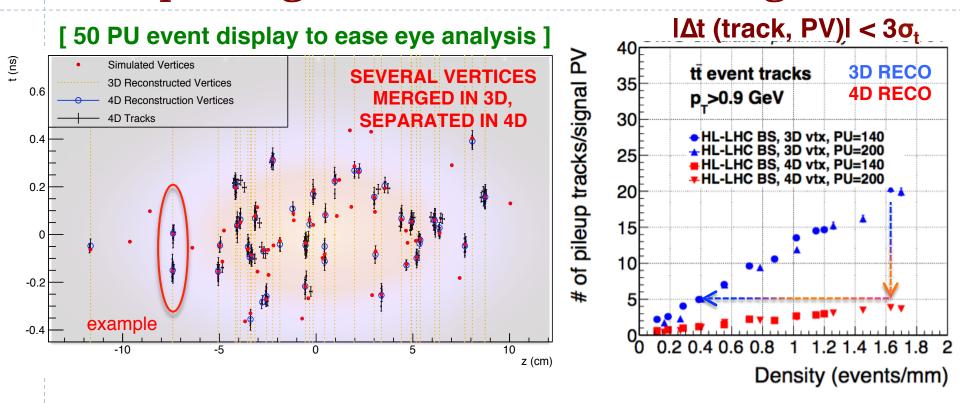
Luminous







Pileup mitigation with track-timing



"Dissect" the luminous region in time

- Space-time vertex reconstruction with 30 ps RMS per-track
- ▶ Beam-spot time spread ~180 ps RMS (constant over the fill)
- ▶ Recover LHC (40 PU) track purity of vertices



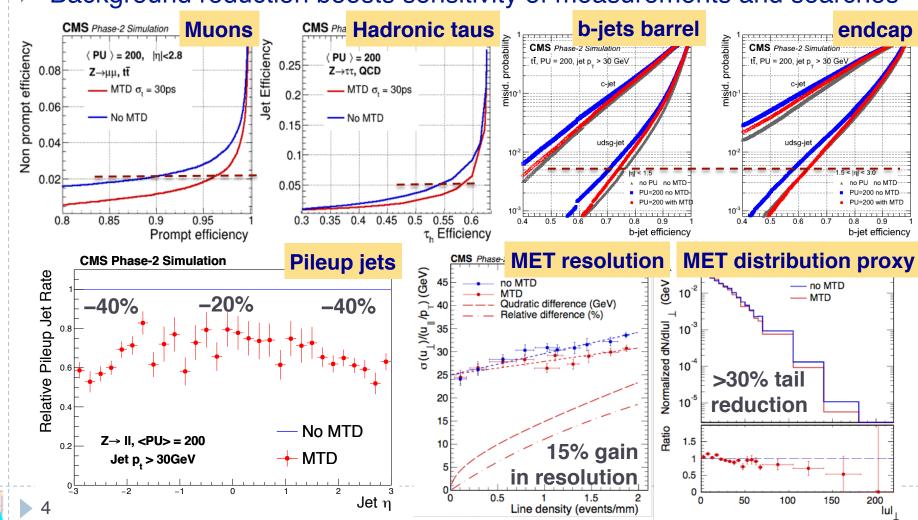




Snapshot of the reconstruction benefits

Performance losses at 200 PU entirely offset with timing

- ▶ Efficiency gains (5–10%) compound in multi-object final states
- Background reduction boosts sensitivity of measurements and searches







Summary of the MTD Technical Proposal (*)

Signal	Physics measurement	MTD Impact
H→γγ H→4leptons	+25% statistical precision on xsecs → Couplings	Isolation Vertex identification
VBF+H→ττ	+30% statistical precision on xsecs → Couplings	Isolation VBF tagging, MET
НН	+20% gain in signal yield → Consolidate searches	Isolation, b-tagging
EWK SUSY	40% reducible background reduction → +150 GeV mass reach	MET
Long Lived Particles (LLP)	Peaking Mass Reconstruction → Unique discovery potential	β _{LLP} from timing of displaced vertices

- There is a <u>beautiful physics case</u> for a <u>hermetic timing</u> <u>detector with 30 ps time resolution</u>
 - Across a wide range of observables and across the HL-LHC program
 - Leveraging gains across the full pseudo-rapidity coverage
- 20-30% increase in effective integrated luminosity





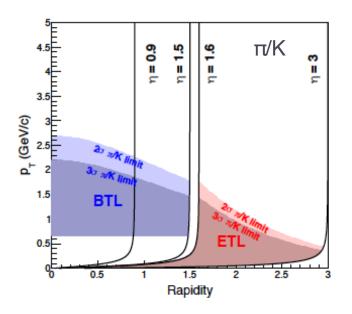
PID with the MTD

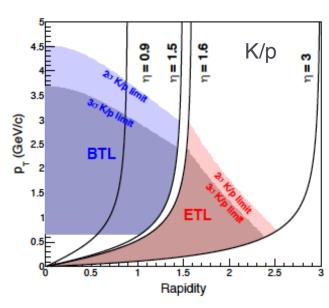
Physics case being extended HI physics in Run-4 (LS3 to LS4)

- The CMS-MTD with 30 ps would almost match ALICE at central rapidities (lyl<0.9) and extend PID coverage to lyl=2.9</p>
- A resolution of 50 ps would still provide acceptance gain and a better separation than the STAR-TOF experiment

▶ The physics case will be included in the TDR

Must achieve 30 ps in (central) BTL in Run4 (limited radiation damage)

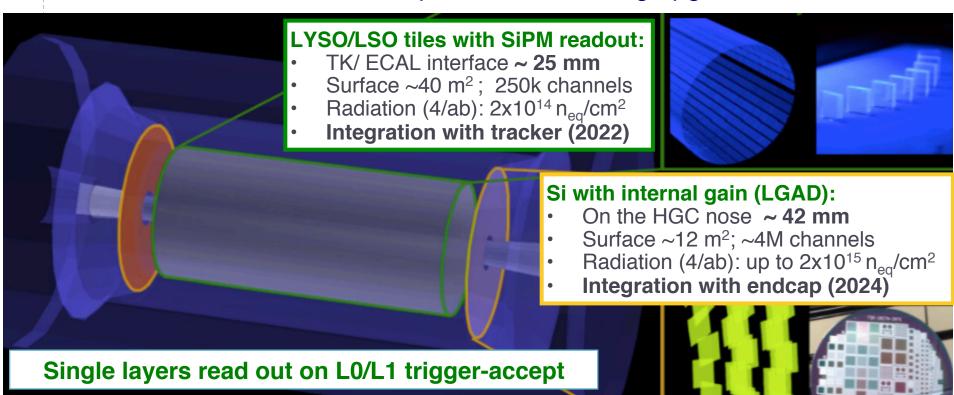






MTD requirements and technology choice

- Hermetic timing detector with 30 ps resolution on charged tracks
- Cost effective design over large area
- Radiation tolerance
- Minimal impact on calorimeter and tracker performance
- Mechanics and service compatible with existing upgrades







Main detector aspects

Barrel timing layer: (BTL)

- Operation at T = -30 °C
 (CO₂ cooling common with TK)
- **LYSO**: 11.5x11.5 mm²
- Custom SiPM: active area < 16 mm²
- ASIC: TOFHIR
 [adapted from TOFPET2]
- LE discrimination with amplitude measurement for time walk correction
- Challenge: SiPM Dark Count Rate and sensor design

Endcap Timing layer (ETL)

- Operation at T = -20 °C
 (CO₂ cooling common with HGC)
- LGAD pad size: 1x3 mm²
- Ganging 3 to 1 at lηl>2.1
- ASIC: Exploit libraries, and expertise from RD53 (65 nm)
- Ongoing design study (preamp + Disc + ToA and TDC)
- Challenge: Scale to large area and readout chip with <30 ps
- ▶ Control cards with power, clock distr., control and data links (IpGBT)
 - Data volume (zero suppression): 1.2 Tb/s BTL + 2.4 Tb/s ETL
- ► Level-1 trigger up-scope option:
 - Exploit data from regions of interest upon L0 from other systems
 - Requires adjustments of the ASIC logic



Clock distribution

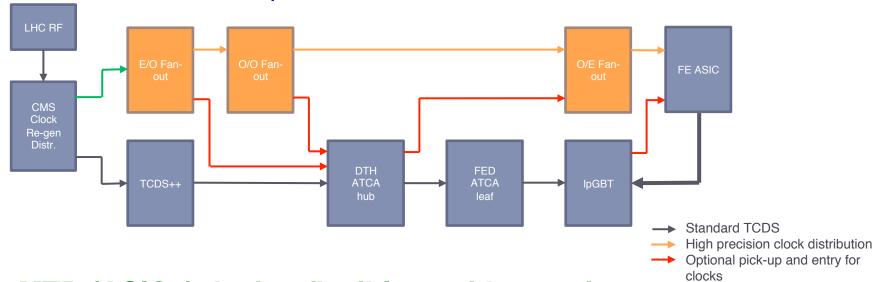
One dedicated clock fibre per readout region

Clock entry local to the lpGBT and front-end ASICs

LHC RF clock distributed via the back-end

Two parallel approaches (CMS wide effort)

- Option 1: Exploit the clock encoded within the control links (IpGBT)
- Option 2: Deploy a separate clock path with dedicated fan-out chip under specification



MTD (ASICs) design flexible to either option





Project status

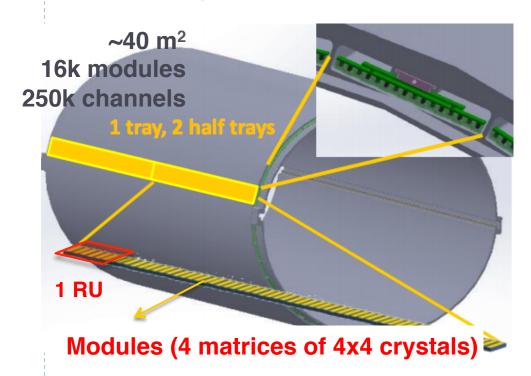
- ► Technical proposal submitted Nov. 2017:
 - LHCC March 1: recommendation to proceed to a TDR (endorsed by CERN RB March 7, 2018)
- ► Technical design report in preparation (Feb 2019)
 - Completion of R&D on sensors and layout optimization
 - Definition of the construction model, quality assurance and check
 - Capitalize on existing projects for power systems, back-end and DAQ
 - Engagement and commitments for construction being defined
 - - >> Mechanical structures <<
- Integration schedule (+ 6 moths on BTL)
 - ▶ Barrel: Integrates with the Tracker → Must be completed by Oct 2023
 - ► Endcap: Integrates with HGCal → Must be completed by Dec 2024

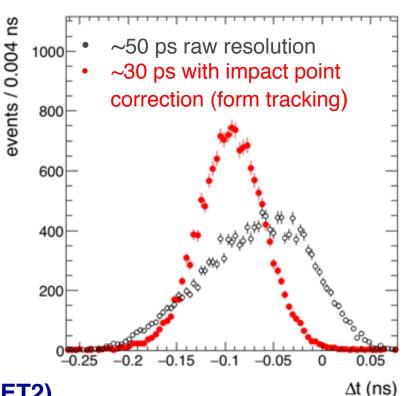




BTL layout

- LYSO/LSO:Ce + SiPMs embedded in the tracker support tube
 - ▶ CO_2 cooling at ~ -30 $^{\circ}C$ (limit SiPMs self-heating and dark rate)
 - Nominal geometry: 11.5x11.5x4 mm³ tile with central SiPM 4x4 mm²





• Read out TOFHIR chip (adapted from TOFPET2)
Leading edge timing + amplitude meas.

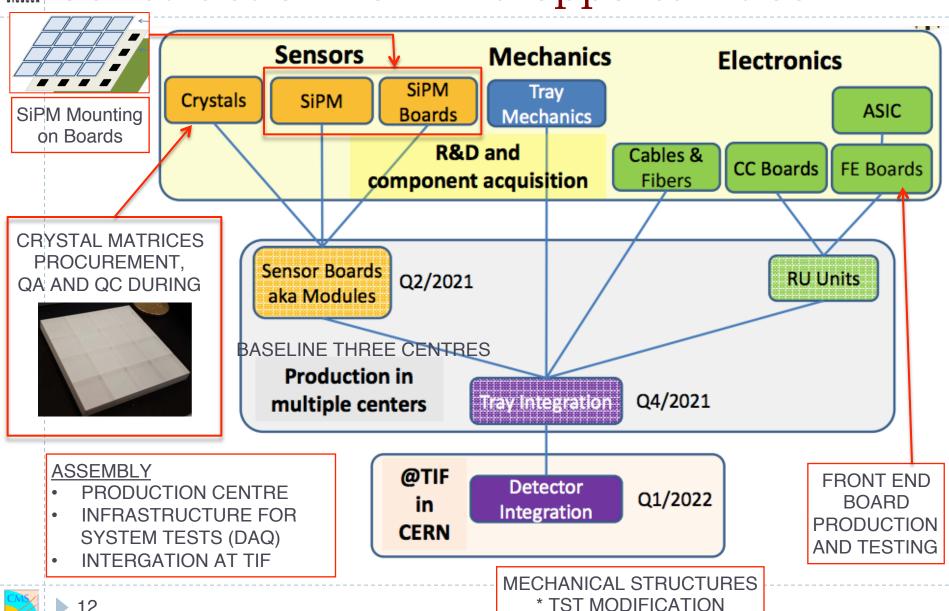
R&D ongoing to mitigate the need to rely on tracking







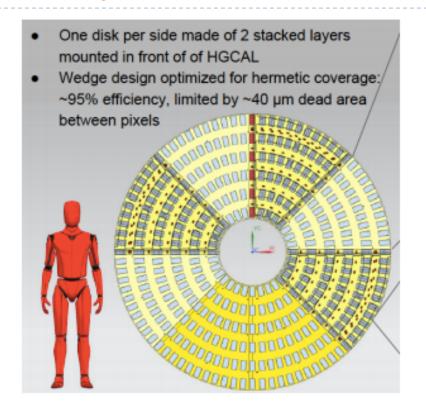
Construction flow and opportunities

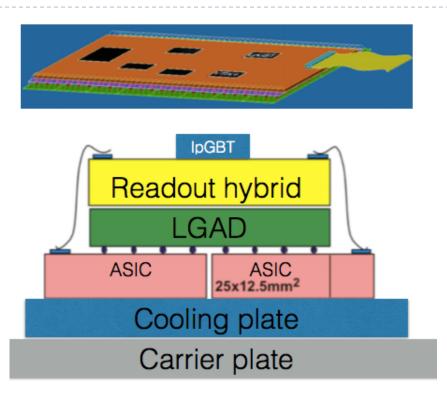






ETL layout





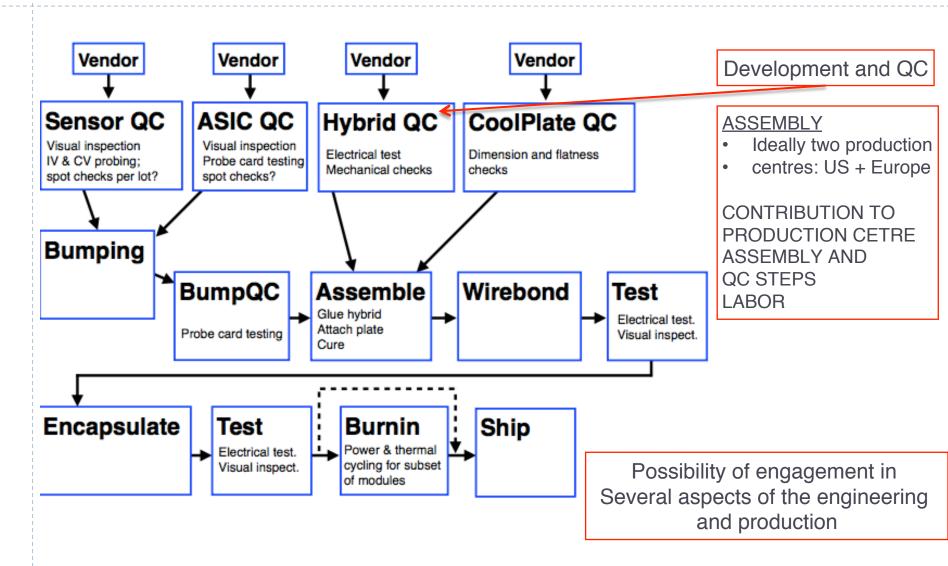
Low gain avalanche diodes (LGADs) mounted on the HGCal nose

- LGAD qualified in beams at irradiation levels needed for HL-LHC
- Nominal geometry: 4.8 x 9.6 cm² modules with 1x3 mm² pads
- ASIC: Preamp + Time-pick-off and TDC similar to ALTIROC1 (ATLAS) but in 65 nm





Construction flow and opportunities







Summary

▶ A TP was approved

- The MTD can provide substantial performance gain at HL-LHC
- Expression of interests from 34 institutions were collected

A TDR is being prepared

- Commitments are being defined and there is plenty of opportunities to engage in
 - finalizing the detector design
 - contributing to the construction and validation process in both technologies (more in ETL than BTL)
 - design and commissioning of the mechanical infrastructure, the power system (BTL and ETL) and the DAQ

