ADC option – TI ADS54J60

- 16-bit 1GSPS ADC
- 70dBFS SNR (11.3 ENOB)
- 2 channels with 2/4 lanes per channel

lanes/ch	ch/FMC	line rate	samp rate
2	4 (5)	10G / 6.5G	1G / 650M
4	2	5G	1G

TEXAS INSTRUMENTS
ADS54J60
SBAS706C – APRIL 2015 – REVISED JANUARY 2017

ADS54J60 Dual-Channel, 16-Bit, 1.0-GSPS Analog-to-Digital Converter

1 Features

- 16-Bit Resolution, Dual-Channel, 1-GSPS ADC
- Noise Floor: –159 dBFS/Hz
- Spectral Performance (f_{IN} = 170 MHz at –1 dBFS):
  - SNR: 70 dBFS
  - NSD: –157 dBFS/Hz
  - SFDR: 86 dBc (Including Interleaving Tones)
  - SFDR: 89 dBc (Except HD2, HD3, and Interleaving Tones)
- Spectral Performance (f_{IN} = 350 MHz at –1 dBFS):
  - SNR: 67.5 dBFS
  - NSD: –154.5 dBFS/Hz
  - SFDR: 75 dBc
  - SFDR: 85 dBc (Except HD2, HD3, and Interleaving Tones)
- Channel Isolation: 100 dBc at f_{IN} = 170 MHz
- Input Full-Scale: 1.9 V_{PP}
- Input Bandwidth (3 dB): 1.2 GHz
- On-Chip Dither
- Integrated Wideband DDC Block
- JESD204B Interface with Subclass 1 Support:
  - 2 Lanes per ADC at 10.0 Gbps
  - 4 Lanes per ADC at 5.0 Gbps
  - Support for Multi-Chip Synchronization
- Power Dissipation: 1.35 W/Ch at 1 GSPS
- Package: 72-Pin VQFNP (10 mm × 10 mm)

2 Applications

- Radar and Antenna Arrays
- Broadband Wireless
- Cable CMTS, DOCSIS 3.1 Receivers
- Communications Test Equipment
- Microwave Receivers
- Software Defined Radio (SDR)
- Digitizers
- Medical Imaging and Diagnostics

3 Description

The ADS54J60 is a low-power, wide-bandwidth, 16-bit, 1.0-GSPS, dual-channel, analog-to-digital converter (ADC). Designed for high signal-to-noise ratio (SNR), the device delivers a noise floor of –159 dBFS/Hz for applications aiming for highest dynamic range over a wide instantaneous bandwidth. The device supports the JESD204B serial interface with data rates up to 10 Gbps, supporting two or four lanes per ADC. The buffered analog input provides uniform input impedance across a wide frequency range while minimizing sample-and-hold glitch energy. Each ADC channel optionally can be connected to a wideband digital down-converter (DDC) block. The ADS54J60 provides excellent spurious-free dynamic range (SFDR) over a large input frequency range with very low power consumption.

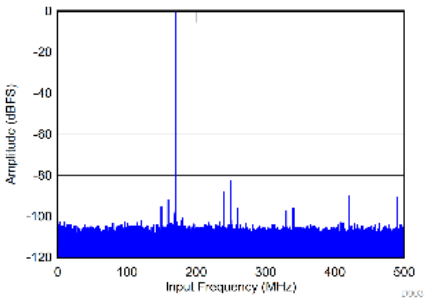
The JESD204B interface reduces the number of interface lines, allowing high system integration density. An internal phase-locked loop (PLL) multiplies the ADC sampling clock to derive the bit clock that is used to serialize the 16-bit data from each channel.

Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ADS54J60	VQFNP (72)	10.00 mm × 10.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

FFT for 170 MHz Input Signal (SNR = 69.8 dBFS; SFDR = 88 dBc; IL Spur = 86 dBc; Non HD2, HD3 Spur = 89 dBc)



Commercial FMCs

Commercial FMCs are all 4 channel so limited to 650M on VFC

- Vadatech FMC231 ($5578 / 14wks)
  - transformer coupled (0.4MHz)
- Hitech HTG-ADC16
  - transformer coupled
- Abaco FMC120
  - DC coupled (?)