Monolithic Active Pixel Detectors: Test beam results from the sPHENIX vertex detector

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Introduction

The successor to the PHENIX experiment, sPHENIX, is currently being designed and constructed as an advanced technology particle detector for use at RHIC and expected to begin data taking in 2023 [1].

The Monolithic-Active Pixel Vertex Detector (MVTX) will be sPHENIX's inner most tracking detector. The goal of the experiment is to measure QGP properties via precision measurements of heavy flavor jets and particles, specifically those involving *b*-quarks. As particles containing *b*-quarks have a mean decay length of less than 1 cm, the MVTX must sit as close to the center of the beam as possible to allow for precision vertex measurements.

The MVTX project share technology from both the ALICE and ATLAS LSII upgrade projects at the LHC and is now entering the production phase. The results of test beam data taken at the Fermilab Test Beam Facility has and is being used to refine the operating parameters of the detector and provide better understanding of it's design to allow for Day One physics data.

Pixel Design

The MVTX uses the ALICE ALPIDE ASIC which consists of 180 nm CMOS technology within a 50μm thick monolithic active pixel sensor [2]. The pixels have a pitch of 27x29μm^2 and are mounted on hybrid integrated circuits (HICs) with 9 ASICS/HIC. The HICs are water cooled and mounted onto a carbon support structure to created a single operating stave, With 48 staves total and each ASIC containing a 512x1024 pixel matrix, this results in over 2.25x10^8 active pixels covering an area of 1780cm^2.

The pixel architecture can be split in to three sections; an analogue front-end comparator with fast charge collection, an analogue pulse shaper with a few microsecond pulse length and a digital AND logic circuit to match the pixel signal with the trigger. Each pixel has a multi-event buffer which can store up to three hits.

The hit pixels are read out in double-columns via the Priority Encoder which cycles over each hit pixel and transfers its address to the Data Transmission Unit on the periphery to be transferred to the front-end readout electronics, the Readout Unit.

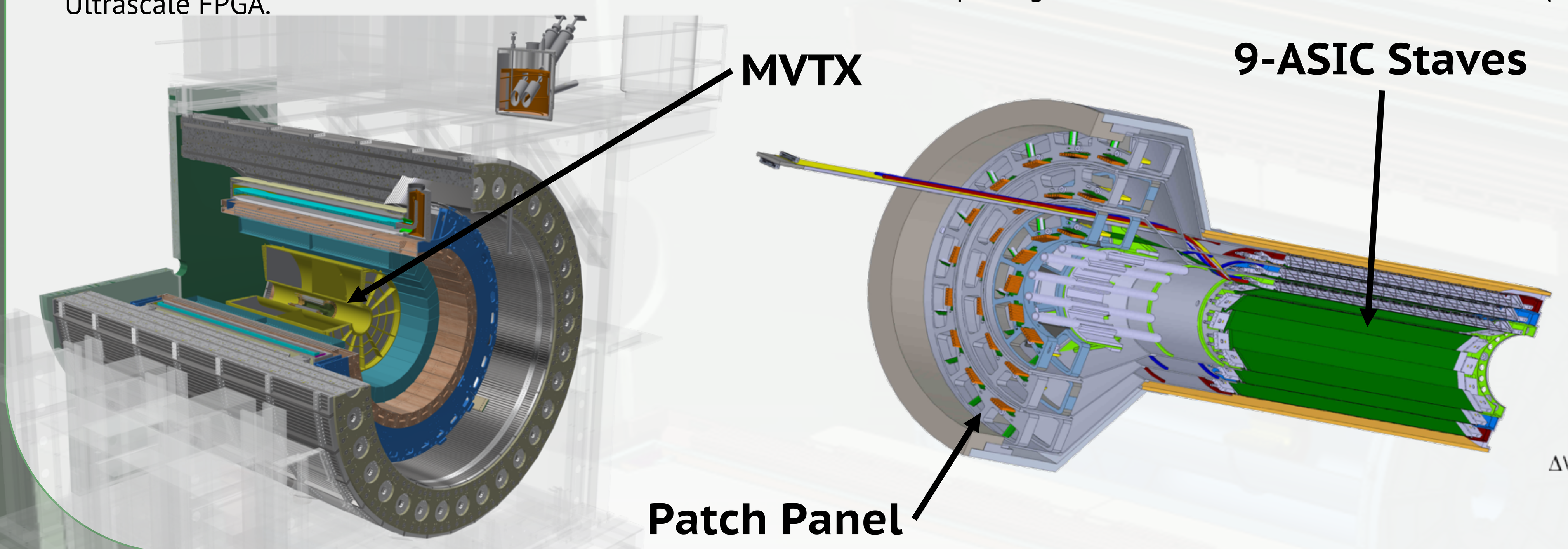
Readout Electronics

The data from each stave is transmitted across more than 10m of differential lines to an off-detector Readout Unit (RU) [3]. It is the RU which is responsible for the transmission of the slow controls, clock distribution, trigger and packaging of the data for optical transmission to the counting house.

The communication between the RU and the counting house is achieved via the GBT protocol and 3 GBTx chips on the RU with the opto-electrical transitions performed by one VTTx and two VTRx's. The data from the ALPIDEs is collected on a main Kintex Ultrascale FPGA.

As the RU's operate in a radiation environment, the system is protected from single-event-upsets using triple modular redundancy and a radiation hard ASIC capable of reprogramming the main FPGA.

The backend electronics uses the Front-End Link Exchange (FELIX) board which will receive data from 24 optical links [4]. As each FPGA has three downlinks, then each FELIX can receive data from 8 RUs or 72 ALPIDE sensors. The FELIX decodes the data and packages it into the PHENIX Raw Data Format (PRDF).

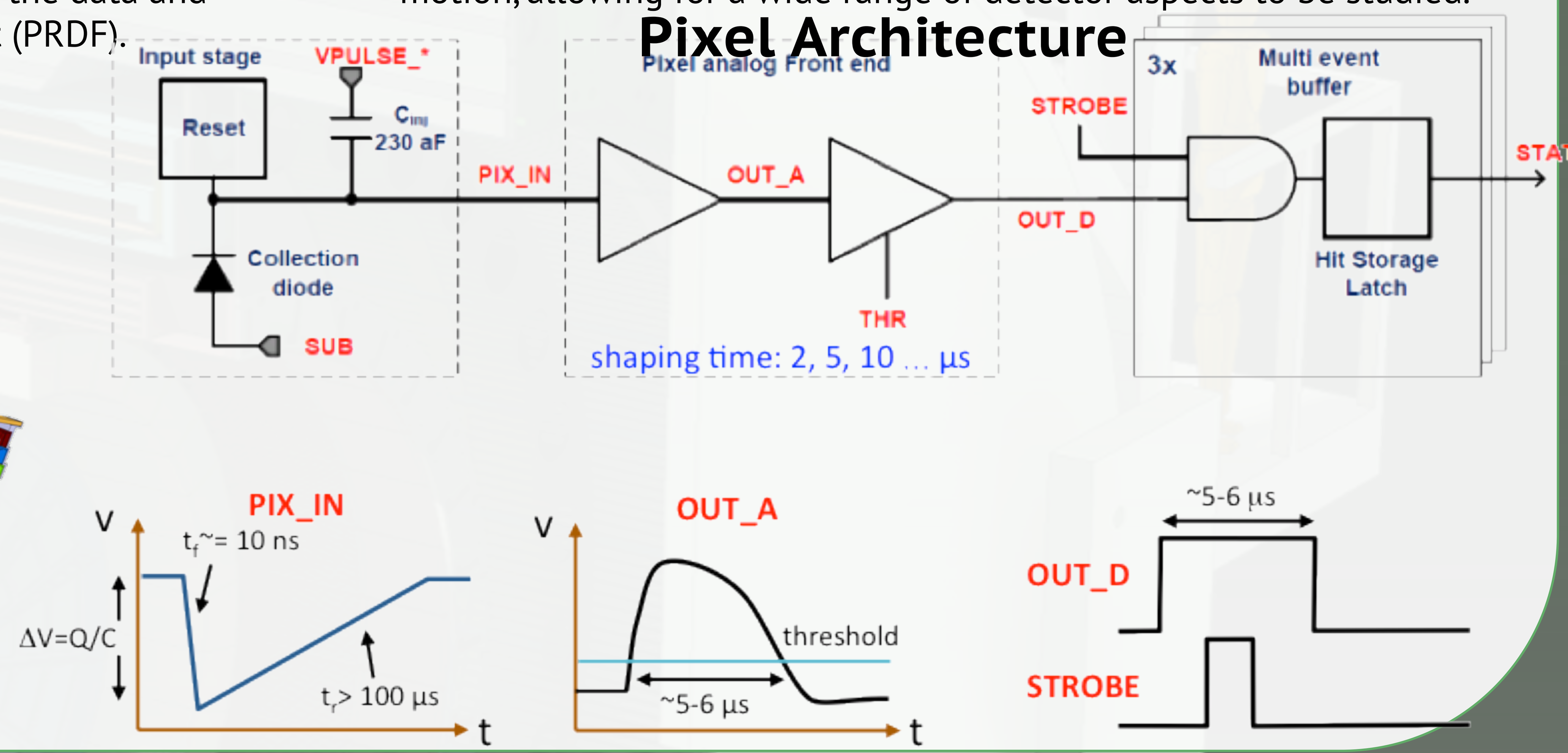


Fermilab Test Beam Facility

The FTBF located at Fermilab, Illinois, USA, is capable of producing 4s long packets of single particles of varying rate and species. The rate can approach 300 kHz which is significantly higher than the sPHENIX trigger rate of 15 kHz while the user can choose between different particle species. The MVTX group used both 120 GeV protons (γ = 130) and 5 GeV electrons (γ = 10000).

The test facility is capable of horizontal, vertical and rotational motion, allowing for a wide range of detector aspects to be studied.

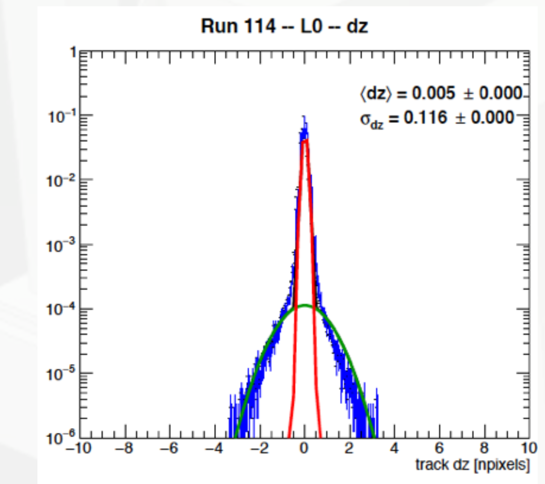
Pixel Architecture



Test Beam Results

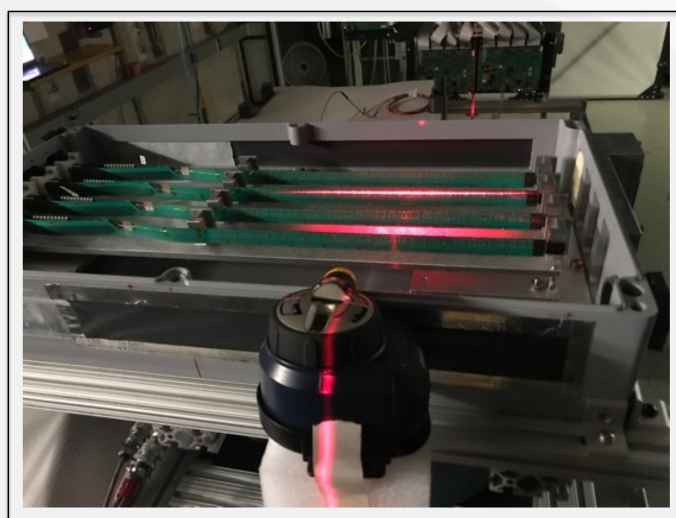
Two test beams were conducted between 2018 and 2019, testing multiple aspects of the detector and readout. The first beam test was performed using prototype devices and four single ALPIDE sensors while the latter test beam used electronically final readout electronics with four complete staves.

The purpose of the initial test beam was to characterize the performance of the ALPIDE chips. Studies from the test beam show that the chip is capable of a hit resolution of approximately 6 μm which is far below the upper resolution limit of 50 μm.

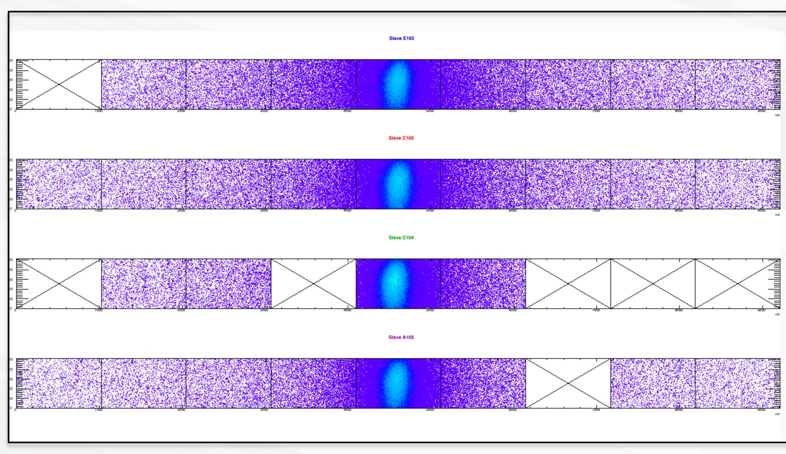


Fit to the cumulative track positions in the ALPIDE chip. The Gaussian resolution is quoted in units of pixels and was measured to be better than 6 μm.

By using full staves in the second test beam, it was possible to characterise more properties of the detector such as the angular dependence of cluster sizes and the true material budget of each stave which is predicted to be 0.3X$_0$%.

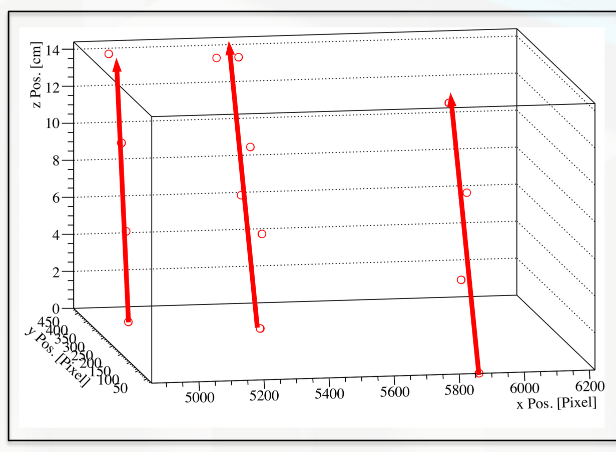


Four staves in the telescope box at the FBTF. The staves are illuminated by a wide laser beam to ensure the readout chain has been correctly configured before beam



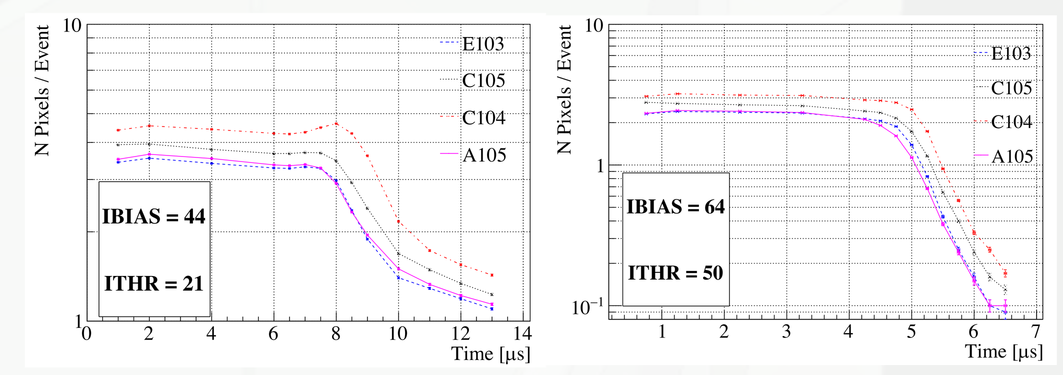
Cumulative hit distribution over the four staves for a typical data taking run at the 2019 test beam

From the test beam data it is also possible to understand and improve on the tracking algorithms that will be used in the final detector. This was achieved by producing fixed-target proton lead collisions upstream of the detector allowing for numerous tracks across each ALPIDE chip.

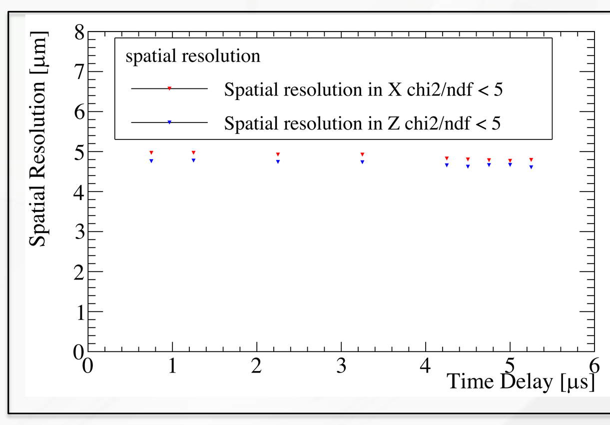


Track reconstruction of a single proton-lead event at the 2019 test beam showing three tracks, without detector alignment corrections. The x-y axis covers a single chip while the z-axis gives the stave separation

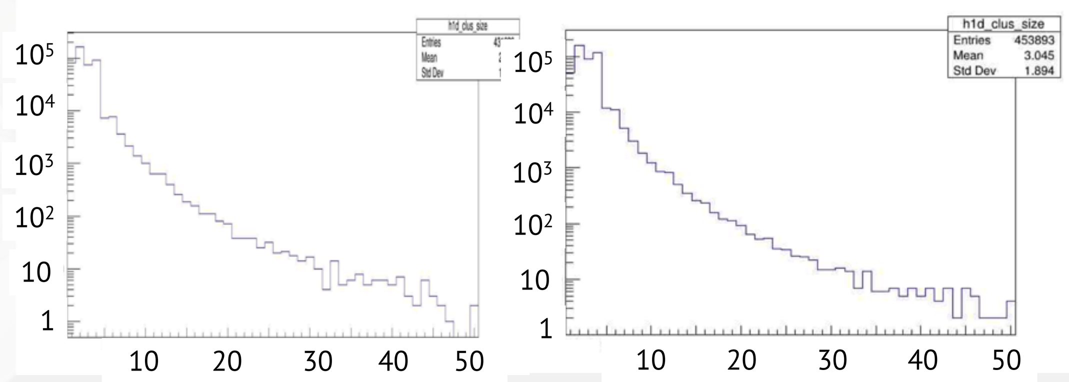
The pixel parameters can easily be tuned by the user to accommodate various physics environments and the LHC environment is very different to the RHIC environment. The hit efficiency was studied by altering the threshold parameters of the analogue pulse shape then varying the trigger delay. It has been noted that the ALPIDE chips can have a hit efficiency > 99.5% and a spatial resolution < 7 μm within the expected RHIC trigger latency.



The number of detected hits per event for the four staves tested as a function of trigger delay. The variable threshold settings are highlighted in bold. The expected RHIC trigger latency is approximately 5μs.



The spatial resolution as a function of trigger delay in rows (blue) and columns (red)



The cluster size distribution for all chips for perpendicular tracks (left) and η = 1 tracks (right). The mean cluster size is 2.72 pixels/event and 3.05 pixels/event perpendicular tracks and η = 1 tracks respectively.

[1] arXiv 1207.6378
[2] Nuclear Instruments and Methods in Physics Research A 824 (2016) 434–438
[3] 2016 JINST 11 C12074
[4] arXiv 1806.10667

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