BIS 2v0 - Proposal

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BIS 2v0 workshop – 15th November 2018

Content

- Motivation to upgrade the BIS
- Proposed hardware/software upgrades
- Planning
- Conclusions

Why a BIS 2v0?

Obsolescence, new requirements and maintainability

Why a BIS 2v0?

Obsolescence, new requirements and maintainability

- **Aging** - limited spares, new installations and support up to the end of HL-LHC
- **Discontinuity** of critical electronic components - Xilinx CPLD XC9500 and FPGA Spartan 3
- **Full occupancy** of FPGA logic cells - no space for implementing new functionalities
- **Wiener VME crate** with redundant power supplies not supported anymore

Why a BIS 2v0?

Obsolescence, **new requirements** and maintainability

- **User interface concentrator** – request to interface PCs in injectors, see talk from B. Todd and D. Nisbet
- **Common interface between BIS and actuators** – request to remove complexity of having to decode the Beam Permit frequencies (BE-RF, TE-EPC…)
- Add **FALSE frequency** to Beam Permit signal – request to mitigate glitches in DC operation (TE-ABT), see talk from R. Secondo
- **Consider beam-beam effects** in the way beam permit loops are linked, see talk from C. Wiesner and D. Wollmann

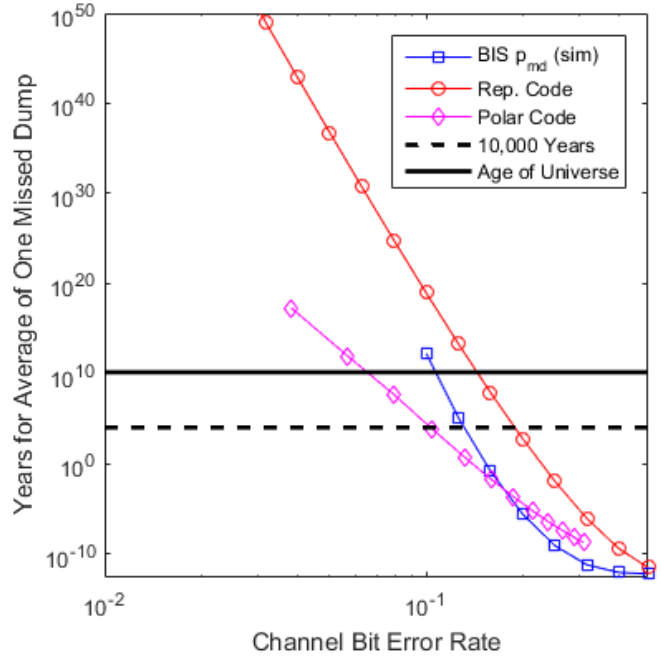
Why a BIS 2v0?

Obsolescence, new requirements and **maintainability**

- Increase **number** of user permit connections to the BIS
- Improve **flexibility** of user permit configurations – maskable /unmaskable, single/both beams configurable on demand…
- Improve **optical** transmission – power budget and diagnostics
- Consider **timing** events as user inputs – e.g. timing destinations as user permits
- Encoding **Beam Permit on packets**? – See next slide

Frequency vs packet-based solution

- Launched **study to compare existing optical solution with some packet-based solutions**
- Advantage is that **additional information** could be transmitted over the same fibres (monitoring, etc)
- Study compares **frequency vs error-correction codes** (n-repetition and polar codes)
  - Existing solution uses signals of 32 edges within a window of 128 samples
  - Repetition code that transmits 32 copies of an information bit within a window of 128 samples
  - Polar code that transmits 32 encoded bits within a window of 128 samples



- **Conclusions:**
  1. Existing solution is more than **adequate in terms of safety and availability**
  2. In principle, transmission of additional information **cannot improve reliability**
  3. Packet-based solution requires **packet-level synchronization and specialized signal processing algorithms**
  4. Good practice to **separate the safety critical signals from diagnostics**

Courtesy: A. Balatsoukas

HW upgrades – Platform

- BE-CO committed to **support VMEbus for HL-LHC era** (see J. Serrano's contribution)
- BE-CO advised not to move to other platforms such as PXI or uTCA
- **VME64x fulfil requirements** in terms of bandwidth and latency for BIS 2v0

- Assuming we keep VME => replacement of WIENER by ELMA chassis
- Side effects:
  - Reduced **number of available slots** (17 in ELMA vs 21 in WIENER)
  - **New backplane design** for both LHC and SPS (keep connectors compatibility?)

WIENER chassis

ELMA chassis

LHC backplane

SPS backplane

HW upgrades – CIBM/CIBX

Manager/Master boards combine user permits to derive two redundant beam permits

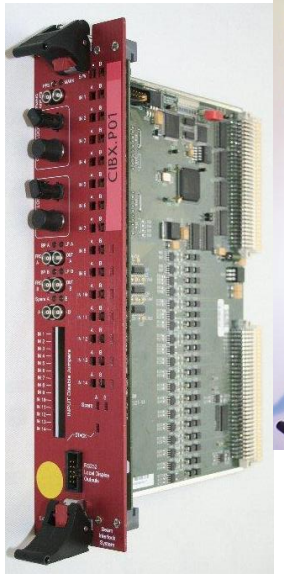
At present

- Physical separation for **critical code** and **monitoring**
- **Obsolete** electronic components and CPLD + FPGA at the limit of its capacity

For BIS 2v0

- New board to improve **limitation on user inputs**
  - Increase **number of inputs** – Trade-off between complexity and nb. of controllers
  - Improve **flexibility** – Configurable inputs (masking/unmasking, single/both beams)
- Integrate **SFP transceivers** – Improved optical budget, diagnostics and maintainability
  - Introduce **FALSE frequency** for beam permits
- Merge **remote diagnostics** from CIBT board
- Improve **routing of timing destinations** - e.g. LINAC4

- Generator (CIBG) and Re-trigger (CIBDS) boards will be based on same HW design



CIBX


CIBM

HW upgrades – User interfaces

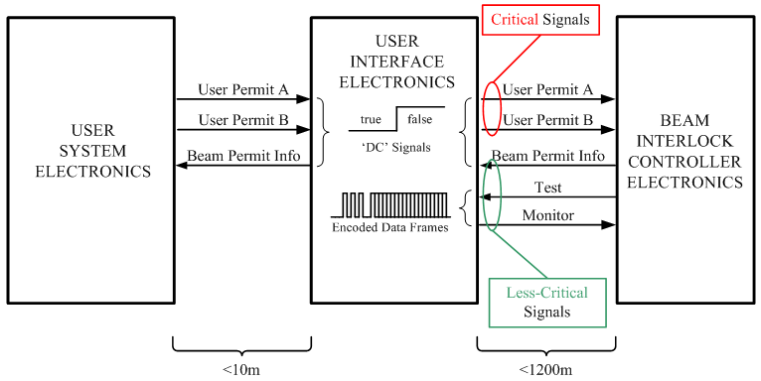
At present

- **Unique hardware** interface for all BIS users (CIBU + CIBF) => ~400 units in operation
- Safety critical implementation relies on **current loops** and analog electronics
- XILINX XC9500 **CPLD is obsolete**

For BIS 2v0

- Redesign **hardware interfaces** following backplane redesign? Cost, impact, backward compatibility…
- Need of **concentrator** to gather multiple user connections (e.g. PCs in LHC injectors)
- **Investigate the need of radiation tolerant design** (CPLD, optocoupler, power supplies, RS485 transceivers - some of them installed close to the beam, e.g. RRs)

CIBUS



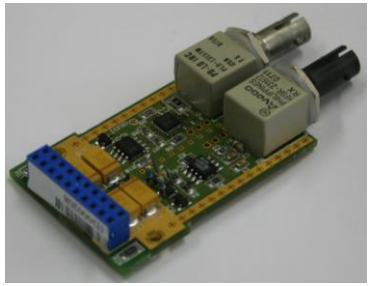
HW upgrades – Optical transceivers

At present

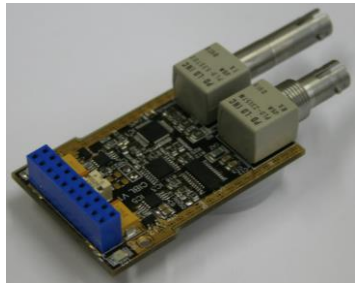
- Two boards used for optical communications – **CIBO and CIBL**
- **CIBO** (ELED) transceiver for **beam permit frequencies** – limited power budget and lack of monitoring
- **CIBL** (LASER) transceiver for **user permit signals** over long distances (e.g. used in CIBF for both BIS and SMP) – high power budget and enhanced diagnostics

For BIS 2v0

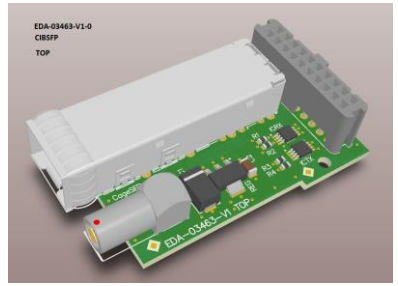
- **New CIBSFP board** to overcome the limitations of the present CIBO
- SFPs provide **high power transmission and reception sensitivity**, enhanced diagnostics and better maintainability
- Plans to replace **CIBL** by **CIBSFP** and maintain a single optical transceiver



CIBO



CIBL



CIBSFP

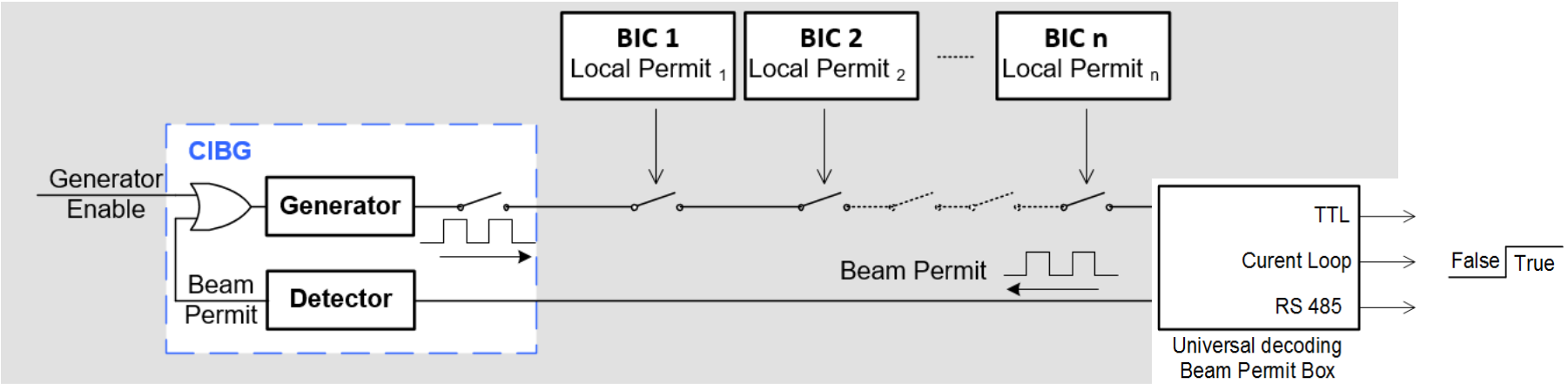
HW upgrades – Interface to actuators

At present

- Beam Permit signals delivered through **optical** links
- Actuators are responsable for **decoding a frequency** (using a CIBO) to derive the Beam Permit - e.g. TSU in LBDS
- Alternatively, Beam Permit signals can be delivered **through a differential signal transmission** and translated to TTL (using a CIBIR) - e.g. RF source in LINAC4

For BIS 2v0

- Due to the diversity of actuators (TE-ABT, BE-RF, TE-EPC…) -> develop a **unique interface** box in charge of decoding the frequencies and delivering the Beam Permit in various standards (TTL, differential, current loop…)
  - **Standard** interface to all
  - **Reliable decoding** of Beam Permit frequencies
  - **Diagnostics** available



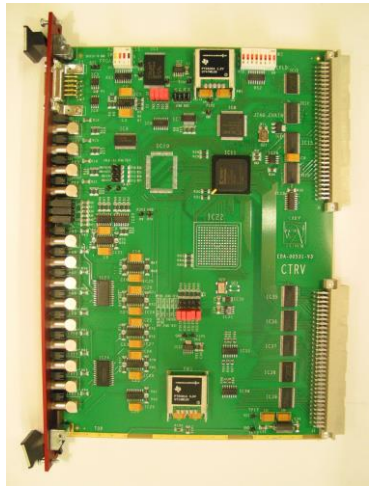
HW upgrades - CISV

At present

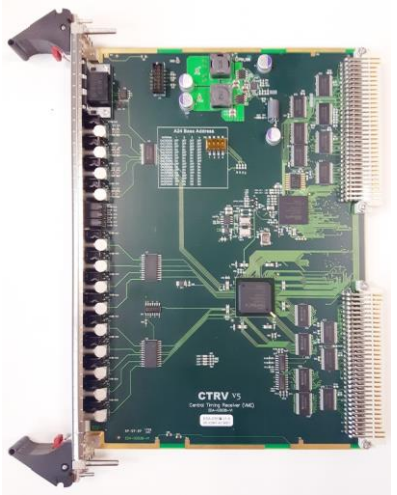
- Board used **to decode SMP flags from GMT** (e.g. Setup Beam, Beam Presence, Stable Beams…)
- LHC BICs receive the **Setup Beam Flag with a CISV board**
- CISV board is based on a CTRV with dedicated firmware maintained by MPE-MI

For BIS 2v0

- An option could be to **port the CISV firmware to the new CTRVD** (from BE-CO)
- Or develop a **new board** taking into account possible new flags (i.e. SMP 2v0)



CISV

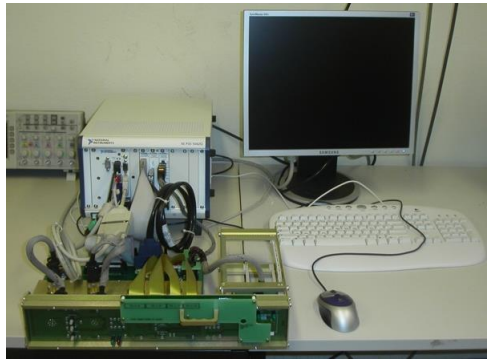


CTRVD

Testbeds + Software upgrades

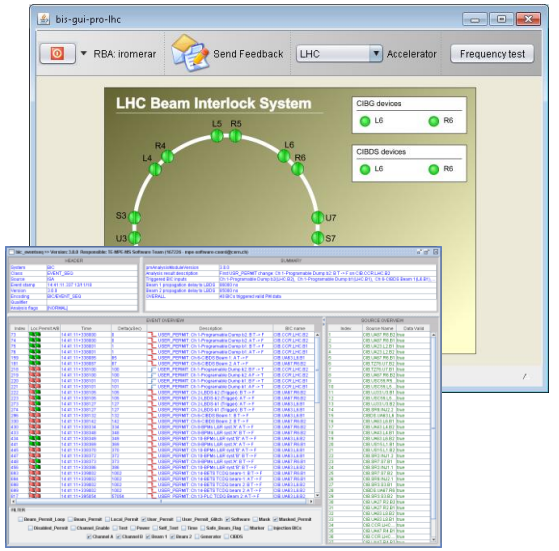
Upgraded hardware will require **new hardware/functional** test benches:

- CIBM/CIBX test bench
- CIBG/DS test bench
- CIBU test bench
- CIBIT & CIBIR test bench
- CIBSFP tester
- + python expert tools for hardware debugging

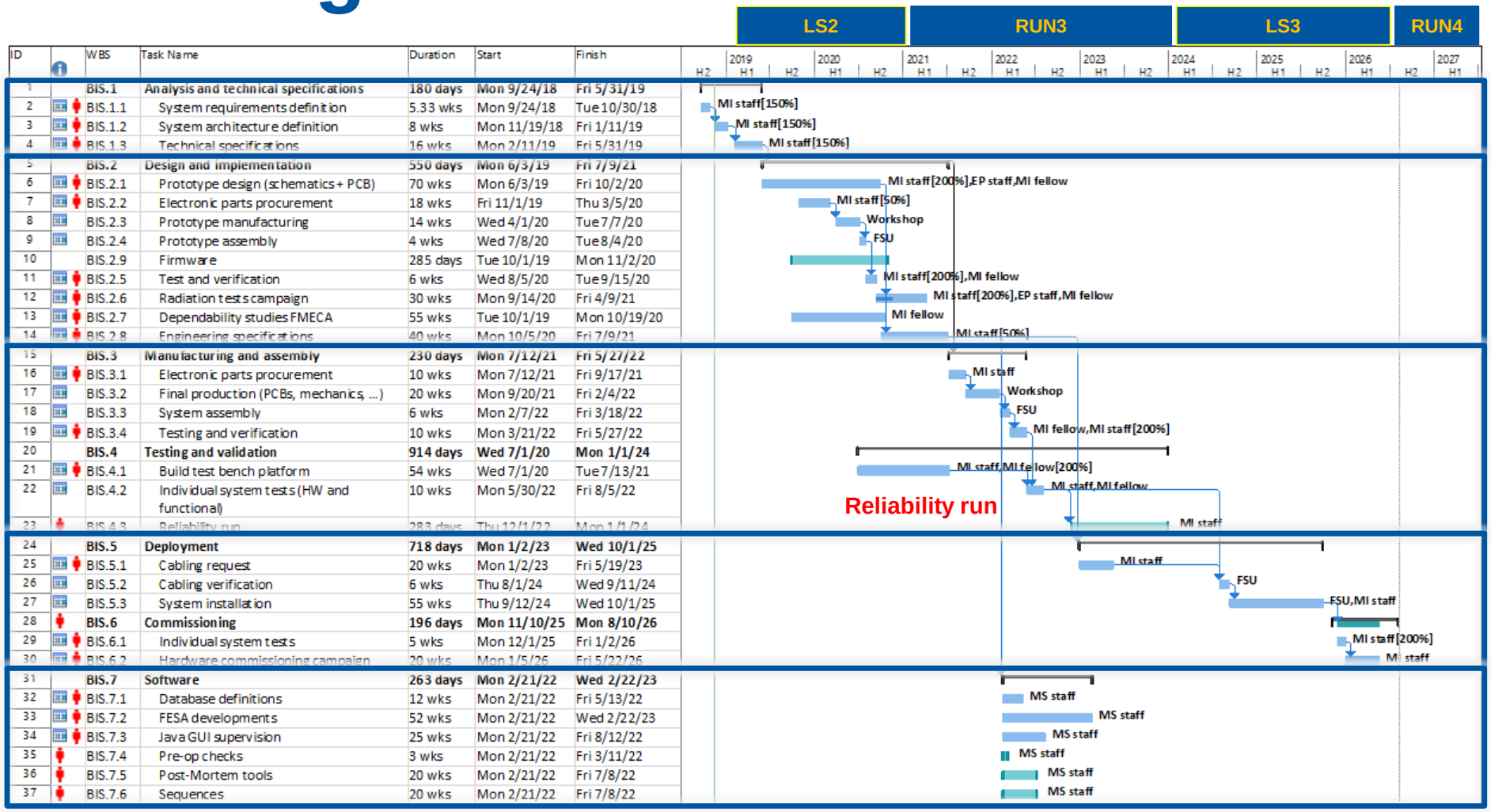


… and **controls:**

- FESA classes required for CIBM/X/DS/G
- Configuration DB + API
- Supervision tools
- Pre-operational checks
- Post-Mortem tools (e.g. BIS-ISA and BIS-IPOC)
- Sequences (e.g. rearming, ACC_TEST…)



Planning



ID	WBS	Task Name	Duration	Start	Finish
1	**BIS.1**	**Analysis and technical specifications**	**180 days**	**Mon 9/24/18**	**Fri 5/31/19**
2	BIS.1.1	System requirements definition	5.33 wks	Mon 9/24/18	Tue 10/30/18
3	BIS.1.2	System architecture definition	8 wks	Mon 11/19/18	Fri 1/11/19
4	BIS.1.3	Technical specifications	16 wks	Mon 2/11/19	Fri 5/31/19
5	**BIS.2**	**Design and implementation**	**550 days**	**Mon 6/3/19**	**Fri 7/9/21**
6	BIS.2.1	Prototype design (schematics + PCB)	70 wks	Mon 6/3/19	Fri 10/2/20
7	BIS.2.2	Electronic parts procurement	18 wks	Fri 11/1/19	Thu 3/5/20
8	BIS.2.3	Prototype manufacturing	14 wks	Wed 4/1/20	Tue 7/7/20
9	BIS.2.4	Prototype assembly	4 wks	Wed 7/8/20	Tue 8/4/20
10	BIS.2.9	Firmware	285 days	Tue 10/1/19	Mon 11/2/20
11	BIS.2.5	Test and verification	6 wks	Wed 8/5/20	Tue 9/15/20
12	BIS.2.6	Radiation tests campaign	30 wks	Mon 9/14/20	Fri 4/9/21
13	BIS.2.7	Dependability studies FMECA	55 wks	Tue 10/1/19	Mon 10/19/20
14	BIS.2.8	Engineering specifications	40 wks	Mon 10/5/20	Fri 7/9/21
15	**BIS.3**	**Manufacturing and assembly**	**230 days**	**Mon 7/12/21**	**Fri 5/27/22**
16	BIS.3.1	Electronic parts procurement	10 wks	Mon 7/12/21	Fri 9/17/21
17	BIS.3.2	Final production (PCBs, mechanics, ...)	20 wks	Mon 9/20/21	Fri 2/4/22
18	BIS.3.3	System assembly	6 wks	Mon 2/7/22	Fri 3/18/22
19	BIS.3.4	Testing and verification	10 wks	Mon 3/21/22	Fri 5/27/22
20	**BIS.4**	**Testing and validation**	**914 days**	**Wed 7/1/20**	**Mon 1/1/24**
21	BIS.4.1	Build test bench platform	54 wks	Wed 7/1/20	Tue 7/13/21
22	BIS.4.2	Individual system tests (HW and functional)	10 wks	Mon 5/30/22	Fri 8/5/22
23	BIS.4.3	Reliability run	283 days	Thu 12/1/22	Mon 1/1/24
24	**BIS.5**	**Deployment**	**718 days**	**Mon 1/2/23**	**Wed 10/1/25**
25	BIS.5.1	Cabling request	20 wks	Mon 1/2/23	Fri 5/19/23
26	BIS.5.2	Cabling verification	6 wks	Thu 8/1/24	Wed 9/11/24
27	BIS.5.3	System installation	55 wks	Thu 9/12/24	Wed 10/1/25
28	**BIS.6**	**Commissioning**	**196 days**	**Mon 11/10/25**	**Mon 8/10/26**
29	BIS.6.1	Individual system tests	5 wks	Mon 12/1/25	Fri 1/2/26
30	BIS.6.2	Hardware commissioning campaign	20 wks	Mon 1/5/26	Fri 5/22/26
31	**BIS.7**	**Software**	**263 days**	**Mon 2/21/22**	**Wed 2/22/23**
32	BIS.7.1	Database definitions	12 wks	Mon 2/21/22	Fri 5/13/22
33	BIS.7.2	FESA developments	52 wks	Mon 2/21/22	Wed 2/22/23
34	BIS.7.3	Java GUI supervision	25 wks	Mon 2/21/22	Fri 8/12/22
35	BIS.7.4	Pre-op checks	3 wks	Mon 2/21/22	Fri 3/11/22
36	BIS.7.5	Post-Mortem tools	20 wks	Mon 2/21/22	Fri 7/8/22
37	BIS.7.6	Sequences	20 wks	Mon 2/21/22	Fri 7/8/22

Definition of requirements

Design and implementation
- HW prototypes
- Firmware
- Test and verification

Testing, validation and manufacturing
- Build testbeds
- Launch production
- Reliability run in 2023

Deployment & commissioning
- Cabling
- Installation

Summary

- **Functional requirements** for BIS 2v0 remain **almost identical** to the present system
- System upgrade needed to address **obsolescence, improvements** and **long-term maintainability** to ensure smooth operation for the HL-LHC era
- **Synergies with SMP 2v0** and technical solutions may have an **impact on the interfaces** with users and actuators
- BIS 2v0 must be ready for **reliability run in 2023/24** and sitewide **deployment during LS3** (2024/25)

Spare slides

BIS inventory

Board name	Description	Operation	Spare
CIBM	Manager board	79	15
CIBX	Master board	5	5
CIBG	Frequency generator board	10	1
CIBDS	Retrigger board	2	4
CIBV	Post Mortem board	1	2
CIBWS	Setup Beam board	1	2
CIBUS	Single user interface	304	45
CIBUD	Double user interface	49	8
CIBD	DC power supply	832	133
CIBFU	Laser user interface - User	36	5
CIBFC	Laser user interface - Controller	36	5
CIBO	Optical transceiver	245	24
CIBL	Laser optical transceiver	89	45
CIBIT	Differential transmitter board	3	1
CIBIR	Differential receiver	6	25
CIBPB	Patch panel for diff. transmitter	3	2
CIBPT	Patch panel for diff. receiver	6	14
CIBT	Test and Monitor board	68	7
CIBMD	Manager display	79	15
CIBTD	Test and Monitor display	68	14
CIBPS	Patch panel for SPS	20	14
CIBPL	Patch panel for LHC	19	2
CIBB	Distribution bay	30	0
CIBEA	Extension type-A	156	20
CIBEB	Extension type-B	78	17

Safety critical electronics

Safety critical electronics for interface with users

Optical transceivers

Safety critical electronics for interface with actuators

Monitor and diagnostics

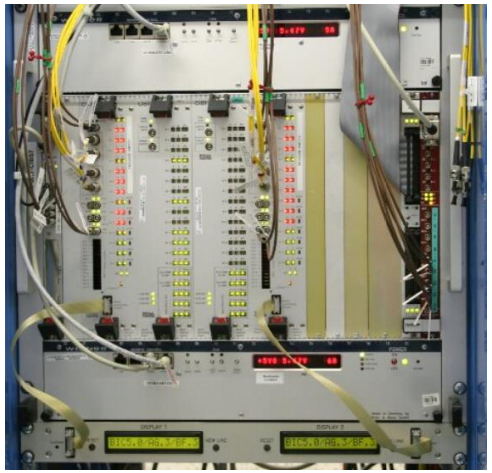
Patch panels and interface boards

More than 2000 electronic boards currently in operation!

Present BIS hardware

- Hardware based on **VME-architecture**
- **Critical** functionality is **hardware** only
- **Physical separation** for critical/monitor functions
- Remote update of monitor but not critical code
- Redundant critical path for **high safety**
- Redundant power supplies for **high availability**
- Modular design for **flexibility**

User interface (CIBU)



BIC front view

BIC rear view