
CERN

BIS v2 Workshop
15-11-2018

Power Converter perspective

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1. The PC environment
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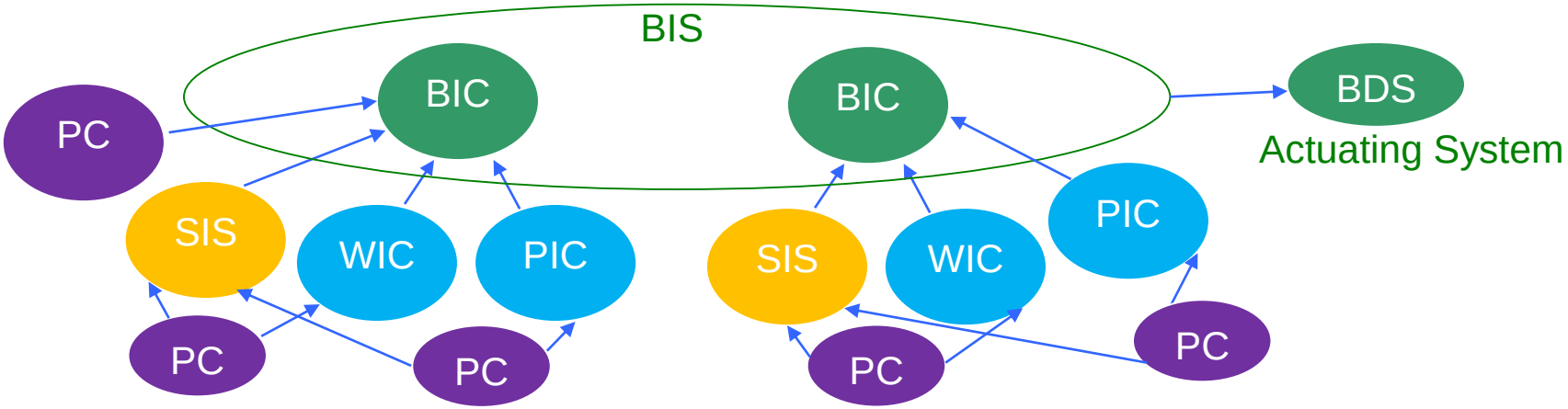
Introduction

How a power converter interfaces to the CERN accelerator complex

1. where reliable knowledge of the converter state is necessary
   a. use WIC (Warm magnet Interlock Controller) or PIC (Powering Interlock Controller for LHC cryo circuits) to interface to BIS
   b. reliable, latched, modest speed (~100ms, exceptionally can be ~1ms)
   c. standard for all EPC power converters
2. where speed is not critical, interlocking can be complemented with SIS solutions (Software Interlock System)
3. where speed and additional functionality are needed (for example no latching of status) interface directly to the Beam Interlock System



How the existing systems work

- LHC Power Converters
  - No direct connection to the BIS
  - All power converters interface via PIC or WIC
  - Fast interlocks use Fast Magnet Current Monitor

See EDMS 678140

- SPS Power Converters
  - Direct connection to BIS through Mugef gateway
  - Fast Extraction Interlock

See EDMS 602470

- L4 and PSB Power Converters
  - Direct connection to BIS for some equipment
  - Source, Quads, Bendings, Septa

See EDMS 1016233

PC Roadmap and the BIS

The roadmap for our power converter controls is based on FGC technology

1. FGC:
   a. Interfacing the FGC to the BIS is already required in the CPS (eg L4, PSB, SPS…)
   b. Existing solution cannot set or monitor thresholds remotely
   c. Precision threshold settings needed (~1% possible today; ~0.1% desired)
2. SPS:
   a. Foresee end-of-life of MUGEF architecture at LS3 (and begin deployment of FGC technology from LS2)
   b. A solution that can scale to many inputs is needed

A new platform is required to interface the power converters to the Beam Interlock System, which is common across the accelerators

SPS Converter Controls Strategy

Requirement, particularly in the SPS, to connect many Power Converters to a single BIS channel:

SPS in LS2: connect 142x FGC3 devices to 9x BIS input channels

SPS in LS3: connect all 228x FGC3 devices (86x new) to all 18x BIS input channels

We need to concentrate the PC signals

Era:	LS1	LS2	LS3
Converter Controls Strategy	All centralized (MUGEF)	mixture	All distributed (FGC)
Interlock Strategy	Fast Extraction Interlock & MUGEF	BISCON	New Beam Interlock System & RegFGC3

BISCON handles the interim case

Agreement with the Machine Protection group (MPE) to provide a new BIS in LS3 to meet our needs

EDMS 1954156

Installation and commissioning

Estimate of Power Converter Beam Interlock requirements in the coming years

Machine	Qty @ LS2	Qty @ LS3
SPS + transfer lines	142	86
PS + transfer lines	0	~50?
PSB + transfer lines	~30	0
L4 + transfer lines	~10	0
Total	~200	~150

In all cases the appropriate FGC3 properties and RBAC rules need to be configured

Installation of a new Beam Interlock board must be announced to CCS, CO and OP

(New) PC to BIS Interface

The basic requirements are:

1. FGC will calculate the USER PERMIT -> no more analog setpoints!
2. Evaluation will be continuous (not limited to specific moments triggered by timing events)
3. Remote setting and monitoring is required, with associated write protection management
4. The USER PERMIT can be calculated from the evaluation of a variety of sources
    1. The PC state
    2. window for either I_meas (A) or V_meas (V)
    3. window on the regulation error (for f{i_ref} or f{v_ref})
    4. window on the derivative of I_meas or V_meas (di_meas/dt, dv_meas/dt)
5. Different settings can be used for each machine USER (ppm functionality)
    a. The USER (ppm) support can be inhibited for simpler applications, so only one setting is required
6. Fast (150us propagation from signal to action), with up to 4 different windows per converter

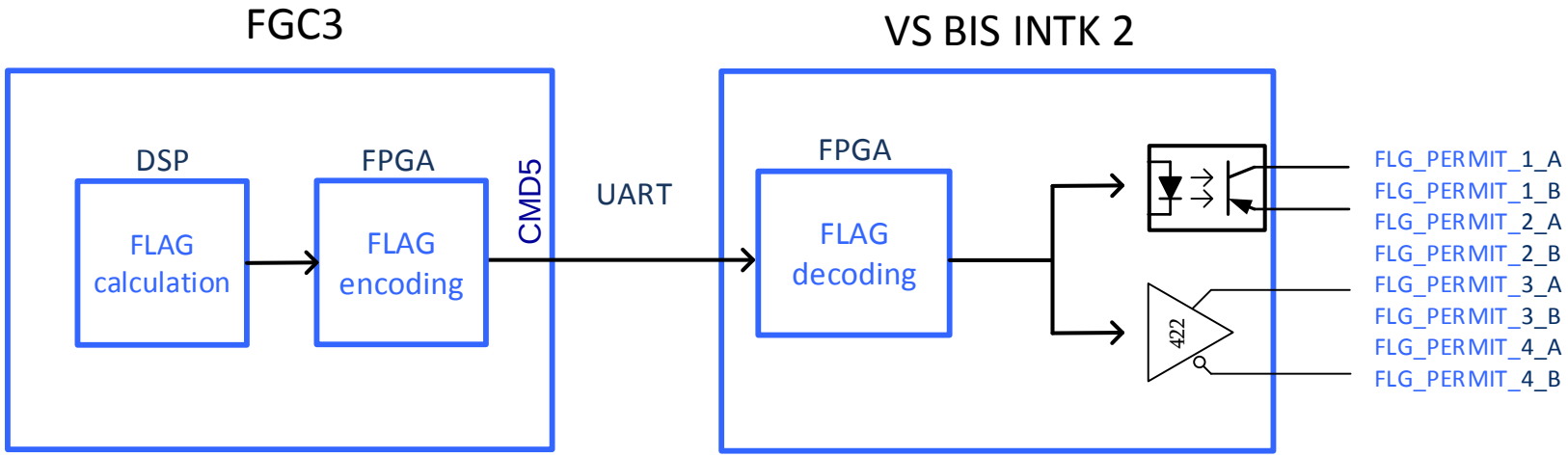
7. Must be able to scale to many power converters (required for SPS, perhaps also other applications)
    a. Need to consider how to send signals on cables up to 100m long

Full description of requirements is summarized in the functional specification here:
https://edms.cern.ch/document/1744675

(New) PC to BIS Interface

Overview of FGC electronic components

- The new version simply decodes the information received by the FGC3
  - acting as a simple interface between FGC3 and CIBU/Concentrator
- Two possible output interfaces:
  1. current loop (direct connection to CIBU)
  2. RS422 (connection to concentrator, capable of communicating >100m)
- an FGC test mode allows one output at a time (ie 1A, 1B … 4B) to be controlled

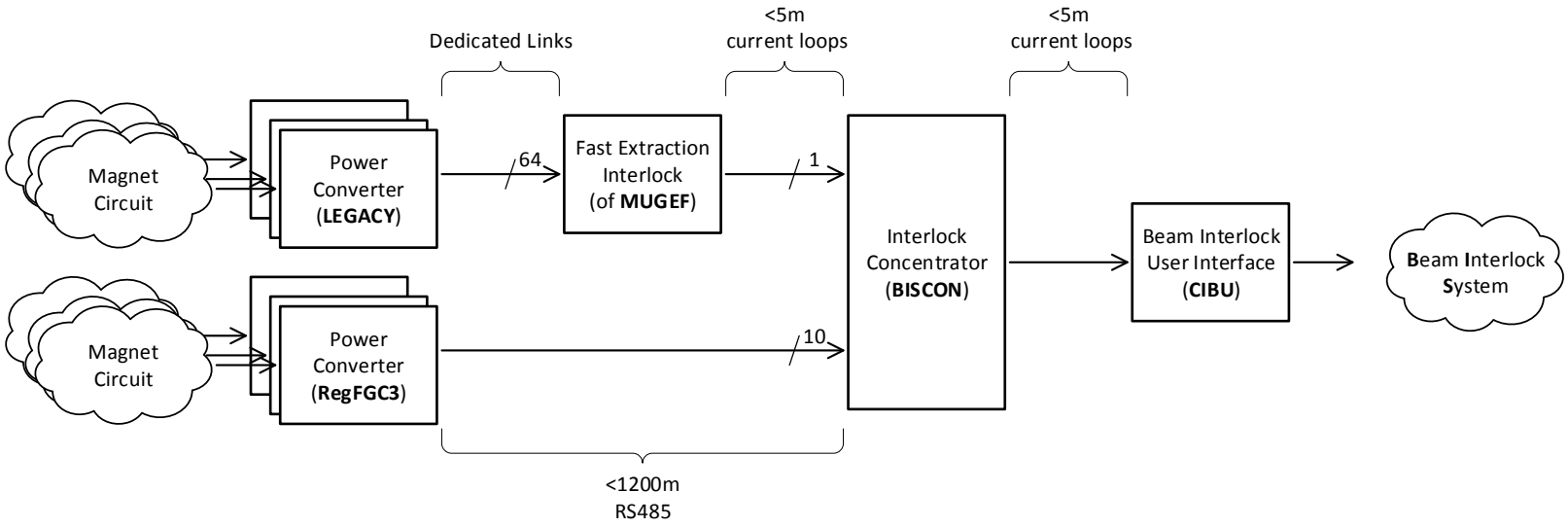


Connecting many PCs to 1 BIS channel

Requirement for deploying FGCs to the SPS

combines:

ten converter FLG_PERMIT signals from RegFGC3
Fast Extraction Interlock FLG_PERMIT from legacy controls



each BISCON can handle two redundant permit flags

Connecting many PCs to 1 BIS channel

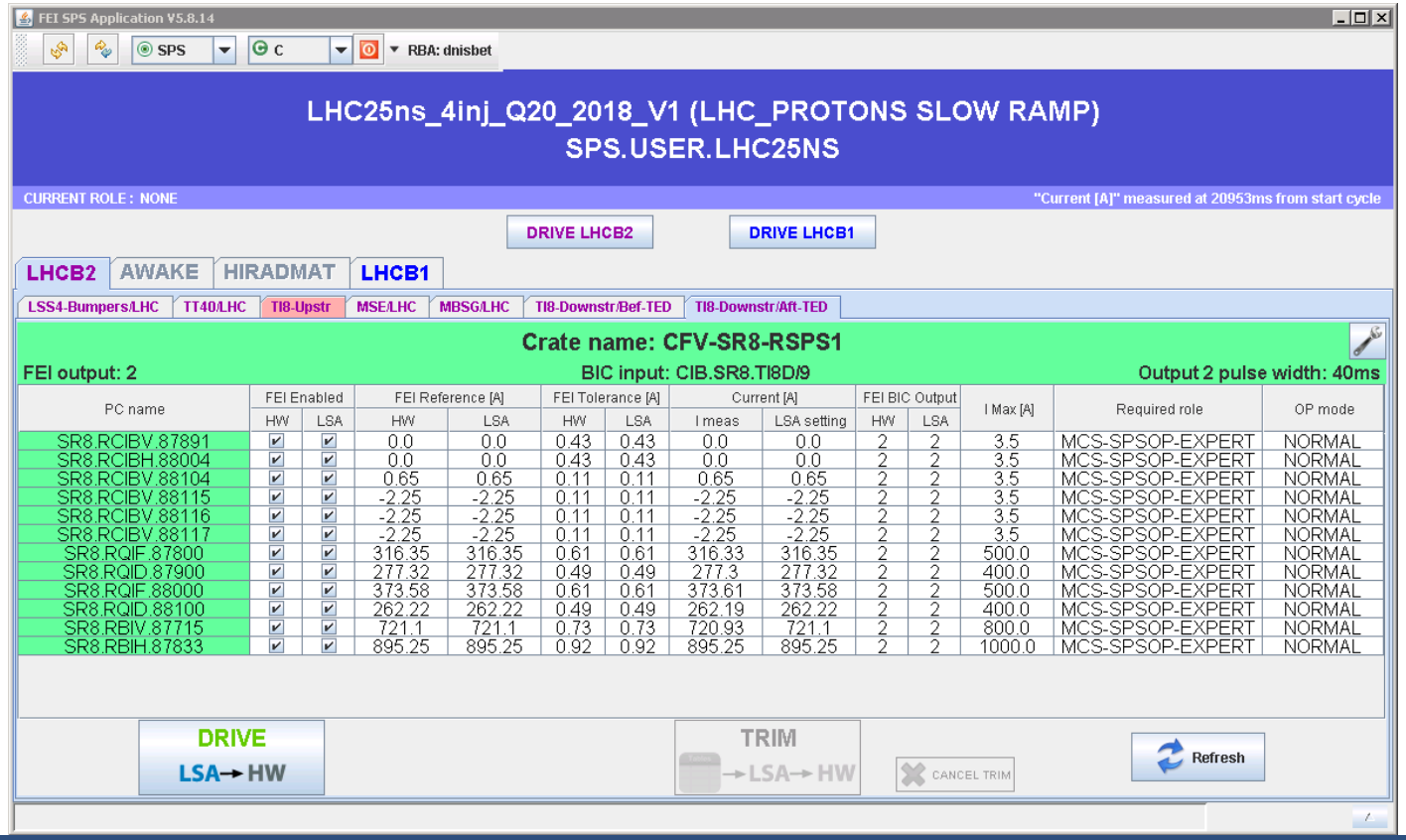
Prototypes made by TE-EPC of a PC signal concentrator solution (BISCON)

- Can be mechanically integrated into the COD racks (3U height, 10 systems/rack)
- Can be daisy chained (easily extend IO capability)
- DC diagnostics with test mode (no “history buffer”)

Diagnostics

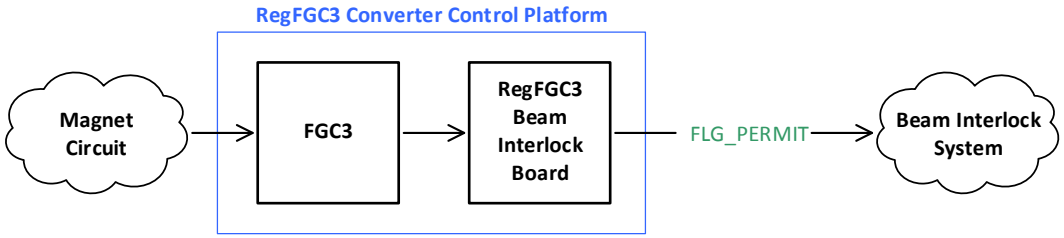
What diagnostics should a new platform be capable of delivering?

1. Ability to validate the PC to BIS connection using a test mode
   - used during HWC and machine checkout, and in fault finding
2. Integration of test mode into the CCC tools
   - for example into the FEI application
3. History buffer to show all transitions of signals affecting the permit



PC name	FEI Enabled		FEI Reference [A]		FEI Tolerance [A]		Current [A]		FEI BIC Output		I Max [A]	Required role	OP mode
	HW	LSA	HW	LSA	HW	LSA	I meas	LSA setting	HW	LSA			
SR8.RCIBV.87891	☑	☑	0.0	0.0	0.43	0.43	0.0	0.0	2	2	3.5	MCS-SPSOP-EXPERT	NORMAL
SR8.RCIBH.88004	☑	☑	0.0	0.0	0.43	0.43	0.0	0.0	2	2	3.5	MCS-SPSOP-EXPERT	NORMAL
SR8.RCIBV.88104	☑	☑	0.65	0.65	0.11	0.11	0.65	0.65	2	2	3.5	MCS-SPSOP-EXPERT	NORMAL
SR8.RCIBV.88115	☑	☑	-2.25	-2.25	0.11	0.11	-2.25	-2.25	2	2	3.5	MCS-SPSOP-EXPERT	NORMAL
SR8.RCIBV.88116	☑	☑	-2.25	-2.25	0.11	0.11	-2.25	-2.25	2	2	3.5	MCS-SPSOP-EXPERT	NORMAL
SR8.RCIBV.88117	☑	☑	-2.25	-2.25	0.11	0.11	-2.25	-2.25	2	2	3.5	MCS-SPSOP-EXPERT	NORMAL
SR8.RQIF.87800	☑	☑	316.35	316.35	0.61	0.61	316.33	316.35	2	2	500.0	MCS-SPSOP-EXPERT	NORMAL
SR8.RQID.87900	☑	☑	277.32	277.32	0.49	0.49	277.3	277.32	2	2	400.0	MCS-SPSOP-EXPERT	NORMAL
SR8.RQIF.88000	☑	☑	373.58	373.58	0.61	0.61	373.61	373.58	2	2	500.0	MCS-SPSOP-EXPERT	NORMAL
SR8.RQID.88100	☑	☑	262.22	262.22	0.49	0.49	262.19	262.22	2	2	400.0	MCS-SPSOP-EXPERT	NORMAL
SR8.RBIV.87715	☑	☑	721.1	721.1	0.73	0.73	720.93	721.1	2	2	800.0	MCS-SPSOP-EXPERT	NORMAL
SR8.RBIH.87833	☑	☑	895.25	895.25	0.92	0.92	895.25	895.25	2	2	1000.0	MCS-SPSOP-EXPERT	NORMAL

As a User of the Beam Interlock



Wish list

- Mechanism to detect **connection presence** between systems
- Read **identification number** from the connection, to avoid swapping mistakes.
- **Current loops** work locally – keep this interface.
- Allow us to connect using **differential signals** – proximity constraints relaxed
- Provide support for **test modes**
- Provide a **user interface** that accepts up to **10x user inputs in a 3U** format
- **Cost per channel** should be kept low

Ben's Wish List (beyond the PC)

Wish list

- it should be possible to determine when the **cable is connected** to the User System
- the various elements of the BIS should have a built in "time-on" or "stress-level" **accumulator**, so that when they fail that the Weibull is easier to do.
- The **optical fibres** need to be sorted out
  - Both in the main loop
  - And in the fibre optic unit
- The **test board** should not depend upon the CIBM
- The reception of **timing information** (e.g. SMP) should be embedded in each card, so that more complex decoding can be done, without using a CISV
- The **partitioning** of inputs should be checked, is 6+8+6 adequate? Should be more?
- Is VME the right **form factor**?

Conclusion

1. New FGC3 Power Converter Beam Interlock interface will be deployed ready for the restart following LS2
   - The settings management will be under the control of the CCC
2. To allow for interfacing many systems to a single channel, a concentrator platform is available
   - Use of RS422 standard allows a distance of >100m between power converter and concentrator
   - Will be extensively used in the SPS
   - Some applications in the PS can also benefit
3. Wishlist for the new BIS platform
   - can the limitations on user proximity to the CIBU be removed (eg RS422)?
   - allow many users to be connected for a modest cost
   - a seamless upgrade would fit with a modularity of 3U and 10 inputs
   - provide a history buffer for all inputs
   - integrate within the CCC environment to enhance remote testing and validation procedures

References

Reference documents

a. EPC Technical Seminar on Beam Interlocking [Indico 754989]
b. PC to BIS Functional spec [EDMS 1744675]
c. Concentrator Eng Spec [EDMS 1954156]
d. MPP meeting, April 2017 [Indico 634449]
e. MPP meeting, July 2016 [Indico 557965]
f. Consolidation IPAC paper, May 2018 [CDS 2289162]
g. New Beam Interlock board [EDA-34614]
h. Old Beam Interlock board [EDA-02662 & EDA-02663]
i. Beam Interlock Operation Note [tbc]

Thank you!

Questions?

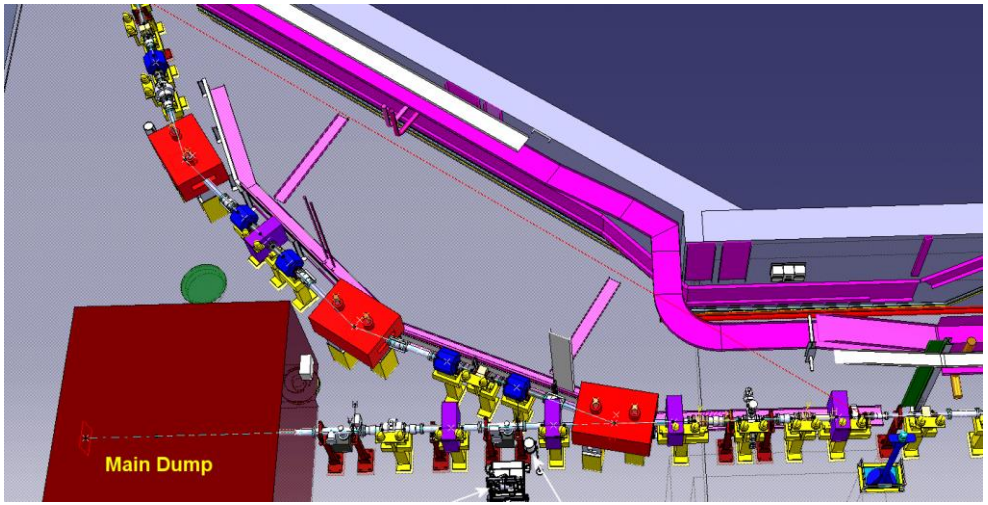
How the existing systems work: LINAC4

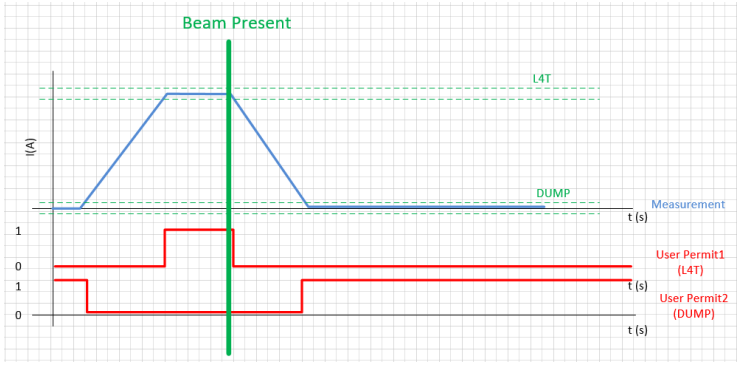
Example of a bending magnet (here at the end of LINAC4: L4T.RBH.021)

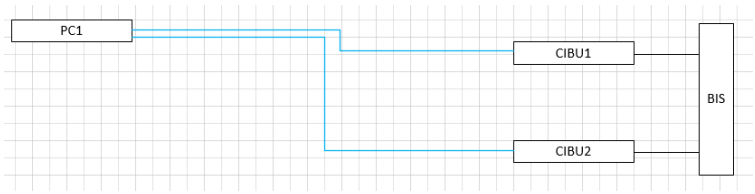
Two destinations:

1. Dump @ 0A
2. PSB at 612 A

Need to verify current is in tolerance to ensure beam stays within vacuum pipe.







How the existing systems work: SPS

Many systems are monitored in the SPS, taking advantage of the MUGEF architecture

Family name	Description	# Circuits	Imax A	tolerance ΔI/Imax
MBB	TT60 dipole	1	7500	0.001
MBG	TT41 main dipole	1	5400	0.001
MBHA	TT40 dipole	1	1100	0.001
MBHC	TT40 dipole	1	1000	0.001
MBI	TI 2 / TI 8 main dipole	2	5400	0.001
MBIAH	TI 8 dipole	1	1000	0.001
MBIAV	TI 2 / TI 8 dipole	4	1000	0.001
MBIBH	TI 2 dipole	1	800	0.001
MBIBV	TI 8 dipole	1	800	0.001
MBSG	TI 8 / CNGS switch	1	4400	0.001
MCIAV/H	TI 2 / TI 8 corrector	88	3	0.1
MCIBH	TI 8 dipole	1	400	0.001
MDAV/MDLH/MDLV	TT60 corrector	4	300	0.1
MDGV/MDGH	TT41 corrector	12	3	0.1
MDSV/MDSH	TT40 / TT41 / TT60 dipole	6	400	0.001
MPSH/MPLH	SPS H extraction bumper	8	400	0.001
MPSV/MPLV	SPS V extraction bumper	8	120	0.001
MQI	TI 2 / TI 8 main quadrupole	34	600	0.001
MSI	LHC injection septum	2	1000	0.001
MST	SPS extraction septum	1	7500	0.001
MSE	SPS extraction septum	2	24000	0.001
QTG	TT41 main quadrupole	8	500	0.001
QTL/QTM/QTR/QTS	TT40 / TT41 / TT60 quadrupole	16	500	0.001

How the existing systems work: SPS

SPS power converter beam interlock is based on the Fast Extraction Interlock (FEI).

The evaluation of the FEI is triggered by a timing event that is sent out twice for each fast extraction :

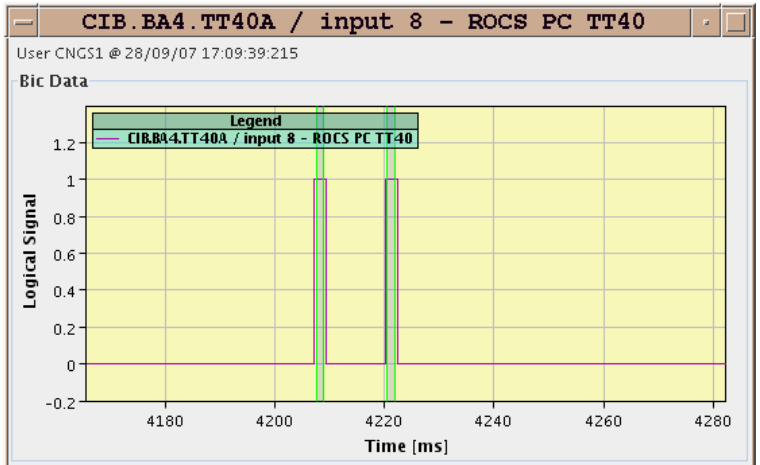
- At -16 ms to perform a preliminary check of the currents → start kicker resonant charge.
- At -4 ms to perform the final check of the currents.

At the moment of each timing event, if all PCs contributing to the PERMIT are in tolerance

- MUGEF FEC will send a PERMIT pulse (~few ms) to the beam interlock system

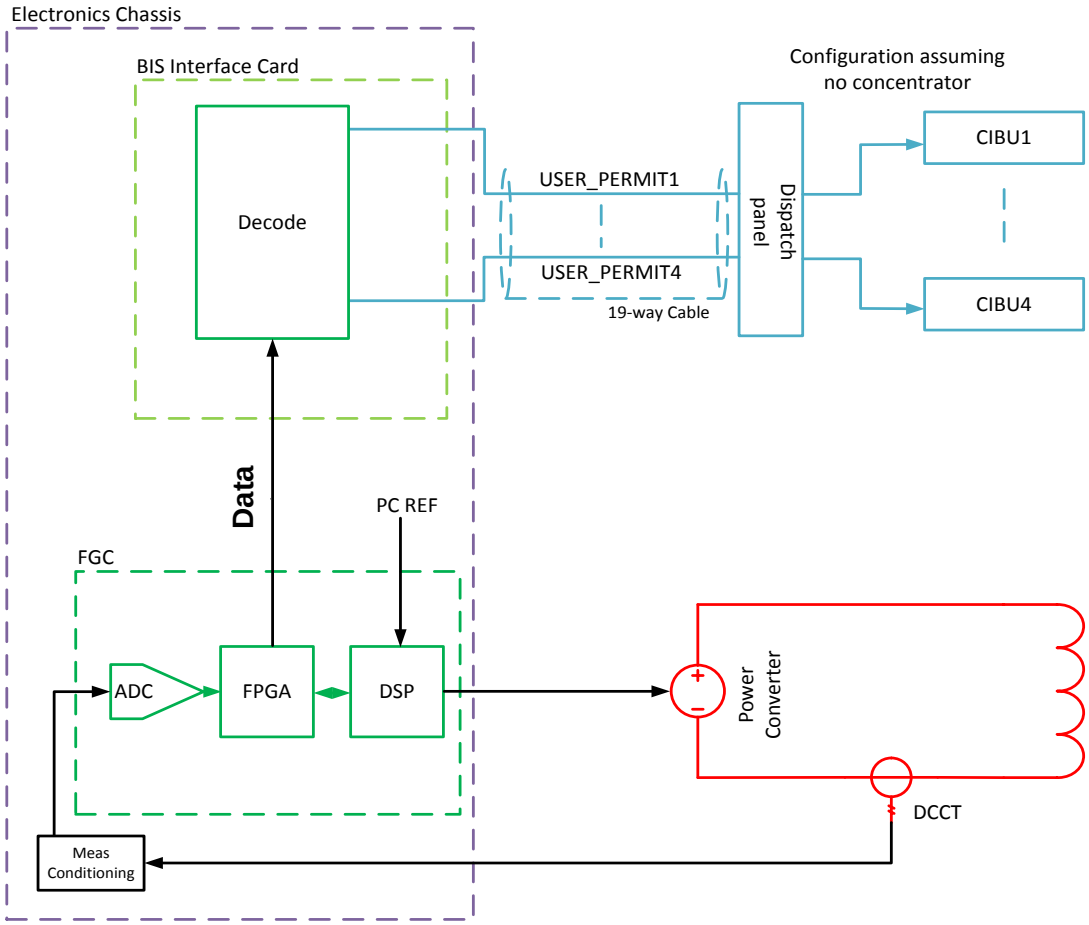
Key observations

1. The SPS FEI is a software based interlock system
2. All thresholds are managed remotely from CCC
3. The FEI is only evaluated when the timing events are sent



When all currents are in tolerance, 2x short pulses (triggered by the timing events) are sent to the BIS

Hardware Implementation Overview

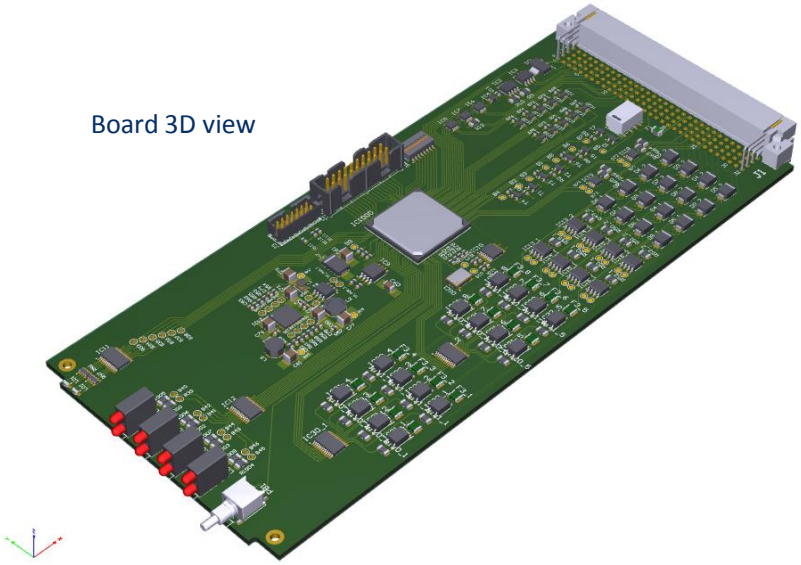


VS Beam Interlock Board

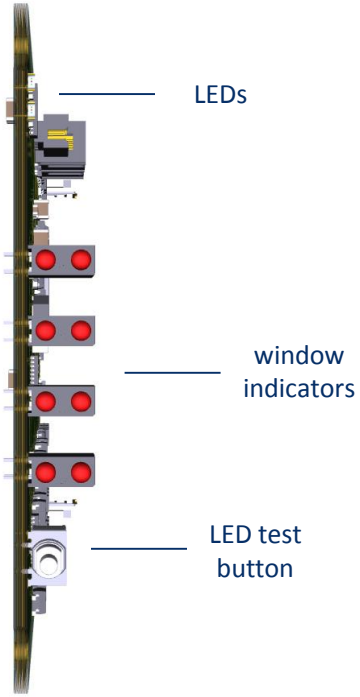
VS BIS INTK 2 (EDA-34614)

- Pinout compatible with previous version (EDA-02662)
- Work ongoing to design a single execution
  - output type (RS422 or Current Loop) is multiplexed and remotely configurable
- Status
  - Board schematic and routing being finalized
- Production plan:
  - Prototype test @ October 2018
  - Pre-series (#10) test in existing converters @ January 2019
  - Series production complete @ June 2019

Board 3D view

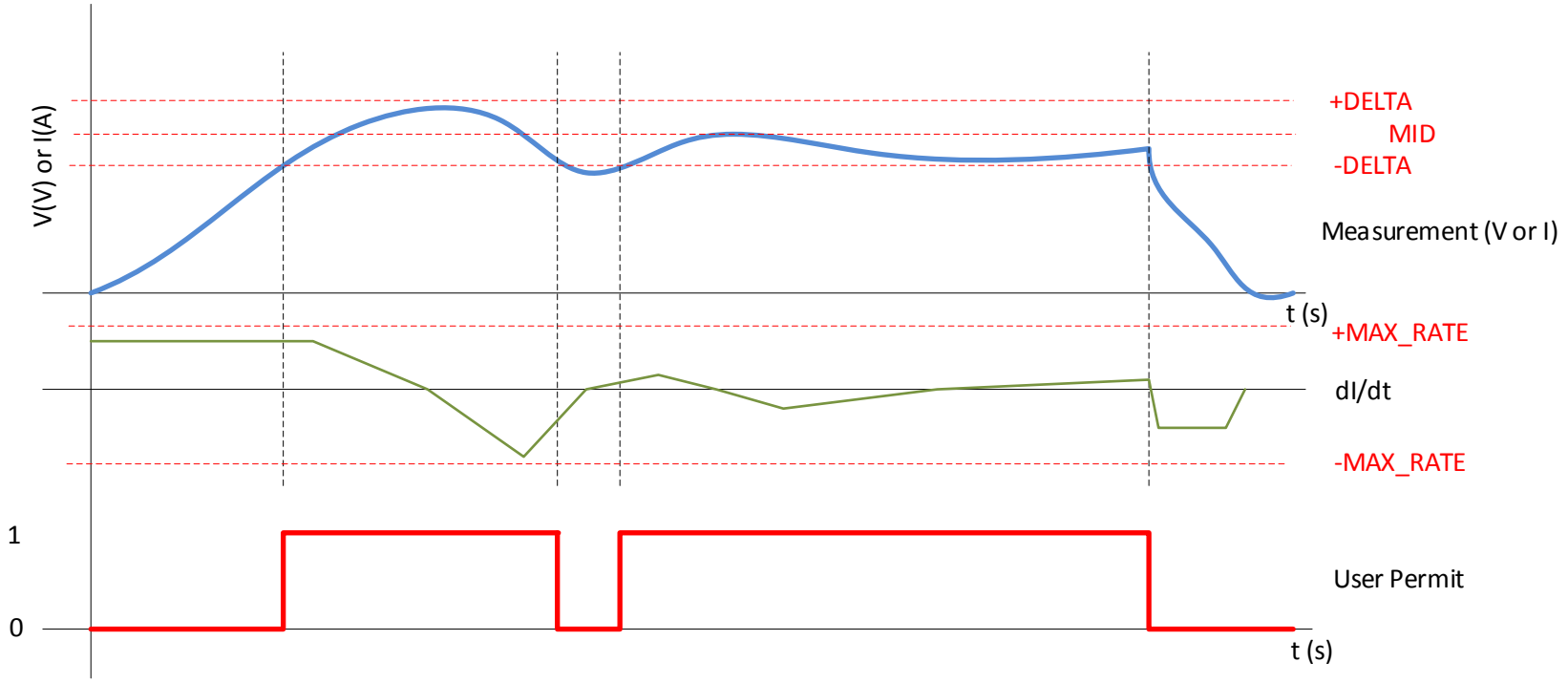


Front panel view



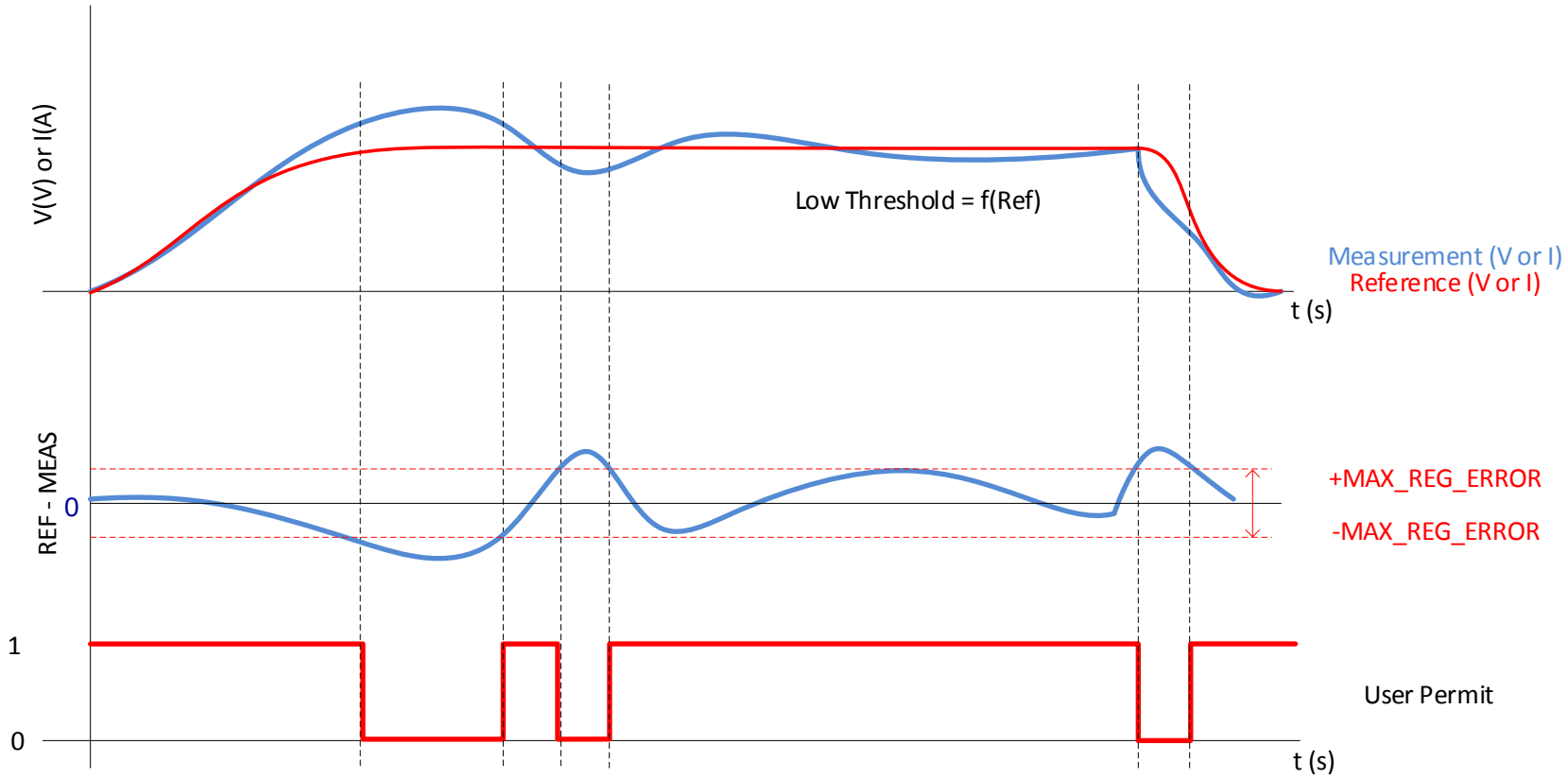
Operation principle

1. Evaluation of a simple window for either I_meas (A) or V_meas (V)
2. Evaluation of the derivative of I_meas or V_meas (di_meas/dt, dv_meas/dt)



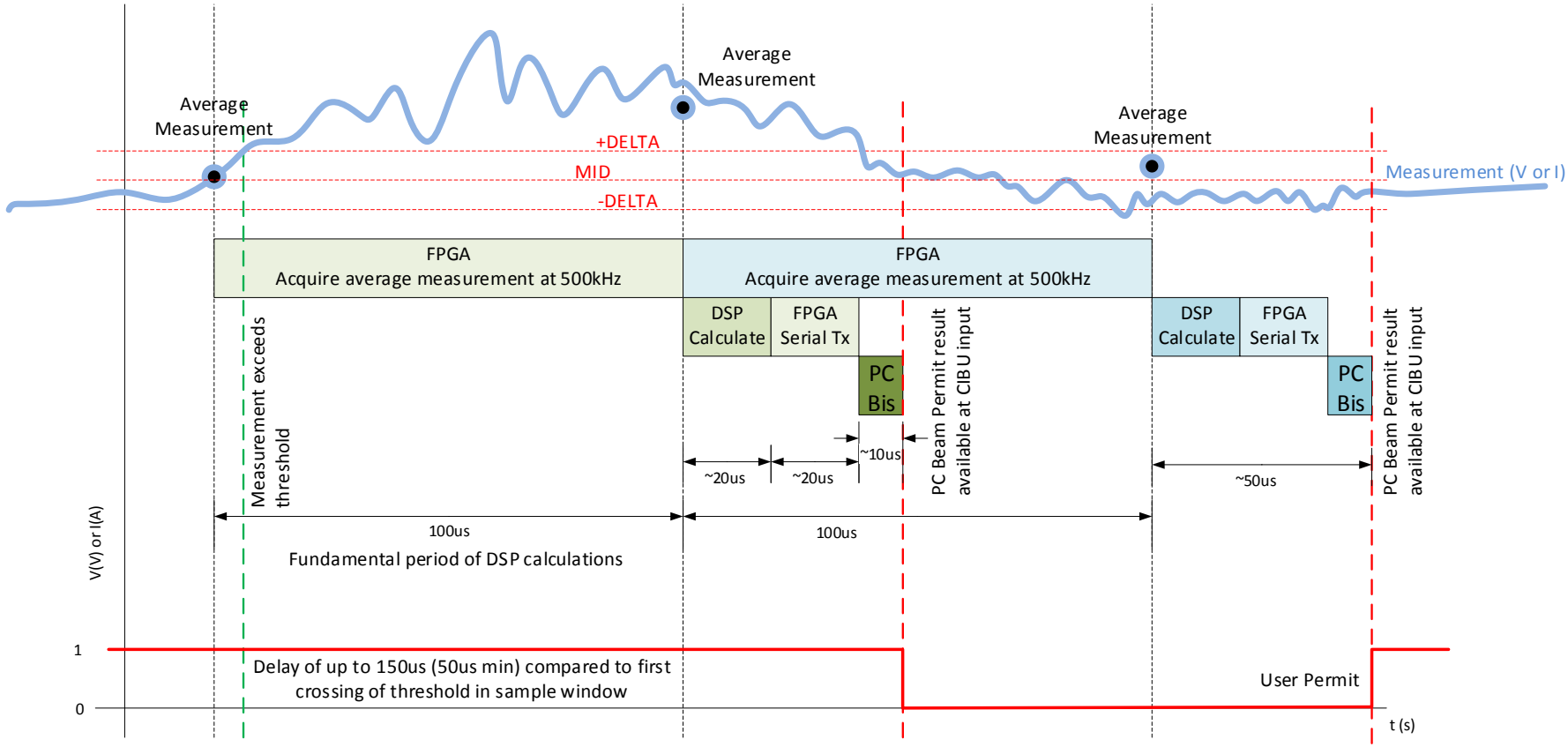
Operation principle

Evaluation of a window around a complex function (for f{i_ref} or f{v_ref})



1. The result is calculated from the error between the converter reference and the converter measurement
   a. The reference is the same as that used for the converter regulation

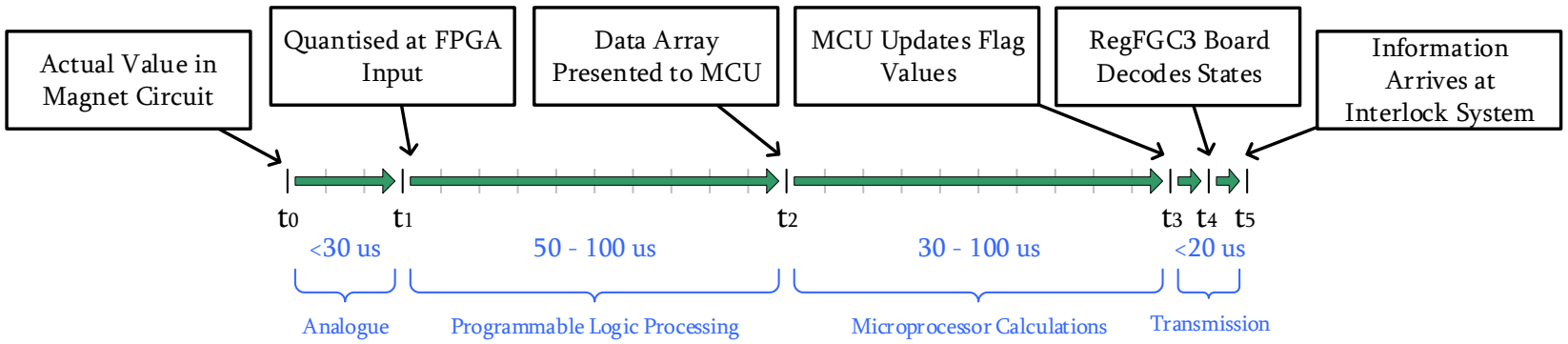
Operation principle



Latency

almost all latency is FGC3 processing

each concentrator adds <5µs latency, part of $t_4 \rightarrow t_5$



Example of RBAC rules

RBAC roles

Access Rules

1 - 7

Device Group	Property Group	Role	Location	Op Mode	Get	Set	Monitor
SPS	INTERLOCKS_GURU	OP-Daemon	AWAKE-HOSTS		☑	☐	☐
SPS	INTERLOCKS_GURU	SPS-Operator	CCC-LHC		☑	☑	☐
SPS	INTERLOCKS_GURU	SPS-Operator	CCC-SPS		☑	☑	☐
SPS	INTERLOCKS_GURU	MCS-SPSOP-GURU			☑	☐	☐
SPS	INTERLOCKS_GURU	MCS-SPSOP-EXPERT			☑	☐	☐
SPS	INTERLOCKS_GURU	MCS-SPSOP			☑	☐	☐
SPS	INTERLOCKS_GURU	MCS-SPSOP-GURU			☐	☑	☐

1 - 7

Access Rules

1 - 10

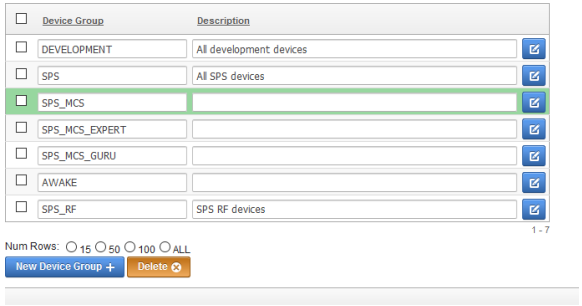
Device Group	Property Group	Role	Location	Op Mode	Get	Set	Monitor
SPS	INTERLOCKS	OP-Daemon	AWAKE-HOSTS		☑	☐	☐
SPS	INTERLOCKS	SPS-Operator	CCC-LHC		☑	☑	☐
SPS	INTERLOCKS	SPS-Operator	CCC-SPS		☑	☑	☐
SPS	INTERLOCKS	MCS-SPSOP-GURU			☑	☐	☐
SPS	INTERLOCKS	MCS-SPSOP-EXPERT			☑	☐	☐
SPS	INTERLOCKS	MCS-SPSOP			☑	☐	☐
SPS_MCS_EXPERT	INTERLOCKS	MCS-SPSOP-EXPERT			☐	☑	☐
SPS_MCS_GURU	INTERLOCKS	MCS-SPSOP-GURU			☐	☑	☐
SPS_MCS	INTERLOCKS	MCS-SPSOP			☐	☑	☐
	INTERLOCKS	PO-Expert		NON-OPERATIONAL	☑	☑	☐

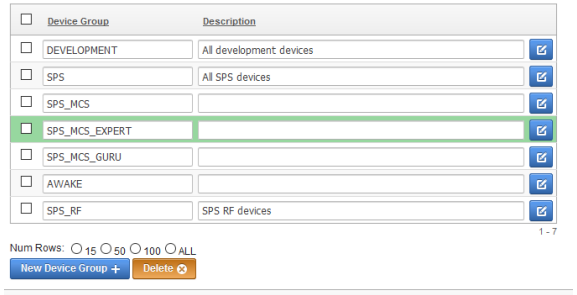
1 - 10

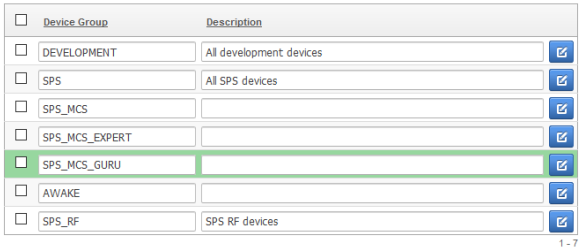
https://wikis.cern.ch/display/TEEPCCCS/libintlk+-+Interlock+library

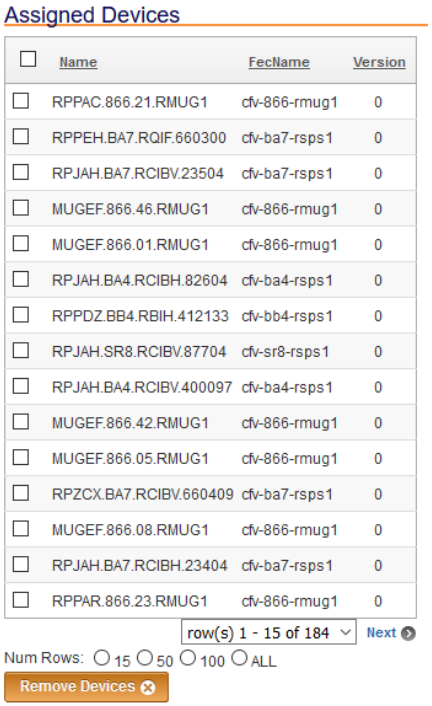
Example of RBAC rules

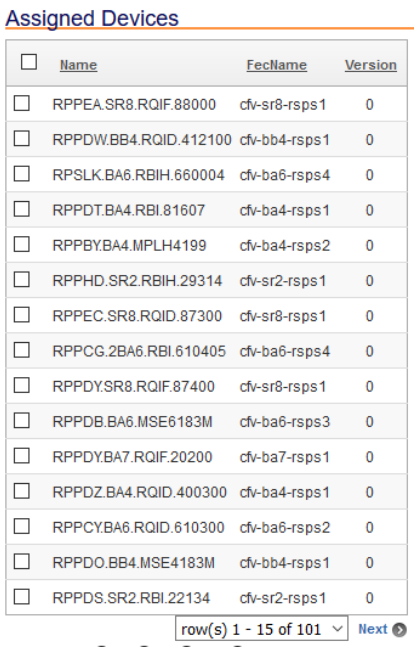
Device groups

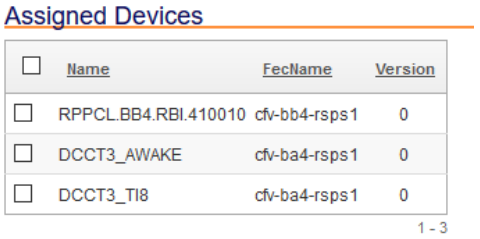












https://wikis.cern.ch/display/TEEPCCCS/libintlk+-+Interlock+library

PC Beam Interlock properties

Multi-ppm support

In the PS complex, the concept of ‘destination’ or ‘multi-ppm’ exists
Essentially every ppm user can have more than one definition, depending on ‘external conditions’
At the moment of execution, the actual configuration for a user that is played is determined by the external conditions

Full BIS support for multi-ppm is very heavy, thus instead the configuration should be made such that the output channels correspond to the different destinations
For example for the L4T.RBH.021

- Channel 1 = Destination DUMP
- Channel 2 = Destination PSB

Further background on the Destination (multi-ppm) concept can be found here

1. https://wikis.cern.ch/display/TEEPCCCS/libintlk+-+Interlock+library
2. http://proj-fgc.web.cern.ch/proj-fgc/gendoc/def/PropertyBIS.htm

Example: SPS Implementation (SR2)

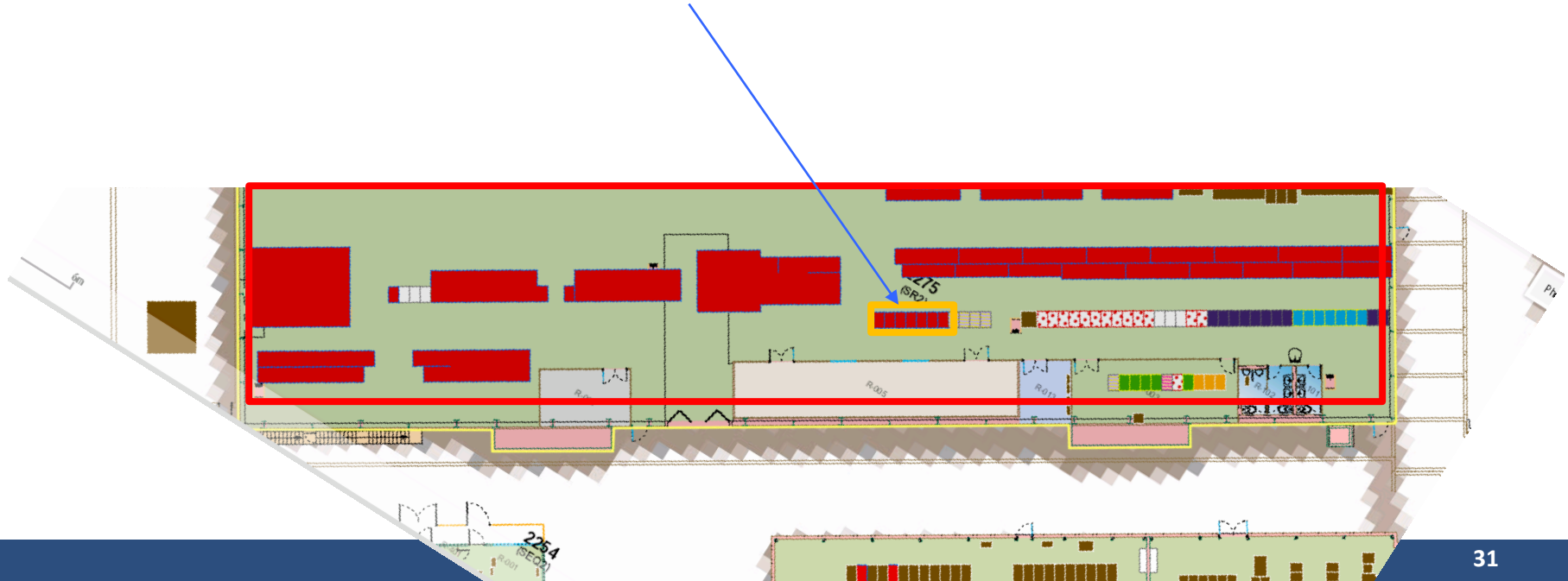
Example of implementation in SR2 @ LS2

i. 18x MACAO Power Converters (new)
ii. 16x (+ spares) Thyristor power converters (new electronics)
iii. 2x (+ spare) COMET_2P power converters (new)

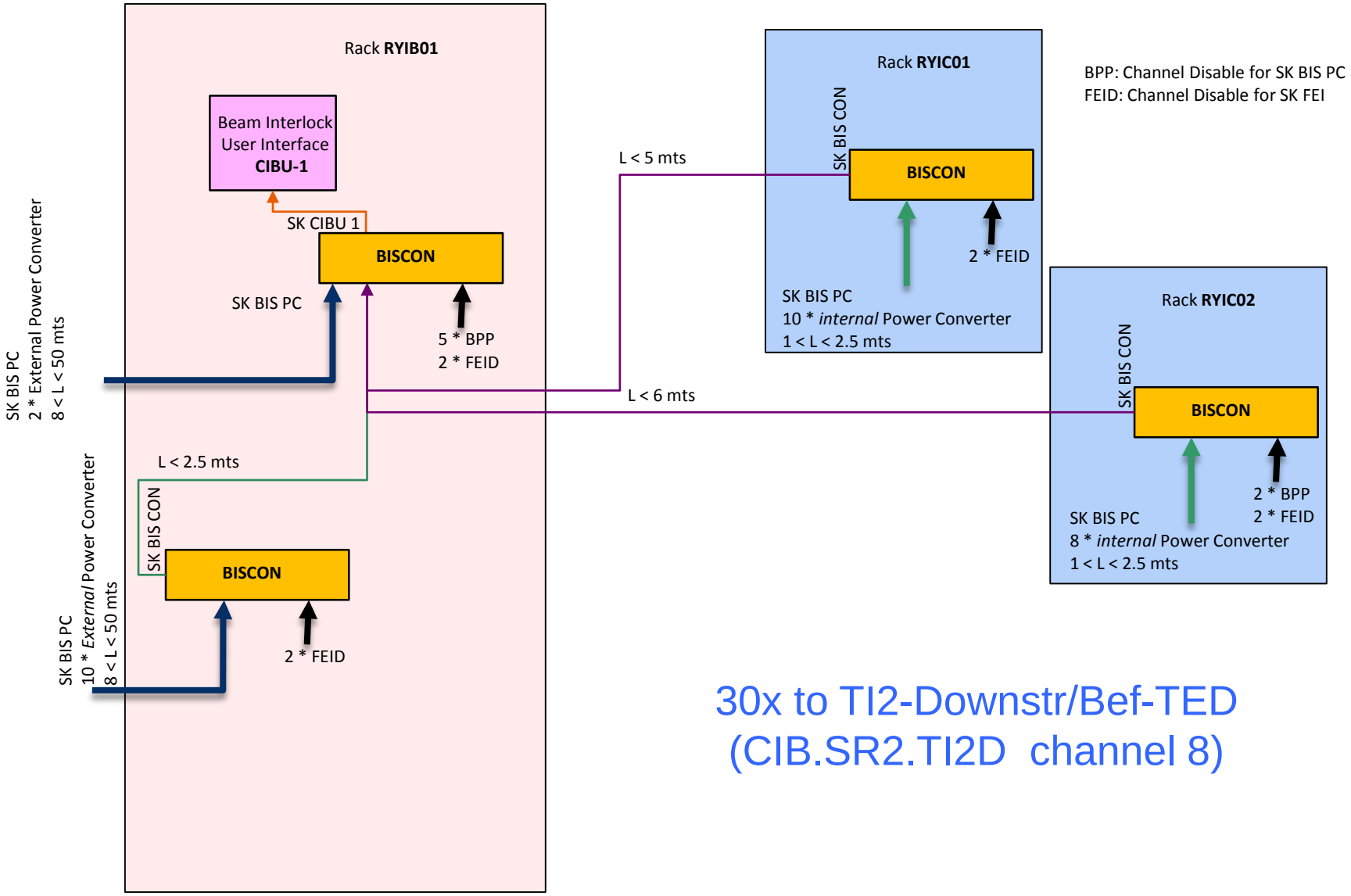
In total 36x power converters are connected to 2x BIS User Interfaces (CIBU)

i. 30x to TI2-Downstr/Bef-TED (CIB.SR2.TI2D channel 8)
ii. 6x to TI2-Downstr/Aft-TED (CIB.SR2.TI2D channel 9)

Control racks are next to MACAO racks



Example: SPS Implementation (SR2)



30x to TI2-Downstr/Bef-TED
(CIB.SR2.TI2D channel 8)