VME bus support plans in BE-CO

Javier Serrano
with help and materials from Adam Wujek and Tristan Gingold

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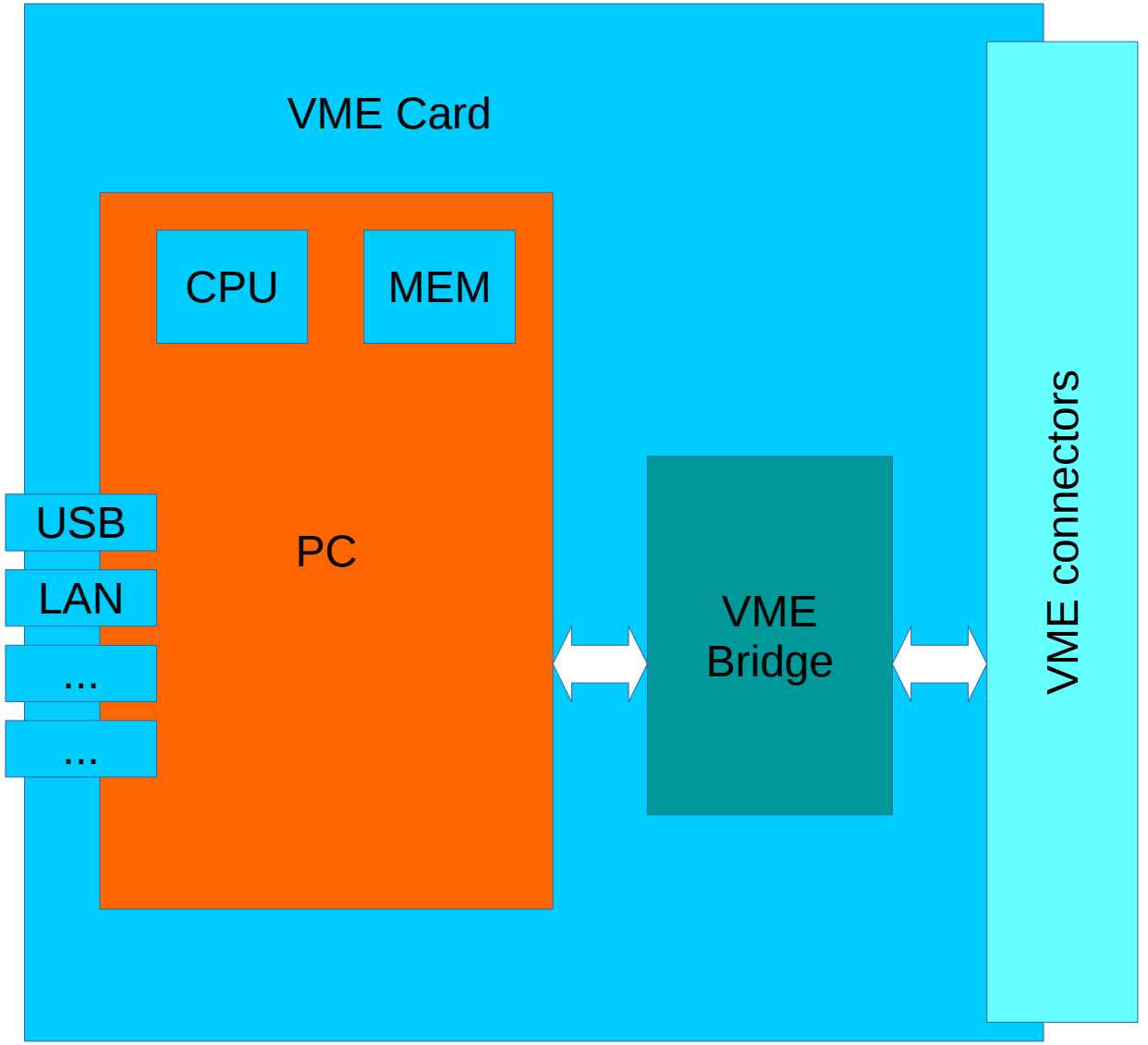
VME specification

- Developed in early 80's for Motorola 68k
  - The used standard is from late 90's
- Modular electronics
- Typically 1 master, many slaves
- Various transmission modes theoretical up to 320MB/s (see later for practical numbers).
  - Single access
  - Block transfer
  - Interrupts

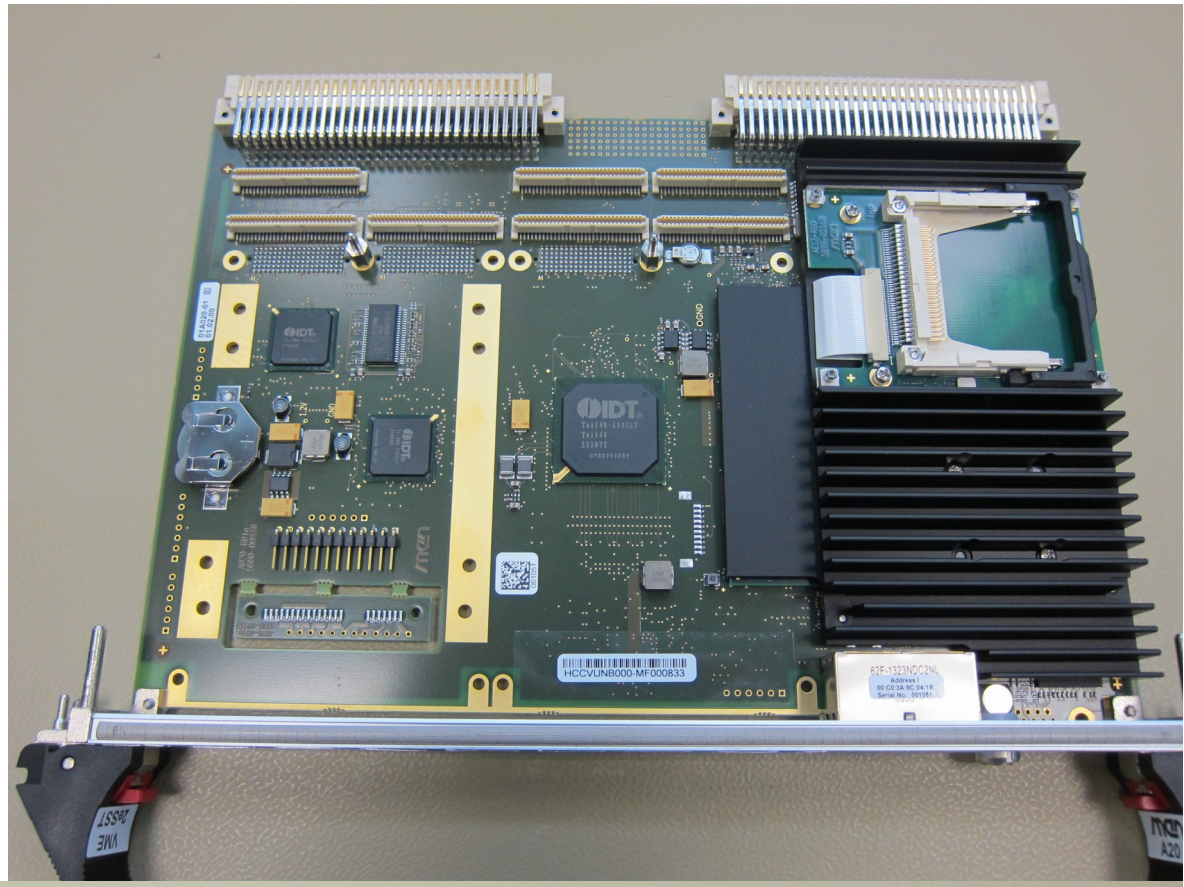
VME SBC Card

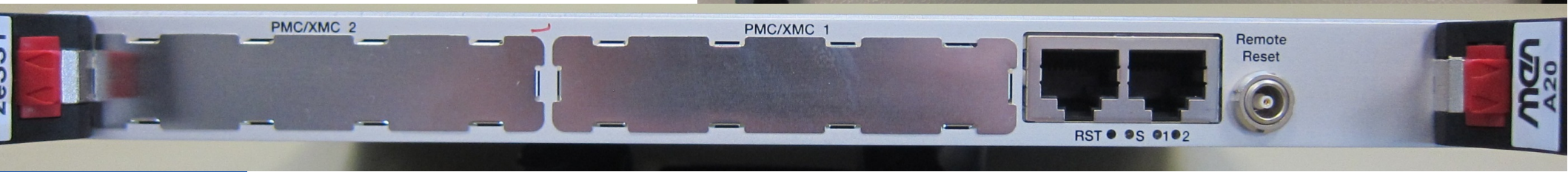


MEN A20

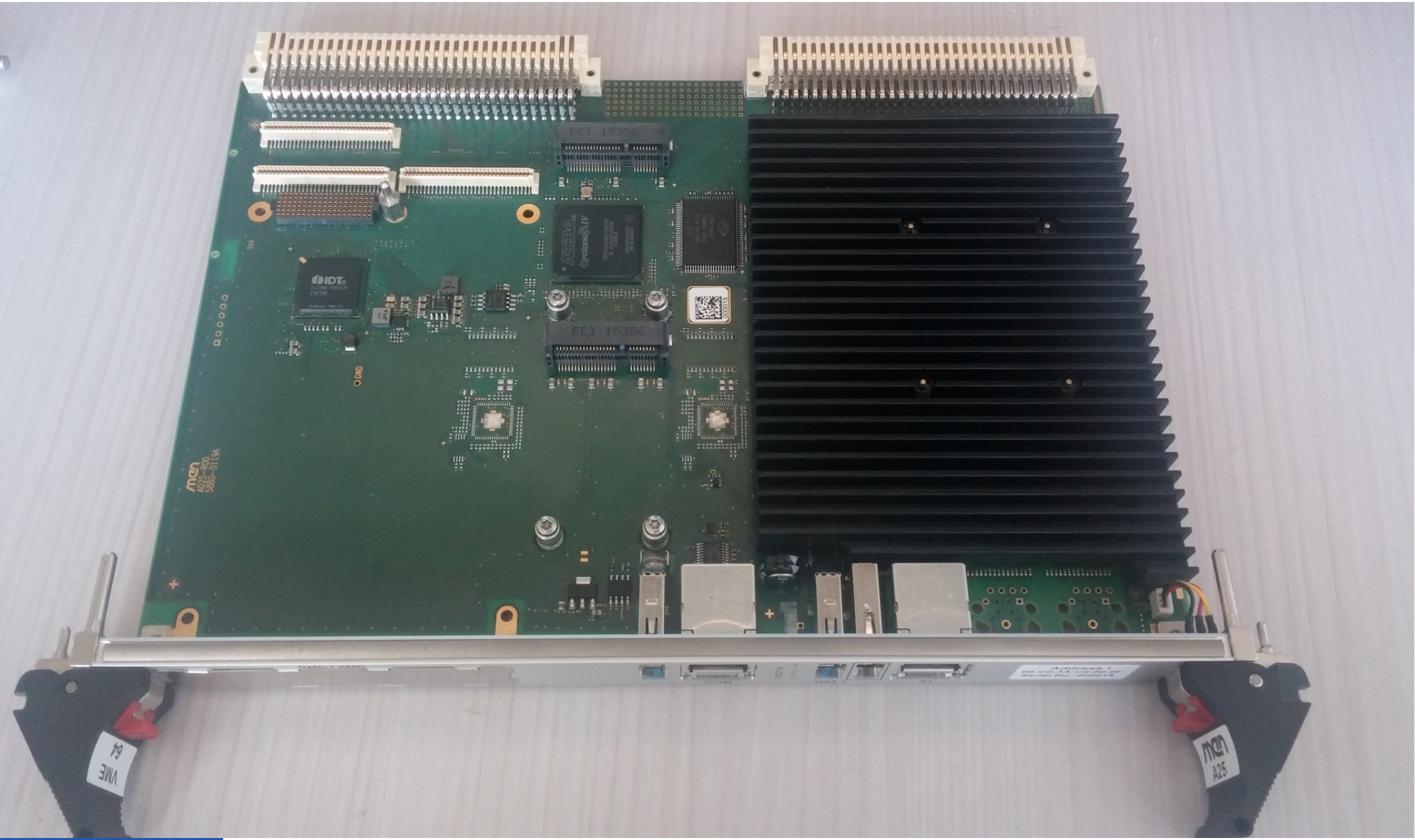
(not sold by MEN any more)

- Intel Core 2 Duo L7400 (1.5GHz)
- 1GB RAM
- Serial console
- 1GbE
- VME bridge based on TSI148
- Running Linux
- Optional 2x PMC slots
- Storage





MEN A25



MEN A25

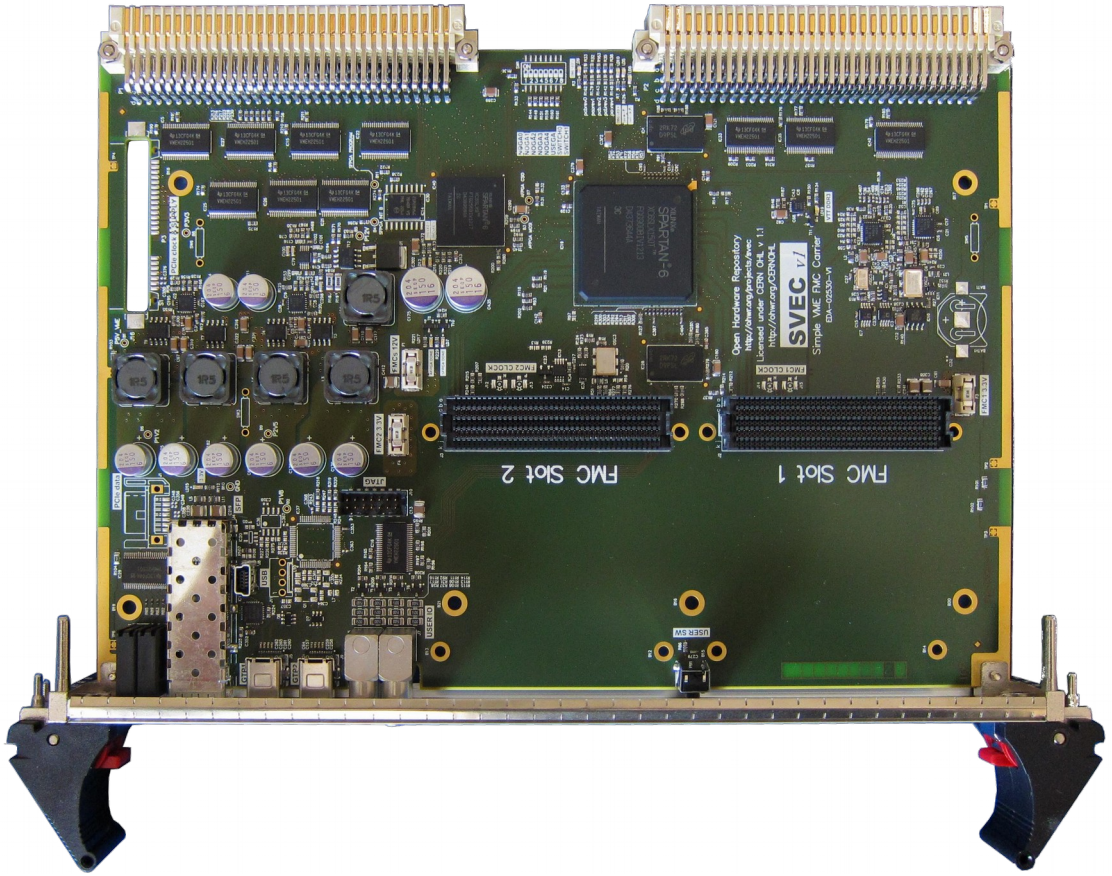
- Intel(R) Pentium(R) CPU D1519 @ 1.50GHz
  - 4 cores, hyper threaded
- 8GB of RAM
- Serial console
- 1GbE
- PMC/XMC slot (only one)
- VME bridge based on FPGA
- 2x USB 3.0 (requires CentOS 7)
- Running Linux (SLC6 and CentOS 7, no SLC 5)
- No lemo reset connector on the front panel

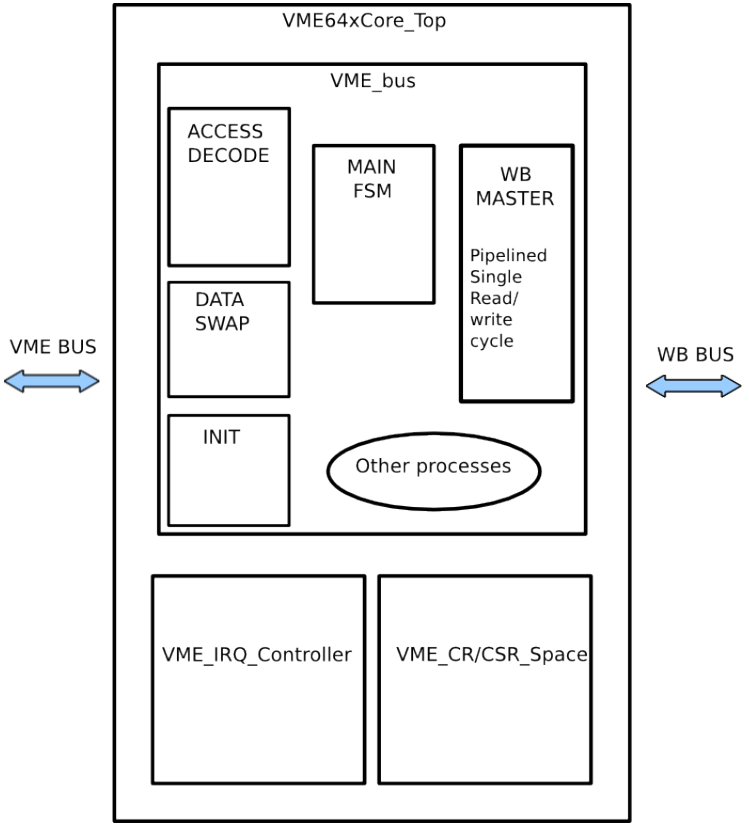
PCIe to VME bridge

- Open Source HDL implementation
- Intel Cyclone IV and can be ported to any other FPGA
- Solves PCIe-to-VME bridging problem
  - … till the end of VME lifetime
  - … for us and all other institutes (GSI, DESY)
- Uses ~30% of FPGA logic elements

- More features can be added if needed (e.g. 2eSST, 2eVME)

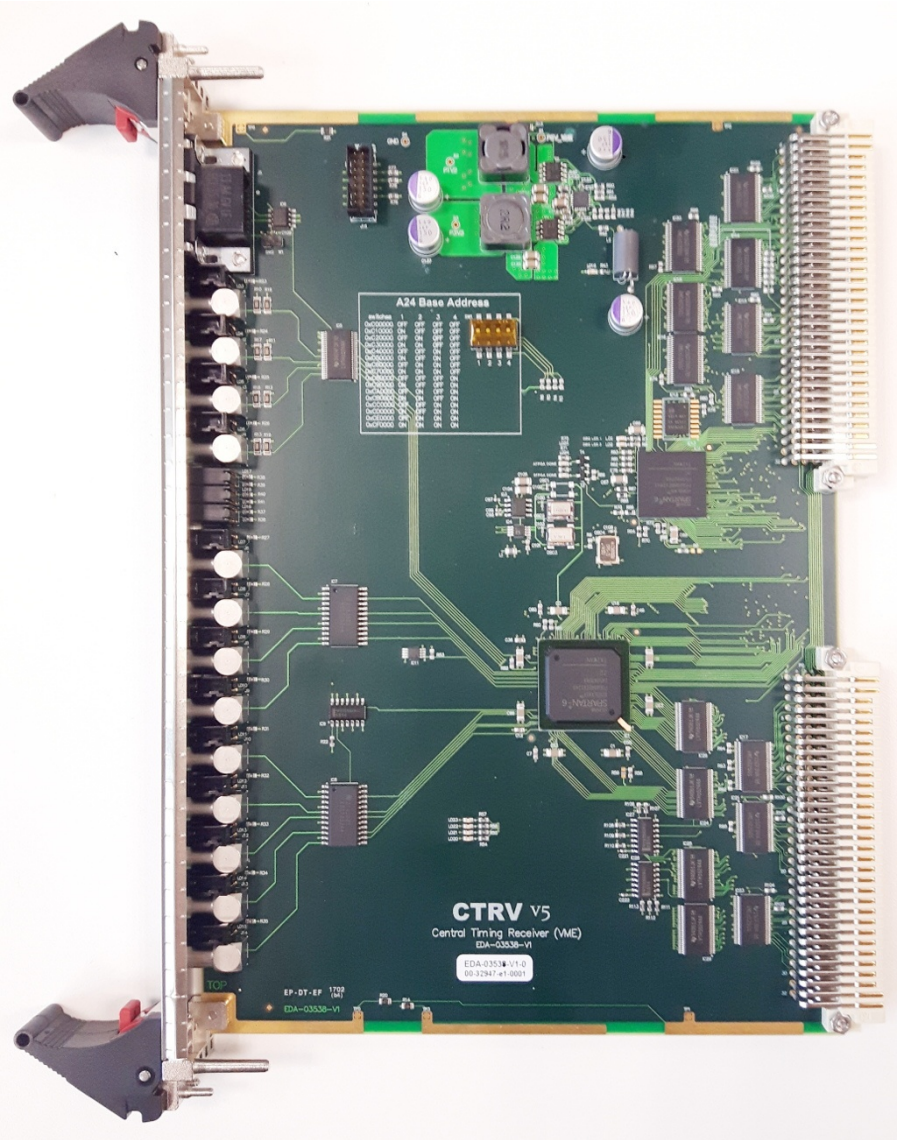
SVEC and VME64x HDL core





See also the Cheby project: https://gitlab.cern.ch/cohtdrivers/cheby/wikis/home

General Machine Timing Receiver



CTRV v5

Upcoming call for tender

- ELMA contract coming to an end
- Almost all ELMA stock committed for LS2
- New call for tender:
  - To be started now
  - Aiming at Finance Committee of end 2019
  - Hopefully prototypes mid-2020
- Come and see us early enough to discuss specific items like:
  - Redundant power supplies
  - Remote monitoring
  - Size variants and number of slots in each variant
  - Dimensions and mechanical details of Rear Transition Modules

Summary

- A25 – new CPU board to replace A20
- Open source implementation of VME bridge will reduce the risk of using VME in the future
- No plans to phase out VME before end of LHC operation. Support includes:
  - Crates
  - CPU boards
  - Slave reference designs. Currently:
    - SVEC board: https://www.ohwr.org/projects/svec/wiki
    - VME64x HDL core: https://www.ohwr.org/projects/vme64x-core/wiki
  - Timing receiver
- Upcoming call for tender for VME64x crates: get in touch with BE-CO to make sure your requirements are taken into account.

Reserve slide

BE/CO FEC Support for Accelerator Control – Roadmap

✳ : Platform Capability
✓ : Future Recommendation by BE/CO

TIME LINE FULL PLATFORM AVAILABILITY	2018 <-- LS2 --> 2019		2020 <-- RUN 3 --> 2023		
APPLICATION - CONSTRAINTS	VME	IPCs	VME	MTCA.4	IPCs
Digital feedback systems	✳		✳	✳ ✓	
Ultra-low jitter timing				✳ ✓	
High-end signal acquisition	✳	✳	✳	✳ ✓	✳ ✓
Multi-gigabit links between boards				✳ ✓	
Simple digital I/O	✳	✳	✳ ✓	✳	✳ ✓
Low to mid-range signal acquisition	✳	✳	✳ ✓	✳	✳ ✓
MIL-1553, WorldFIP		✳			✳ ✓
High Availability - Module Hot swap				✳ ✓	
High Power Dissipation / slot	✳		✳ ✓	✳ ✓	