BIS 2v0 Workshop

Thursday 15 November 2018

Wrap-up

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Personal Conclusions from Today

- Andrea: Availability during Run 1 & 2
  - 79 events tracked: 74 events maintenance, 4 events availability, 1 event blind failure (user side issue)
  - Most faults related to CIBD or Wiener power supplies: **Powering**
  - Failures put in availability matrix
    - Powering related failures are transparent for operation or < 1h
    - CIBF Weibull → recent replacement due to ageing
    - When does grey turn green? Action solves root of the problem (remove wrong type of fibre)
    - **No effect failure (decoupling capacitor) can cause many problems**, especially when they accumulate (Etienne)
  - Compared with 2005 predictions: number of false dumps according to expectations – about 1 per year → safety also OK
    - Some failures were not considered in the original system, so we are actually more reliable for the equipment considered (Markus)
  - Conformity of user connection is very important
    - More details later
  - BIS fault tracking to be improved – link to InforEam?

Operational Experience (Christophe) Examples

- Connection between different BIS systems (machines)
  - Many interfaces and lack of monitoring, three different history buffers, and most likely not sufficiently safe
- Decoding of timing information – not safe enough either
- User connections to backplane (B1/B2/Both/mask)
  - Found ways around, not clean
- Diagnostics for cyclic machines
  - Asynchronous update of GUI
  - Added cyclic view ,,,,history buffers. User != Destination…PM
- CIBF – too complex → connect directly to backplane?
- CIBT used for monitoring – merge with CIBM?
- CIBU connection to users
  - Not always conform: 26 % not conform before LS1- on the connection level, does not include within the user system

Feedback from Operation (Jorg et al.)

- BIS first operation in SPS in 2006 – BIS deployment still growing
- History buffers invaluable, including addition of timing events → possibly **put more machine information**
- Only tricky operational part is the re-arming LHC transfer lines after power cycles in the SPS complex: understanding
- BIS diagnostics for pulsed machines – also mentioned by Christophe
  - Difference between OP view and Expert view → compact
  - Mask ALL BLMs on the different BICs
  - Which are the active interlocks masked by SBF? (un)mask everything.
- Slow extraction SPS interlocking – new proposal
  - No key system to stop it, need to dump the beam but will miss next cycles for other destinations. Proposal for timing **destinations** (North Area, Ship) & SMP for SPS and possibly also act on some power converters. Ring Master and extraction BIS.
  - NEW CONCEPT for SPS.
  - **Check if this changes requirements for BIS2,** might affect mostly the SMP and BIS2 architecture
  - For after LS3
- Christophe: too much flexibility is not safe …
- No link between supercycle and BIS

HL-LHC Requirements (Daniel)

- Additional users form the new equipment
  - **Make a list asap so we know better the number of connections**
- No faster links to LBDS required
  - Not micros, for crab cavities considering gaining turns …
- Missing beam-beam kick with higher intensity bunches
  - Linking B1 & B2 becomes more critical: **link by hardware with less delay** (presently up to two turns delay)
  - Automatic linking above a certain total beam intensity and/or bunch intensity
  - LBDS to take into account the linking flag (Andrzej)?
  - **Acceptable Run III ?** – most likely (Ivan) → **to check, present linking is not safe!**
  - Linking in each BIS? **Only dump one beam at injection, link above injection**
  - Check on configuration differences to effect BB kick (Jorg)
- TCDQ levelling would require information / interlocking related to **bunch intensity → SMP v2**
- Interlocking of e-lens (not baseline) or quality of beam – doesn't effect BIS2 requirement on delay

BIS v1.23 (Raffaello)

- Consists of the BIS SFP system
  - Replaces CIBO daughter board, which has certain limitations
- Advantages
  - Larger power margin, low drift, off-the-shelf, hot plug, monitoring
- Add the False Frequency
  - Introduction of a false frequency clock in CIBM, the true frequency is only generated in one place
  - Worst case delay is 3.4 micros → Andrzej for present system use same window? Fast and slow detection. ABT responsibility. TSU doesn't stop the BIS at the moment, change for BIS2.
- Tested in the LHC on a parallel test loop
  - Including TSU and CIBDS
  - 1832 dump events analysed, 275 with full TSU data
  - about 40 non-standard events and 3 events presently under investigation
- Transmitted and received power very stable
  - Some interesting variation measurements
- **Ben: tested in non-normal situation, like switching one off, sending telegrams might avoid some of the gain compensation problems**
- Andrea: risk of generating true frequency….

External dependencies (David et al.): EPC

- LHC power converters connect to BIS via PIC, WIC, FMCM
- SPS & injectors: direct connections
- EPC moving to FGC technology all over, no mugef
  - SPS LS2 142 FGC3 devices through 9 BIS channels → mixture, call this BISCON = BIS Concentrator – use current connections to BIS
  - SPS LS3 all **228 FGC3 to connect to 18 BIS channels → BIS2**
- PS has no BIS (yet)
- Configure FGC for interlocking details & PPM
  - Edms doc
  - Two different standards of interlock output, also RS42
  - Test mode
- BISCON prototype exists in the lab – some remote monitoring, no timing, detailed info from FGC
- Wish list for BIS2
  - **Detect if system is connected**, with id number
  - Connection standards, test modes
  - 10 users in a 3U format, cost per channel low
  - **Build in 'time-on' counter** – see more details on slide 15

VME bus support (Javier)

- VME no signs of disappearing
- CPU
  - MEN A20 → MEN A25, pc with a PCIe to VME bridge
- SVEC and VME64x HDL core
- General machine timing receiver: CTRV
- **Call for tender for crates**
  - **ELMA contract coming to an end**
  - **Give any specific requirements, LIKE NUMBER OF SLOTS**
- VME support until end of LHC operation guaranteed
  - uTCA not the same level of support in the coming years
  - PCIexpress less mature than uTCA
  - Support of the crate important as well (Christophe) → **follow-up with CO for the tender**

BIS 2v0 Proposal (Ivan)

- New requirements
  - Concentrator, common interface to actuators, false frequency, linking the loops
  - Increase flexibility maskable/b1/b2/both etc.
  - Timing events as user inputs → reliability required for the injectors
- Packages
  - Make test of power cycling crates and sending packages in present system based on frequency
  - Tomasz: packets can affect reliability but packets have the advantage of bit error rates which give a pre-warning. For injectors timing etc. to be send as safety information – relation to SMP
    - On the frequency sent, can also have glitch counter to check on data quality…
- Keep VME, but new crates and new backplane
  - **Keep same connectors**
- CIBM/CIBX/CIBG/CIBDS improvements
- CIBU
- **Radtol design required?**
- SFP
- Interface to actuators - standardise
- CISV – provide our own board?
- Test benches and software to be upgraded
- Planning: LS3 for injectors starting one year later than for LHC

Discussion

- **Andrzej: Overview of all interlocked systems before starting BIS 2, look across all accelerators, BIS architecture over the complex - PS has no dump …**
- **Overview on what to do below SPS – timing included in the BIS? PSB has a lot included in the SIS – global analysis. BIS – SMP – Timing – Loops – External conditions. Reliability requirements.**
- **One solution for everything still valid ?**
  - **If injectors are to act on the next cycle (does not need to be fast) and it is less safety critical, could we envisage a different system from the BIS, fast PLC solution?**
  - **Where does timing come in? → Destination**
- **SPS North Area is between the worlds – also destination dependent but want to dump as well**

What is next ?

- Coming soon:
  - Half day workshop on injector interlocking (**new!**)
  - Half day workshop on SMP v2
- Paper work
  - MPE group Steering Board road map
  - Technical specification confirming technical choices
    - Comments and approval by most of you

Many thanks to all speakers and participants