Cavity BPM at CLEAR

A. Lyapin, M. Cargnelutti, M. Wendt

RHUL/iTech/CERN

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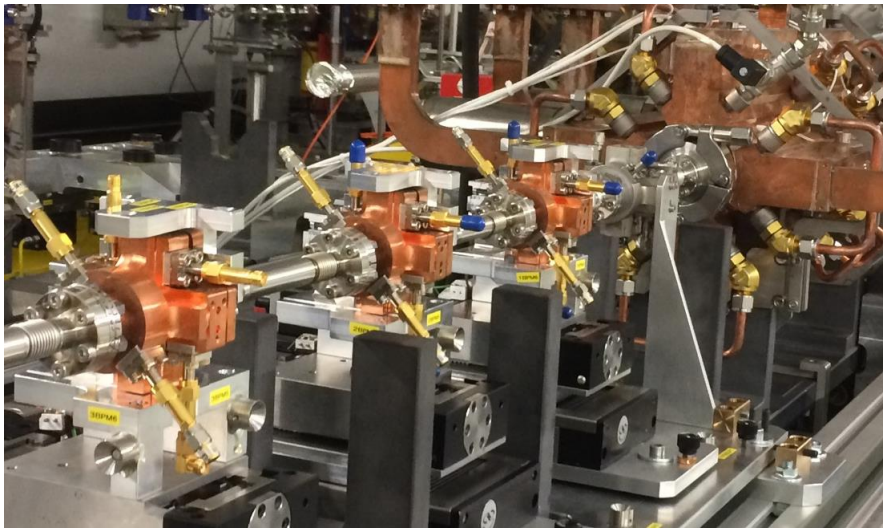
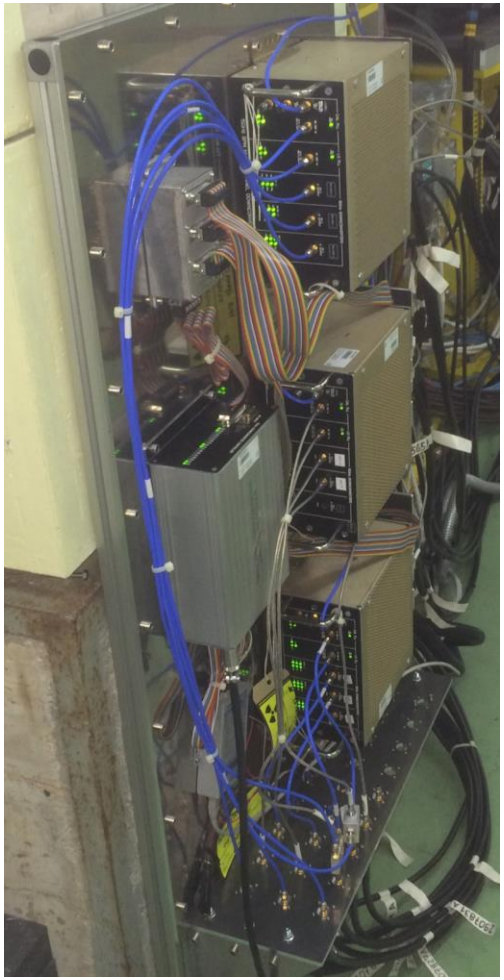
Outline

- Present Cavity BPM system in CLEAR
- Experience with the present system
- Proposed future system:
  - RF down-converter
  - Signal processing
  - Digitiser
- Phased approach to the upgrade
- Conclusions

Present CBPM system @CLEAR

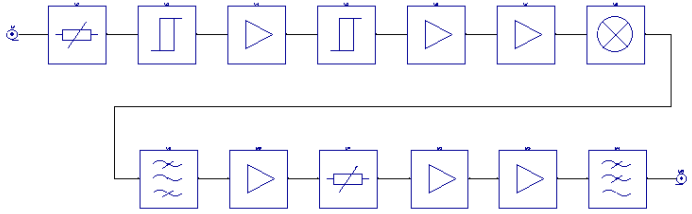
- A demonstrator system for CLIC main beam cavity BPMs
- High spatial (50 nm) and high temporal (50 ns) resolution needed for beam based alignment, wakefield-free steering and *online dispersion correction* via energy chirped trains
- 3x 15 GHz low-Q (fast decay) position cavities
- Downconversion to a lower frequency for digitisation
- Transverse movers for calibration and alignment



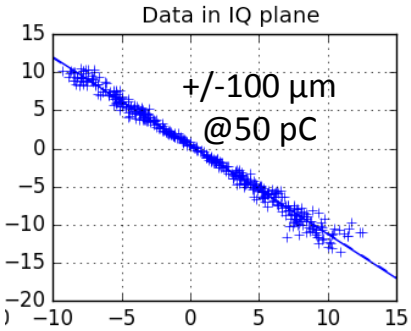


Experience with the present system

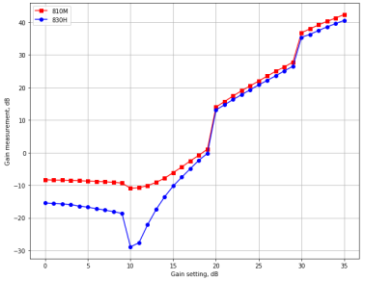
- A number of issues found, some critical to performance:

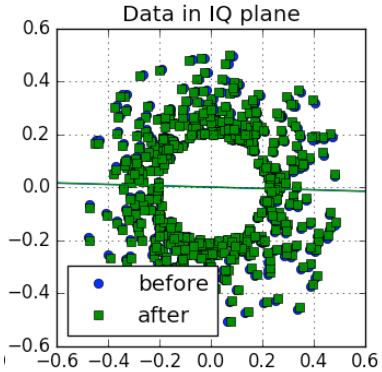


- Electronics too complex
  - Excessively high gain
  - Attenuation resulted in increased noise
  - Poor linearity
  - Radiation hardness issues



- Electronics control issues
  - Impossible to use the optimal setting
  - Now fixed with a new control

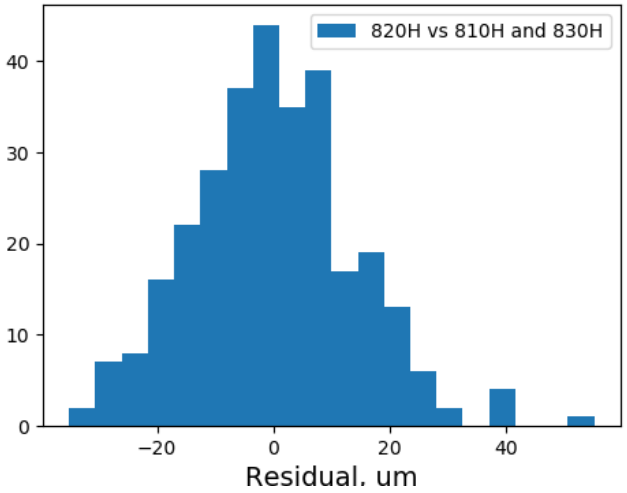


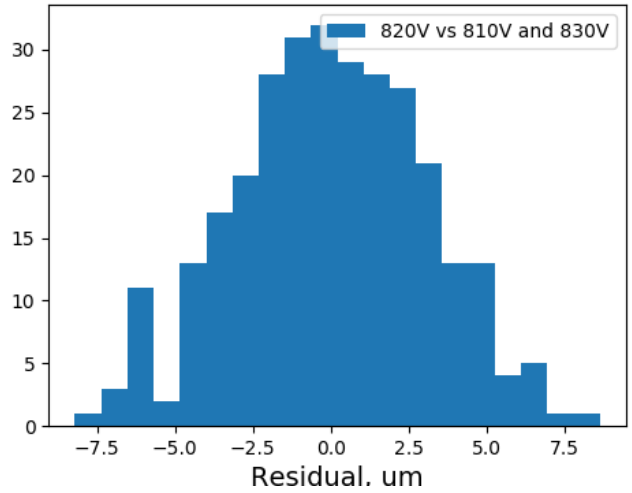


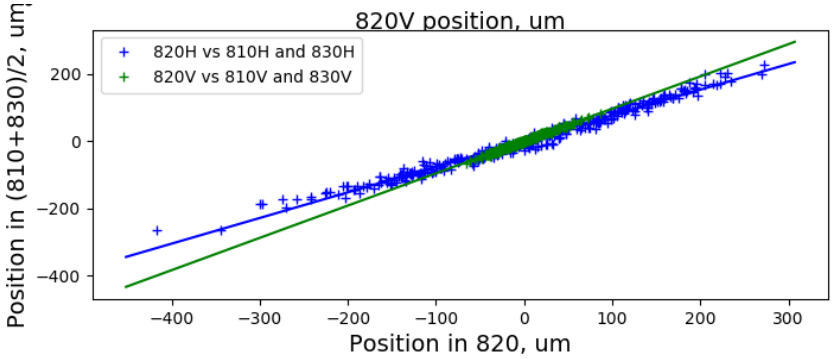
- ADC clocks randomly go out of sync
  - Use lower bit resolution digitiser
  - Resolution limited to 1-2 μm

Experience with the present system

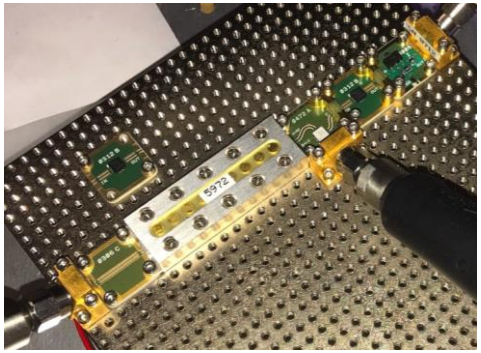
- The best resolution measurement around 2 μm, as expected given the limitations

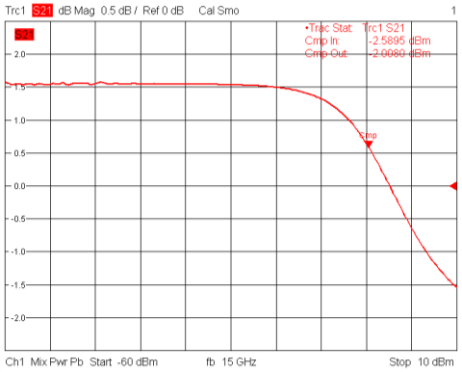


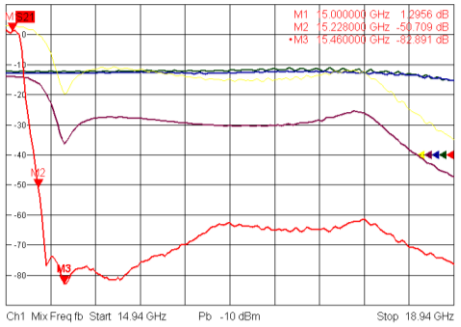




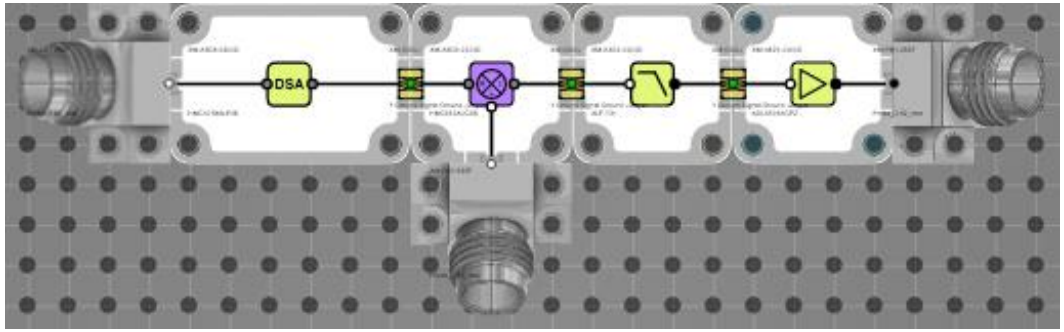
Proposed future system: RF downconverter

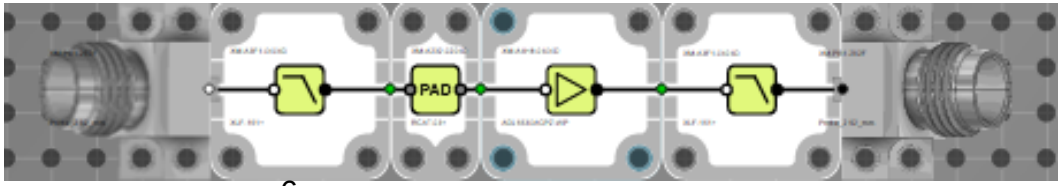






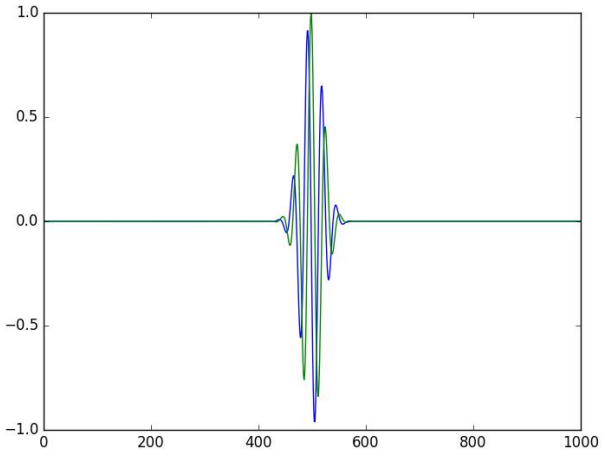
- Same single-stage downconverter concept, but no excessive gain, linearity important
- Use modular “RF Lego” approach by XMicrowave
- Minimize control: only front-end step attenuator is controllable, needed for high charge operation with bunch trains
- Use rad hard voltage regulators (found to be most sensitive in the old system)

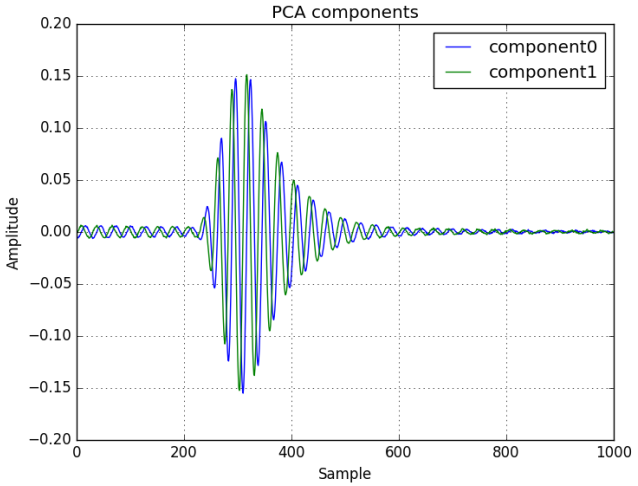




Proposed future system: Signal processing

- 2 types of analysis tried so far: Digital Down-Conversion (DDC) and Principal Component Analysis (PCA)
- In both cases we can use a basis of 2 windowed orthogonal sin/cos-like signals to map the amplitude and phase of the position signals corresponding to a known offset introduced during calibration
- DDC: Gaussian window, positioned arbitrarily; PCA: Signal-derived window
- We've been concentrating on DDC as it is robust, better understood and some corrections, such as for timing changes, are possible, although PCA can deliver higher resolution
- Both algorithms can be accelerated using FPGA-based processing
- In addition, can use iTech-developed power measurement based method

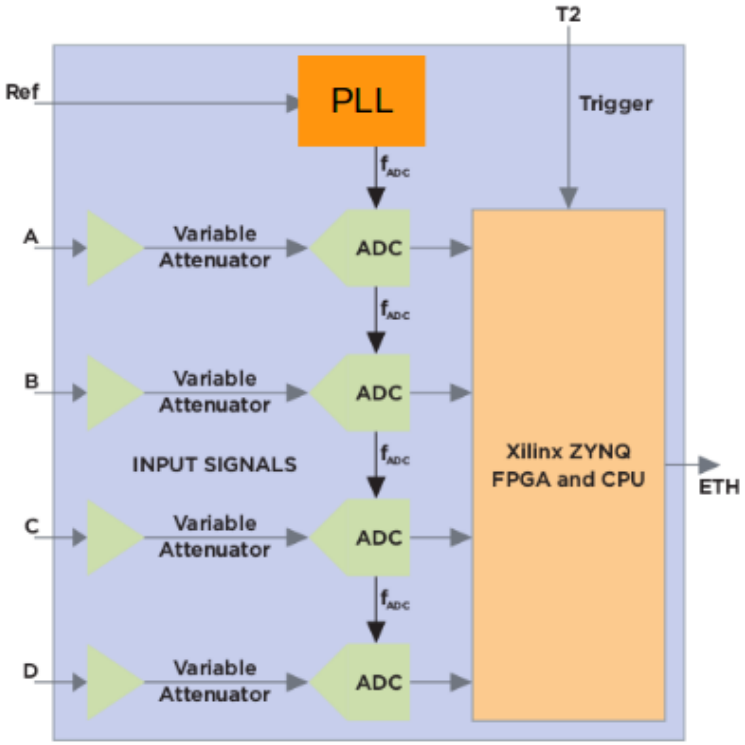




Proposed future system: Digitiser

Libera Digit 500 – AC coupled

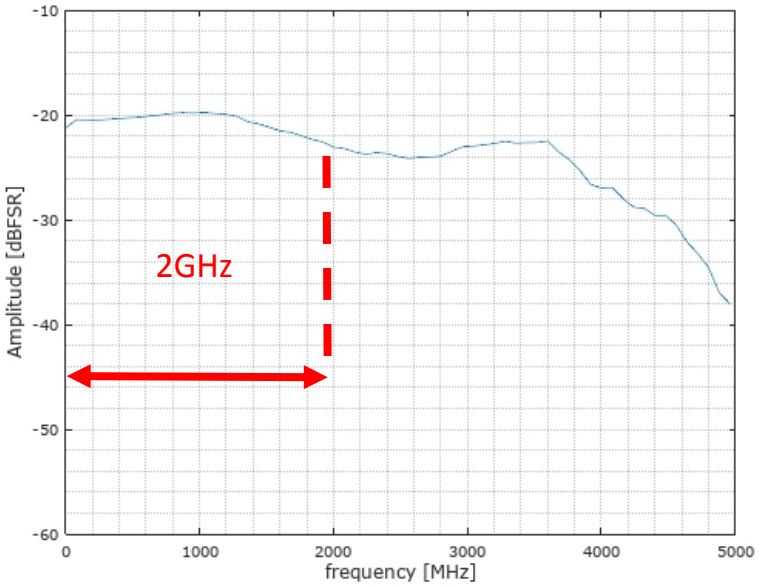
- 4 Channel AC coupled Digitizer
- ADC: 500MSps – 14 bit
- Bandwidth: 1MHz – 2GHz
- 32 dB variable gain
- Segmented memory with up to 500M ADC samples per channel
- Network attached



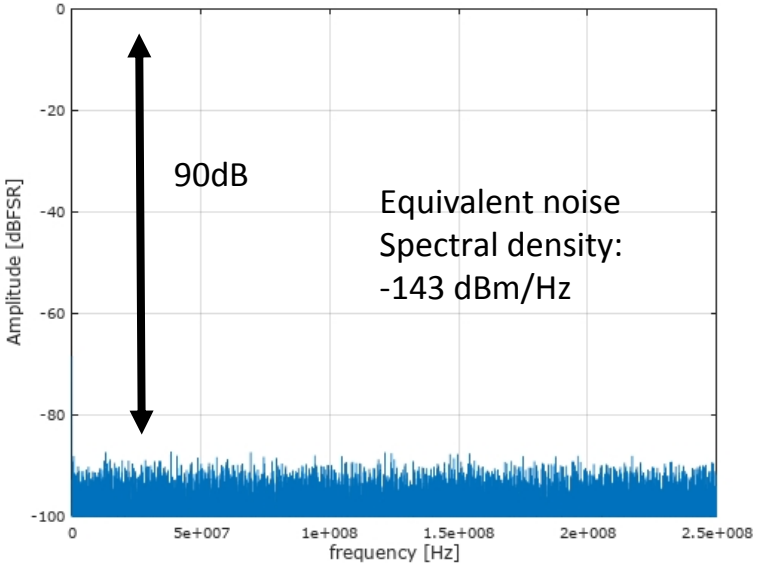
Proposed future system: Digitiser

Digit 500 Performance

Bandwidth measurement



Noise floor measurement



- Terminated inputs (50Ohm)
- Internal attenuation: 32dB

Proposed future system: Digitiser

Project phases

PHASE 1: Proof of principle

- New DWC and Digitizer on 1 CavityBPM
- ADC Data acquisition and Offline post-processing
- Standalone system (not integrated in CERN controls)

Deliverables

- Validation of DWC and Digitizer
- First performance assessment
- Data processing confirmation

Proposed future system: Digitiser

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PHASE 2: Online standalone system

- New DWC and Digitizers on 3 CavityBPMs
- ADC Data acquisition and online processing (SW)
- Standalone system (not integrated in CERN controls)

Deliverables

- Validation of DWC and Digitizer
- First performance assessment
- Data processing confirmation

- 3 BPM system
- Assessment of XY resolution
- Calibration confirmation

Proposed future system: Digitiser

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PHASE 3: Real-time integrated system

- ADC real time processing within the FPGA
- Integration in CERN controls

Deliverables

- Validation of DWC and Digitizer
- First performance assessment
- Data processing confirmation

- 3 BPM system
- Assessment of XY resolution
- Calibration confirmation

- Online system, ready for operation

Proposed future system: Digitiser

Project phases

Proposed timeline

PHASE 1: Proof of principle

- New DWC and Digitizer on 1 CavityBPM
- ADC Data acquisition and Offline post-processing
- Standalone system (not integrated in CERN controls)

→ April – May 2019

PHASE 2: Online standalone system

- New DWC and Digitizers on 3 CavityBPMs
- ADC Data acquisition and online processing (SW)
- Standalone system (not integrated in CERN controls)

→ July – Nov 2019

PHASE 3: Real-time integrated system

- ADC real time processing within the FPGA
- Integration in CERN controls

→ Jan 2020 – May 2020

Conclusions

- The current CBPM system at CLEAR has shortcomings in the **analog front end** (gain, linearity) and the **digitizer** (ADC resolution). The RMS position resolution of the system is limited to 2um.

- A **new system** is proposed with a new downconverter based on modular RF components and a commercial wideband digitizer. The ADC data acquired can be processed with two separate methods (Digital Down Conversion and Principal Component Analysis).

Conclusions

- The current CBPM system at CLEAR has shortcomings in the **analog front end** (gain, linearity) and the **digitizer** (ADC resolution). The RMS position resolution of the system is limited to 2um.

- A **new system** is proposed with a new downconverter based on modular RF components and a commercial wideband digitizer. The ADC data acquired can be processed with two separate methods (Digital Down Conversion and Principal Component Analysis).

- The electronics upgrade is proposed through a **three-phase project**, starting from the validation of each separate component and progressing with incremental integration with the goal to deliver an online operational system at the end of the project.