Simulations of the sensor design for CLICTD

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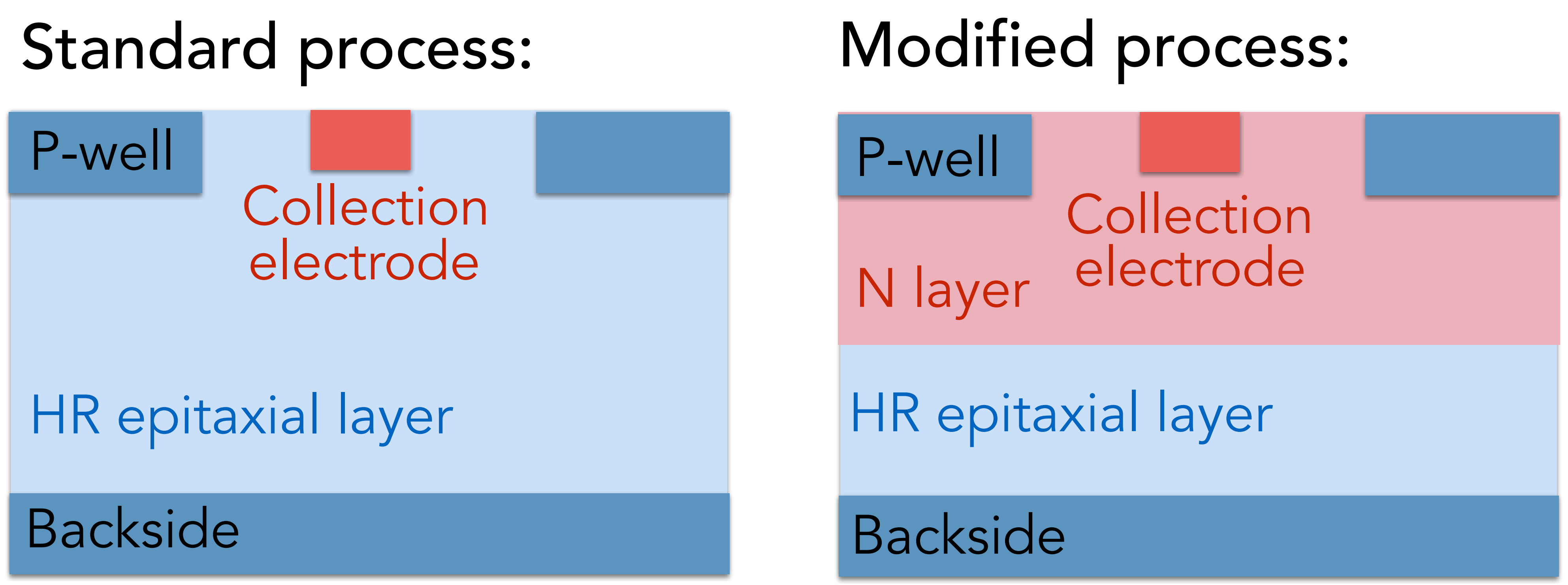
CLIC Workshop, January 2019

A fully monolithic HR-CMOS CLIC tracker chip - CLICTD

Promising results of 180 nm HR CMOS imaging process:



Full analogue performance for pixel size of 28 μm x 28 μm promising to meet requirements for CLIC tracker:

CLICdp-Pub-2018-004

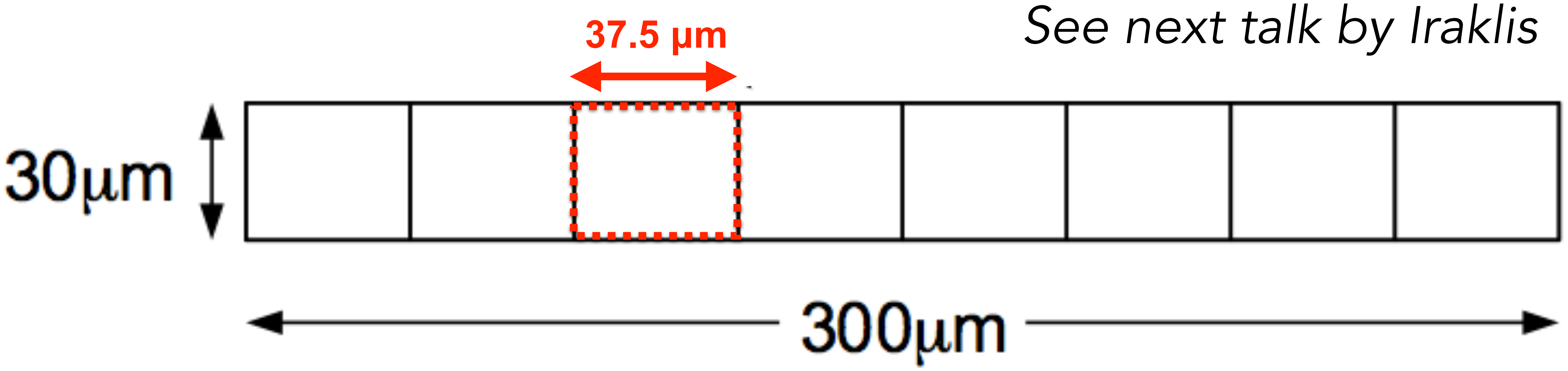
- Spatial resolution < 7 μm
- Timing resolution ~ 5 ns
- Efficiency > 99%

Design of fully monolithic CLIC tracker chip:

- Pixel segmented in high granular sub pixels to maintain fast charge collection while reducing digital logic
- Pixel size of 30 μm x 300 μm
- Sub pixel size of 30 μm x 37.5 μm

Fixed pixel and sub pixel layout of CLICTD:

See next talk by Iraklis



Which process variant?

Standard process: | Modified process: | Gap along both dimensions: | Gap along z-dimensions:

No uniform depletion:
—> Slower charge collection
—> More charge sharing
—> Superior spatial resolution

Uniform depletion:
—> Faster charge collection
—> Reduced charge sharing

Avoid low field regions:
—> Even faster charge collection
—> Less charge sharing
—> Superior timing resolution?

Compromise:
—> Faster charge collection in z
—> Less impact on charge sharing and spatial resolution in rΦ?

Sensor-simulation strategy

3D electrostatic TCAD

3D transient TCAD

Monte Carlo Allpix Squared

Detailed fully self consistent solution to study time resolved response

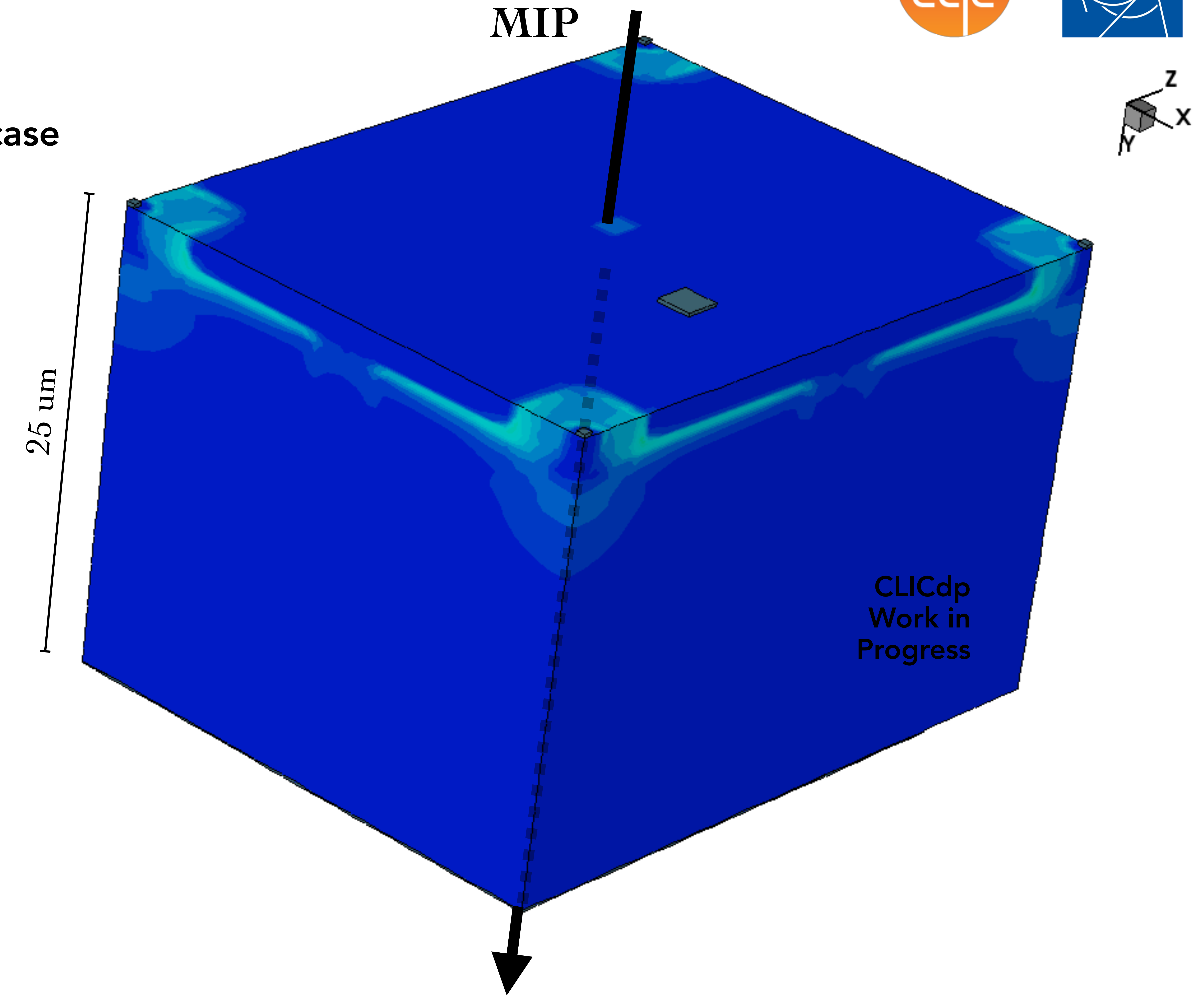
High statistics performance evaluation

3D TCAD simulation setup

Simulation of pixel edge to benchmark worst case scenario in view of timing performance:

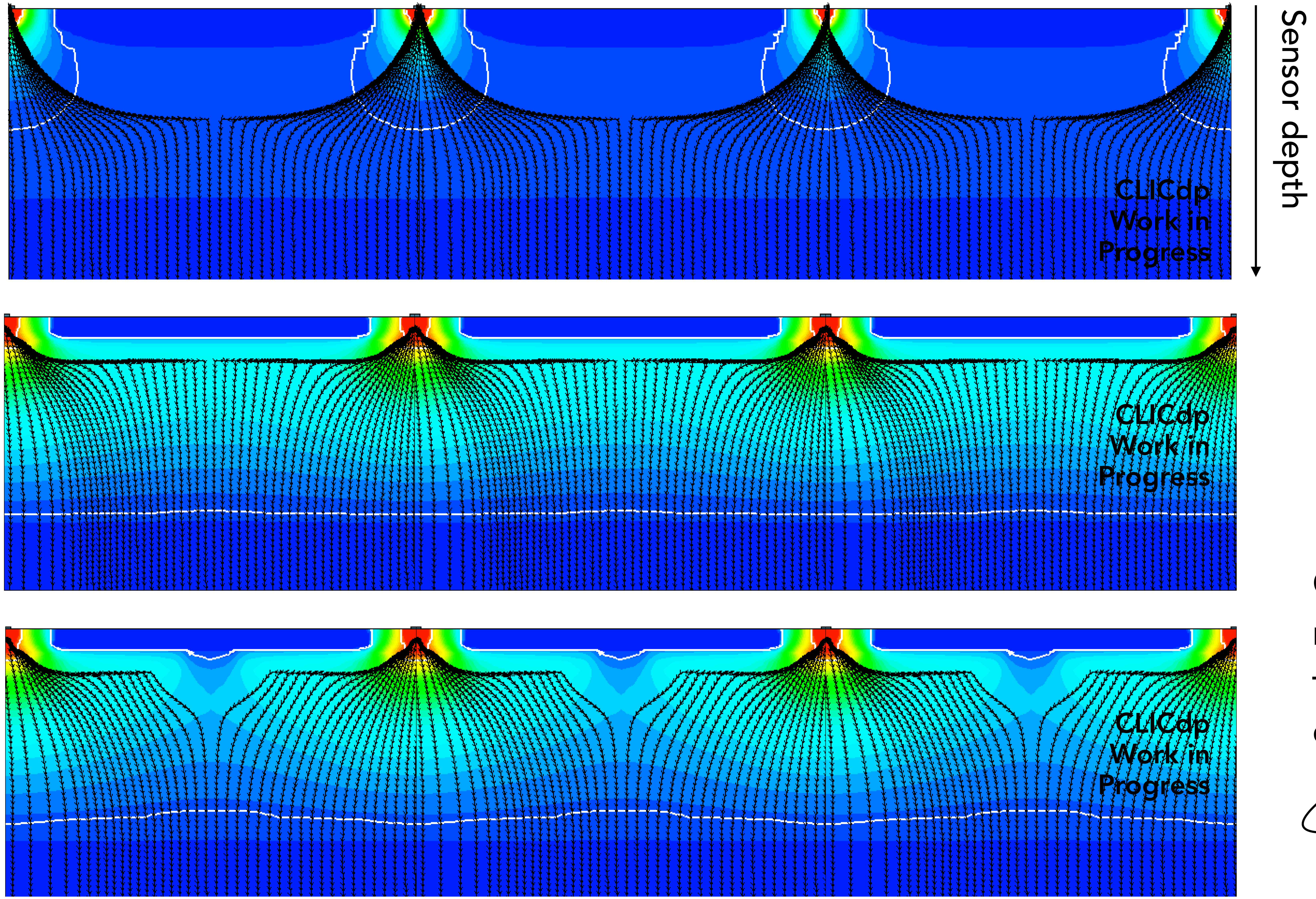
- Lowest electric field regions
- Slowest charge collection

↳ ***Detailed fully-self consistent solution (impact of charge carriers on electric field, induced current, ..)***



Electrostatic solution - why to make a gap in the N layer?

Electrostatic potential:



Standard process:

Modified process:

Modified process **with gap** in n-layer:

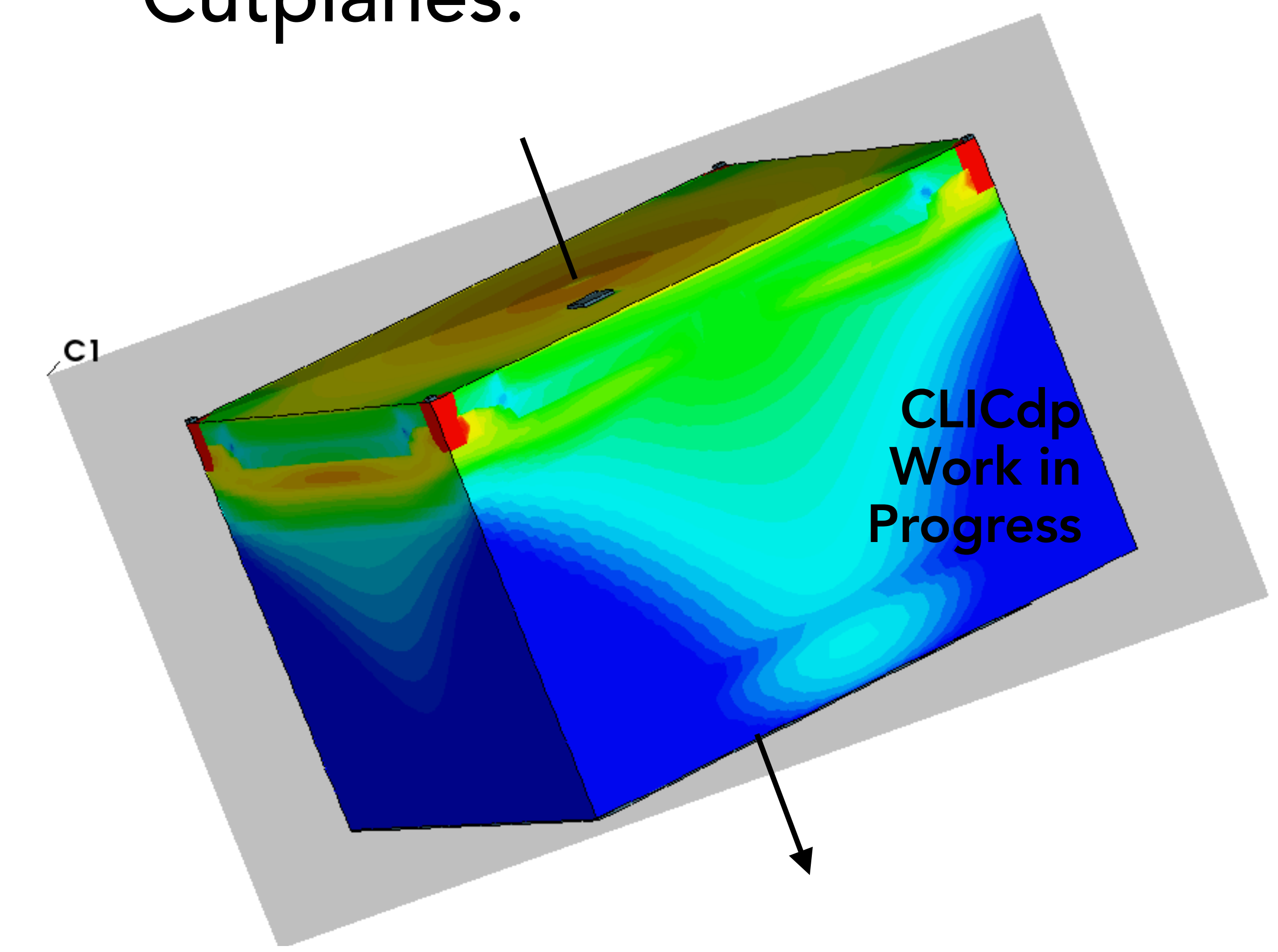
Black arrows mark electric field streamlines

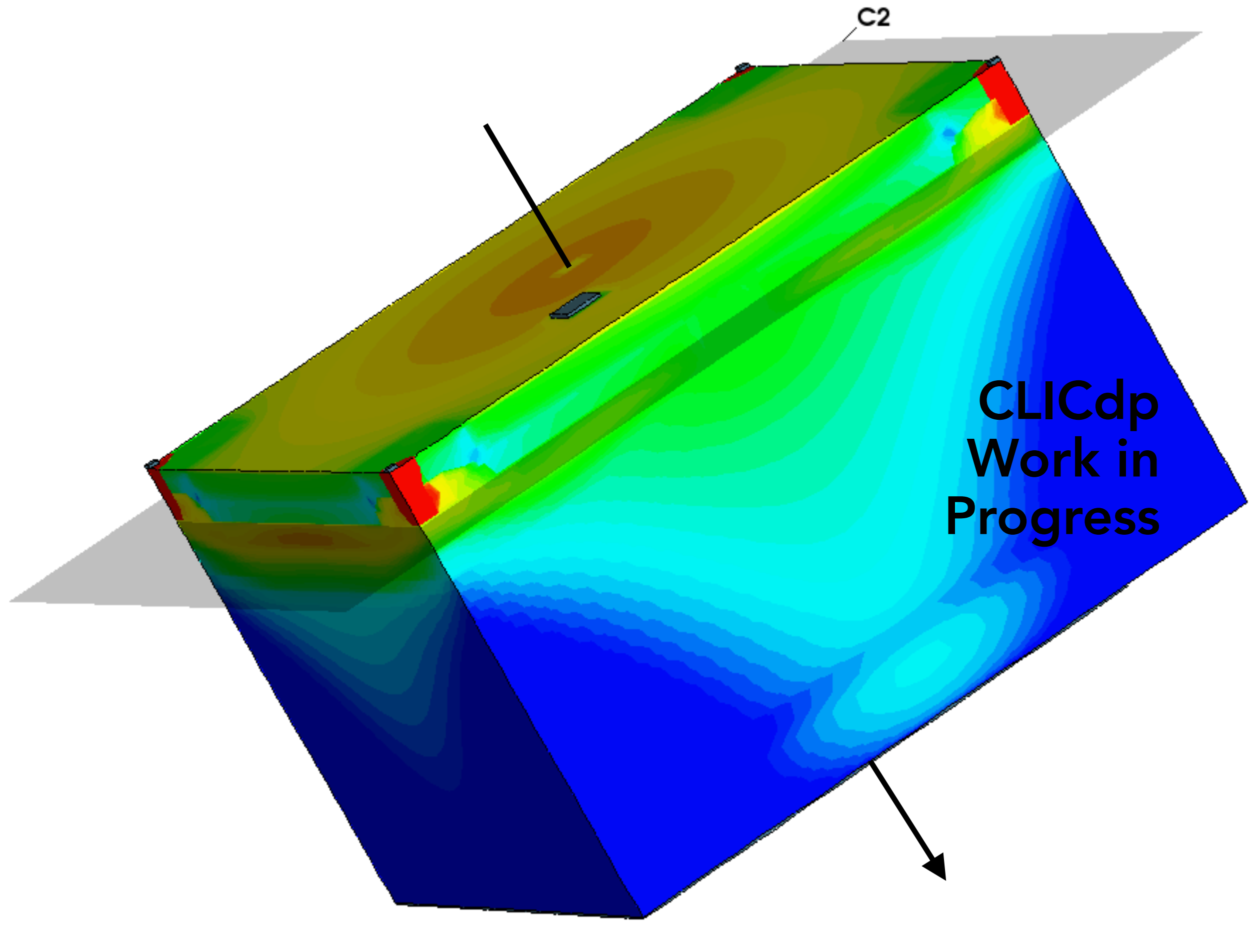
Gap in the N-layer for the modified process bends the field lines towards the collection electrode

↳ Faster charge collection

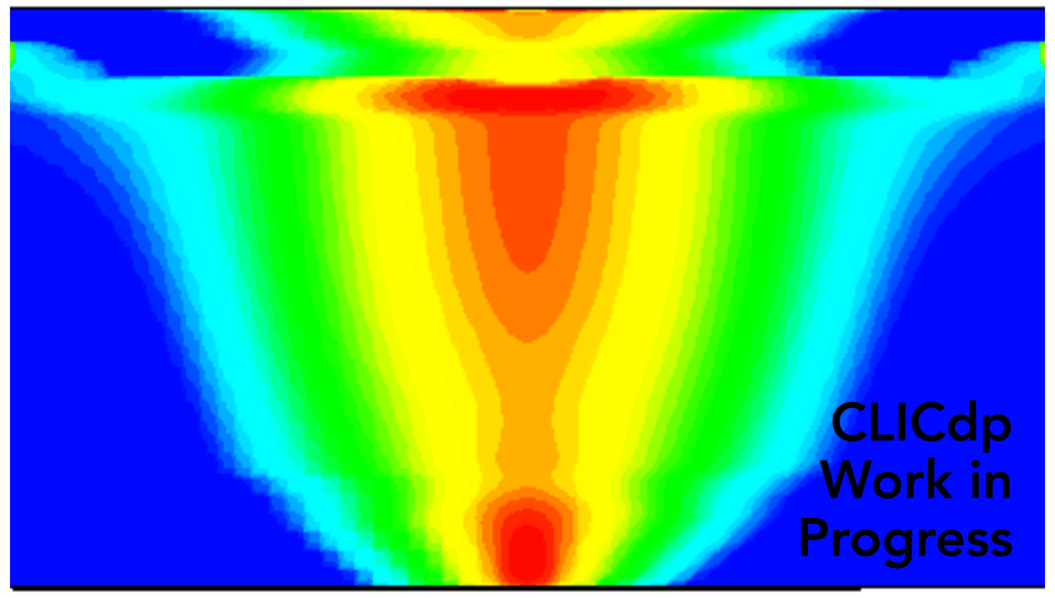
Transient / electron density 1.5 ns after particle incident

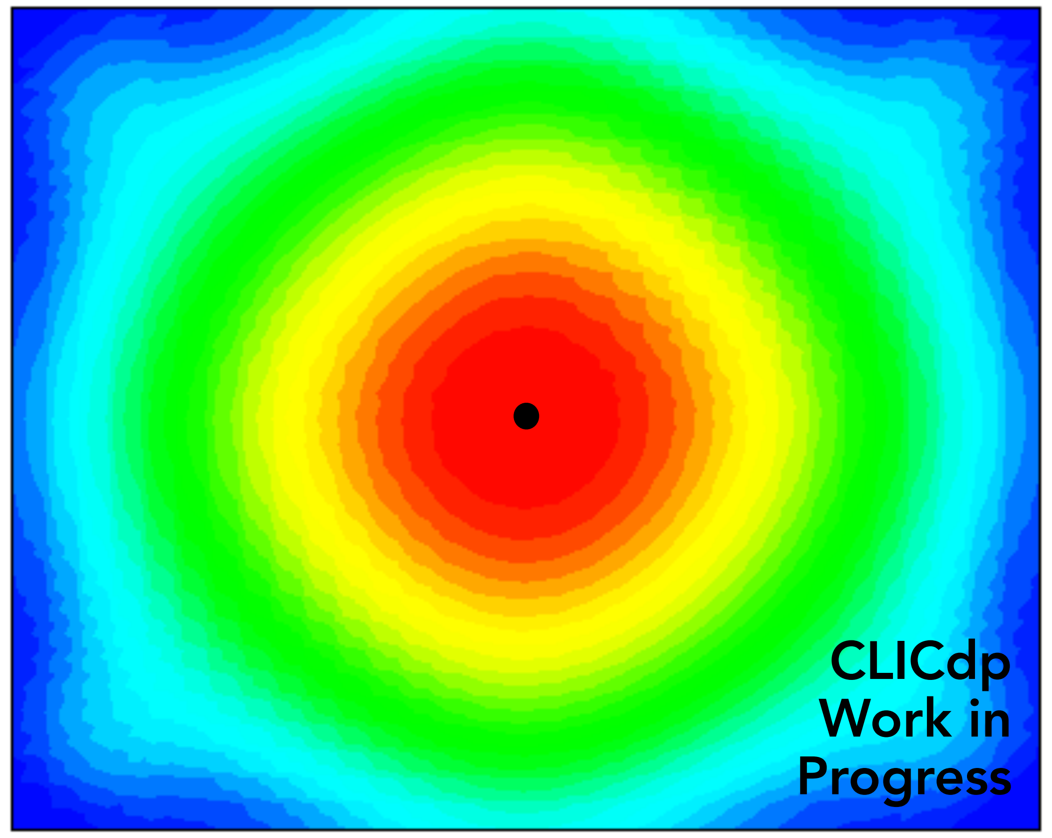
Cutplanes:



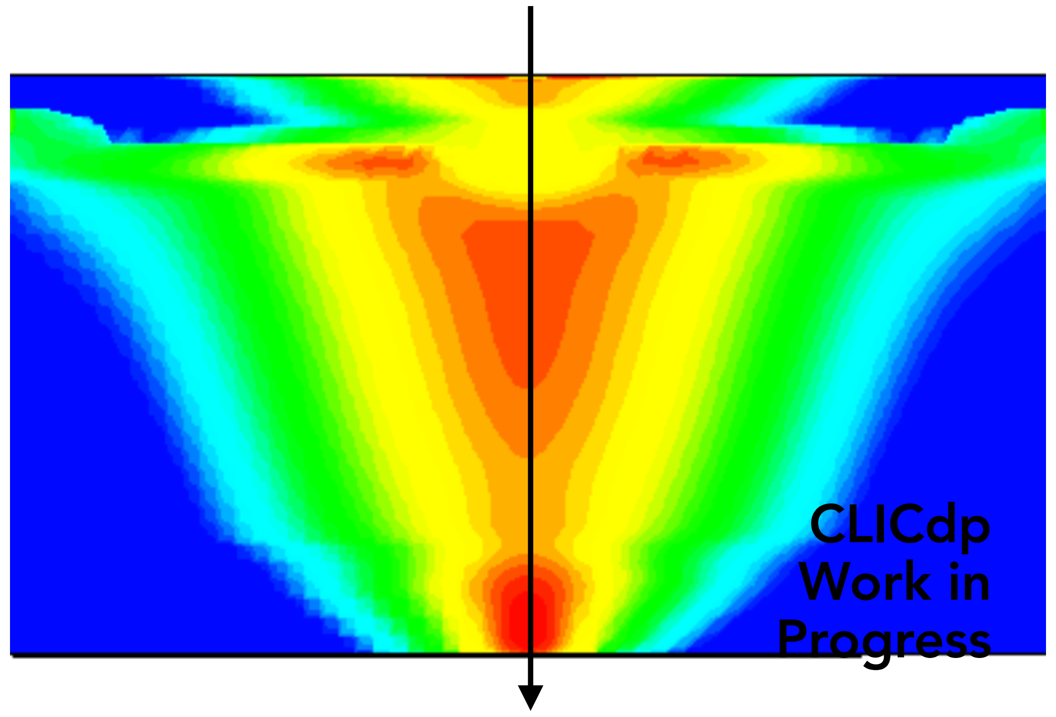


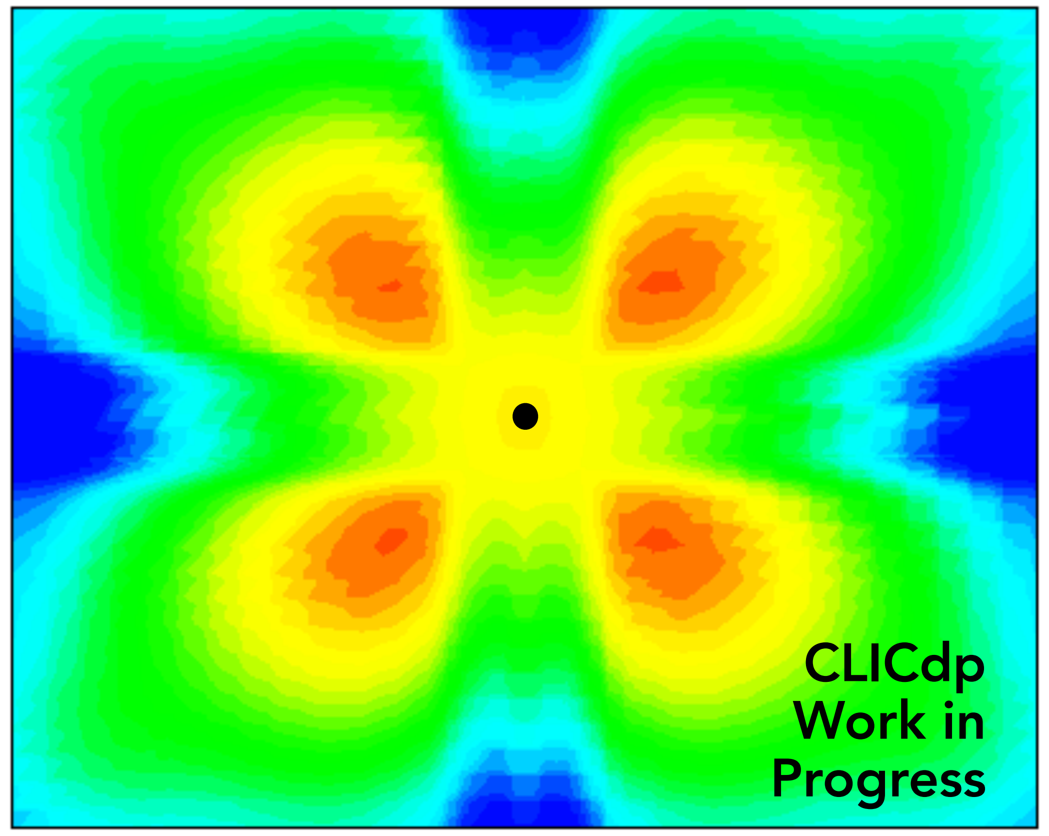
Modified process:



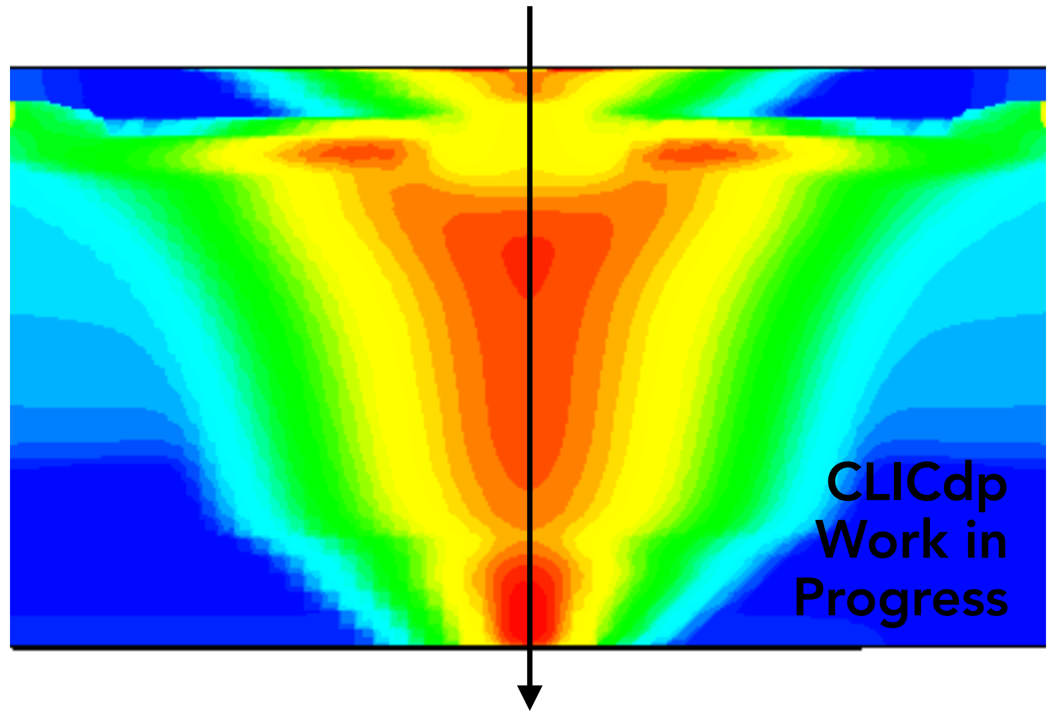


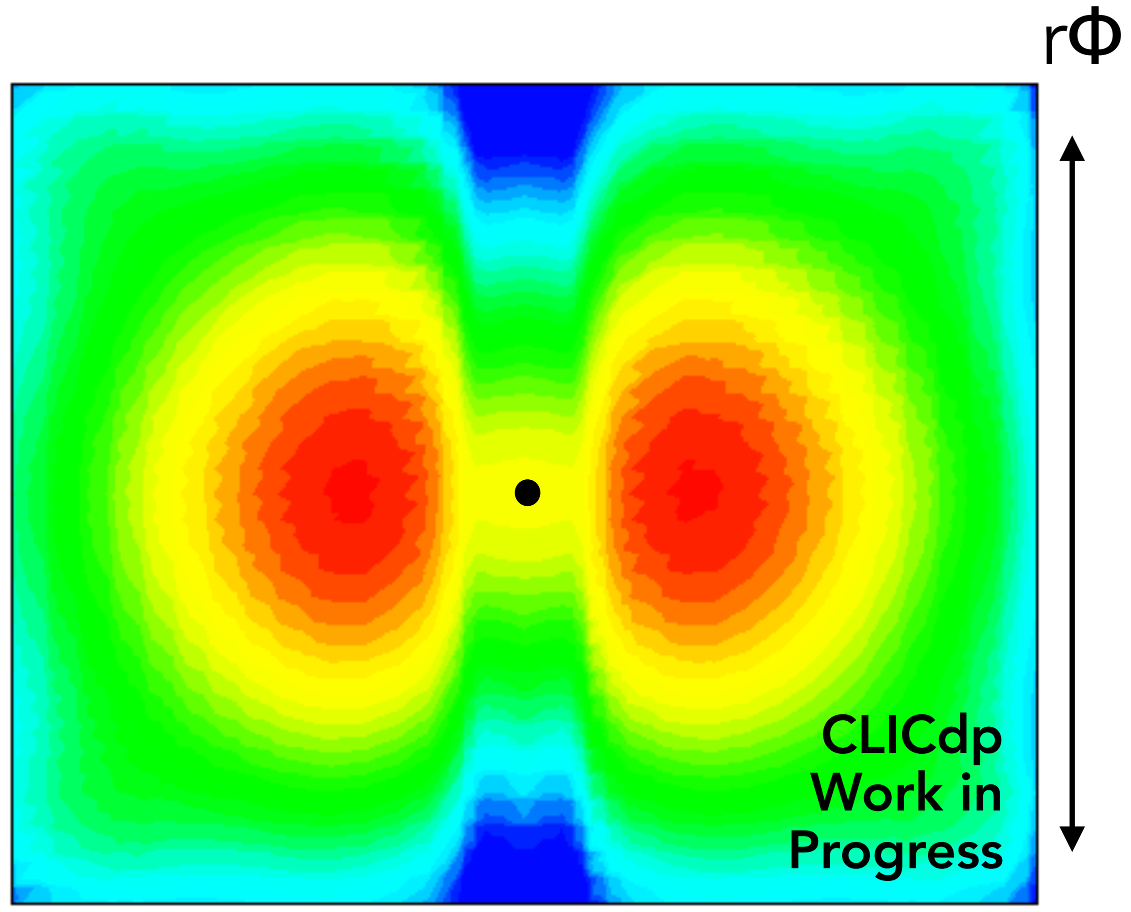
Gap in both dimension:





Gap only in z dimension:

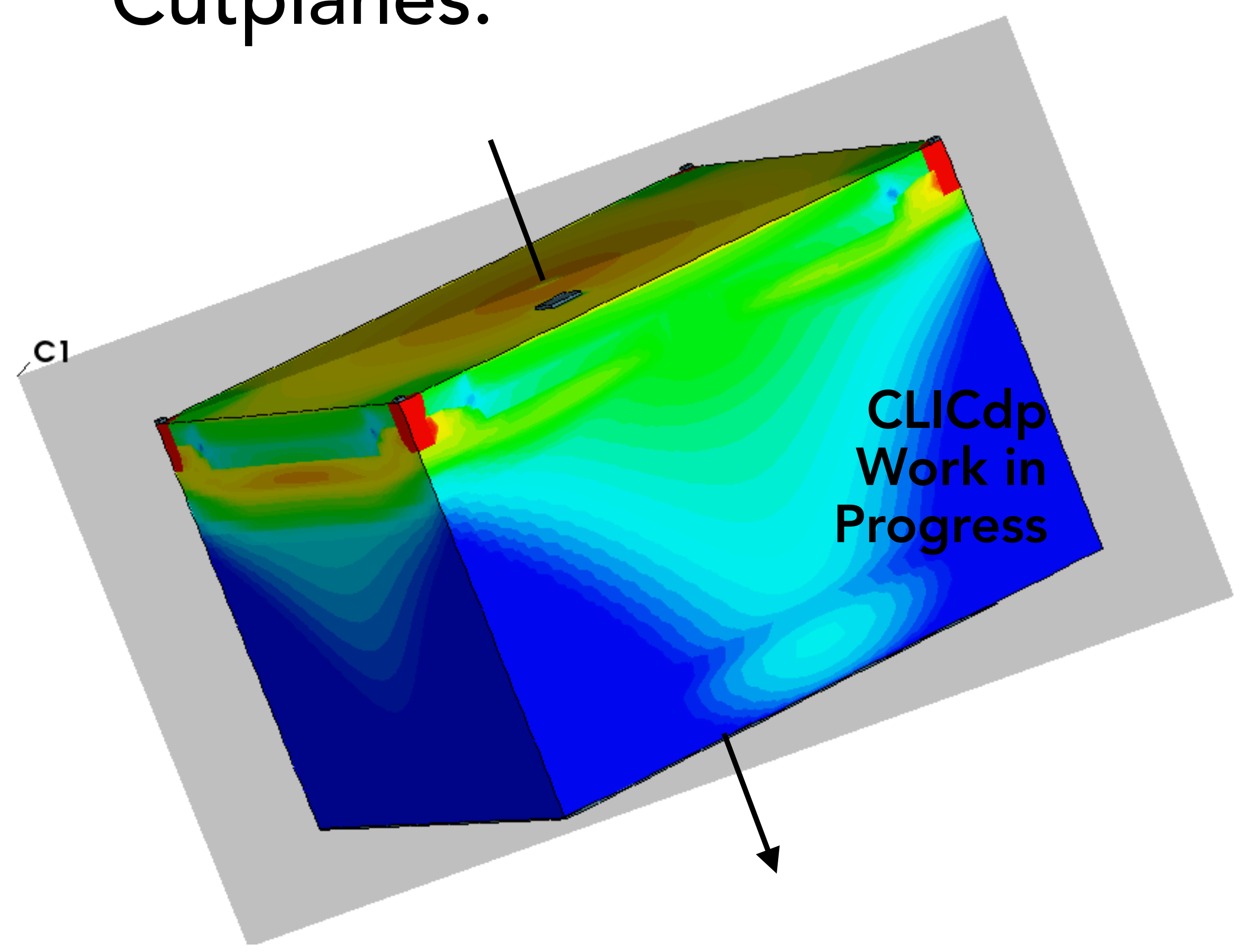


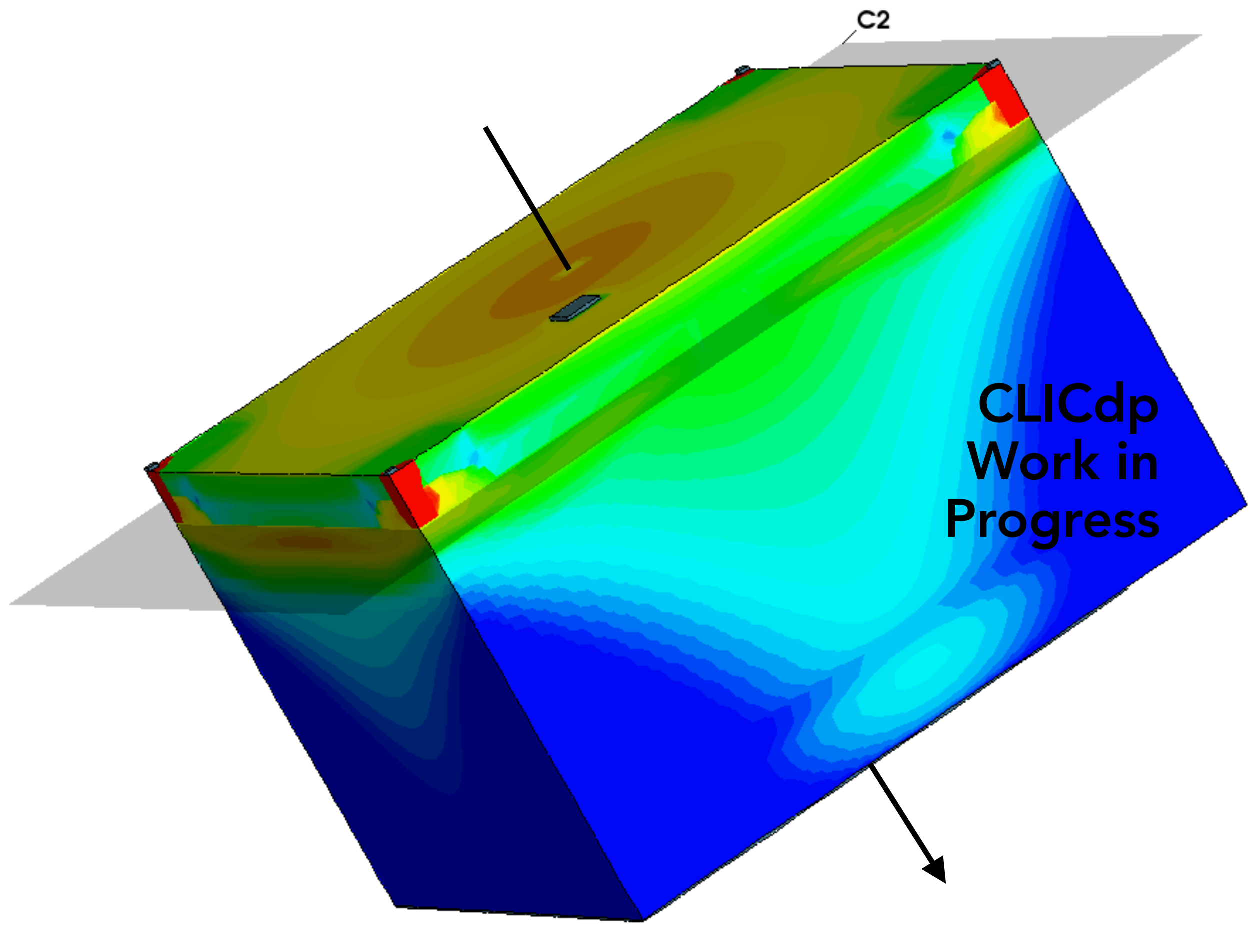


Charge sharing along rΦ is less effected compared to gap in both dimensions

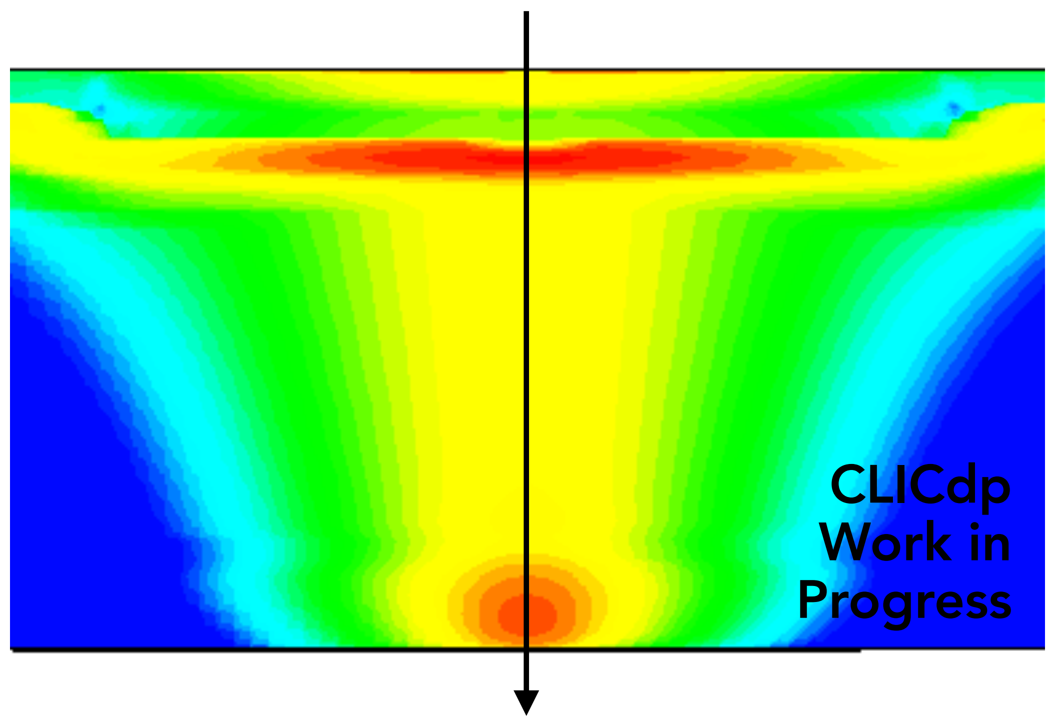
Transient / electron density 3 ns after particle incident

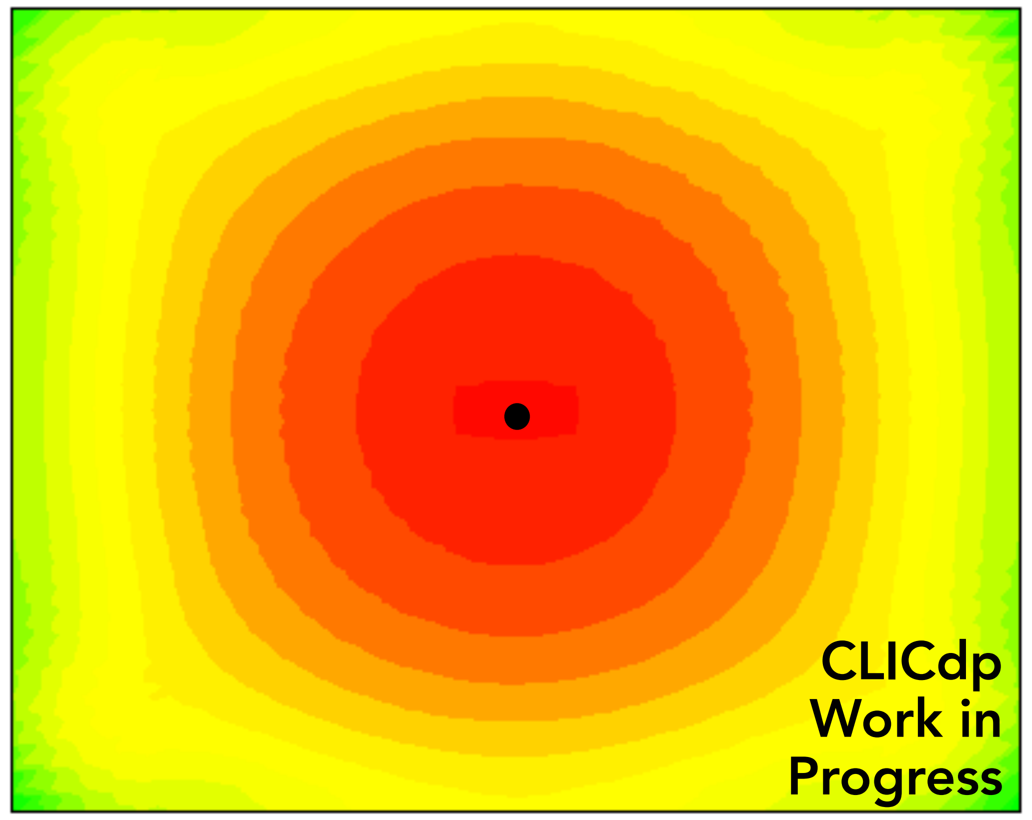
Cutplanes:



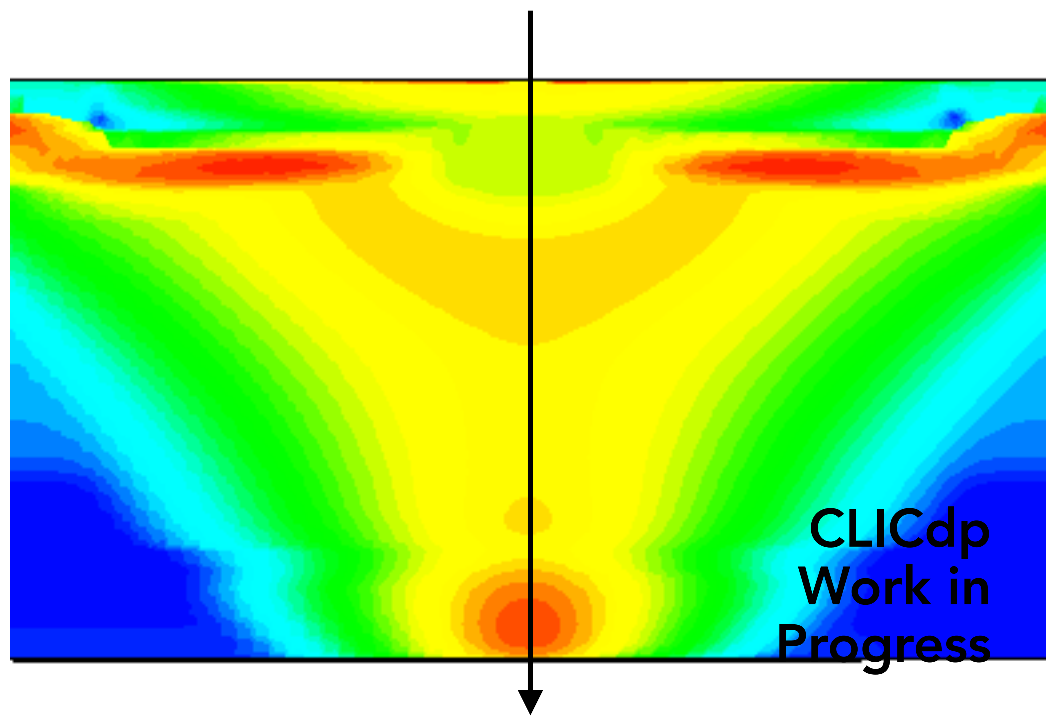


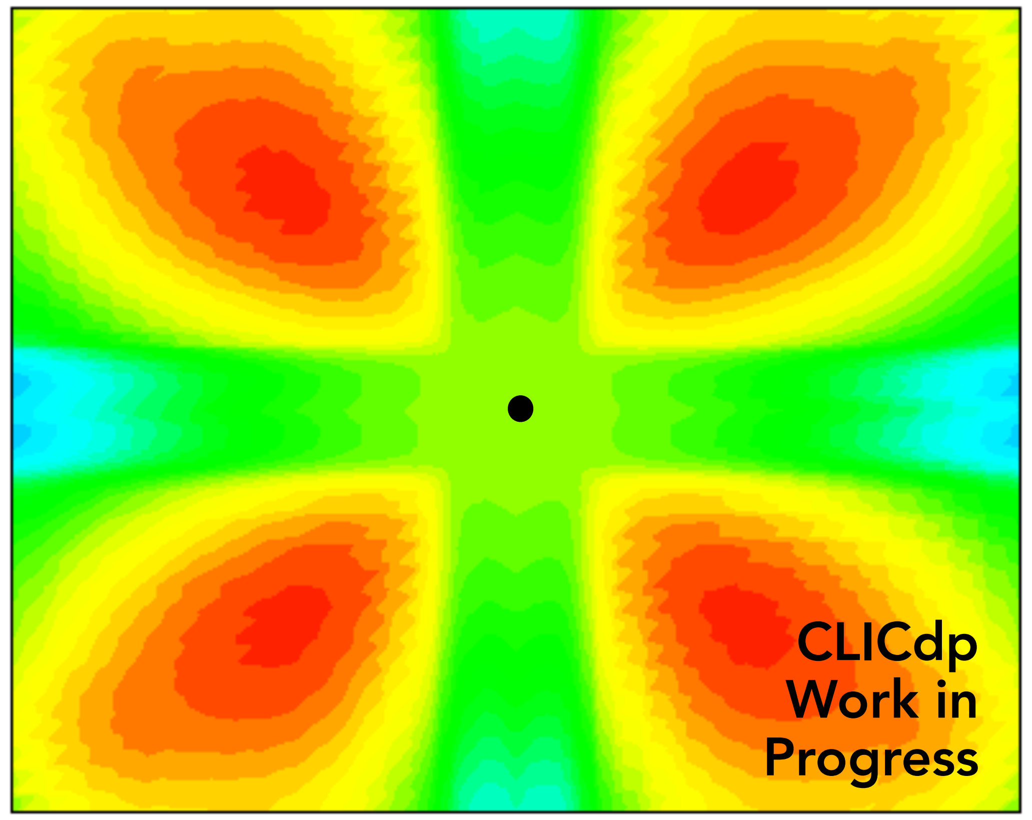
Modified process:



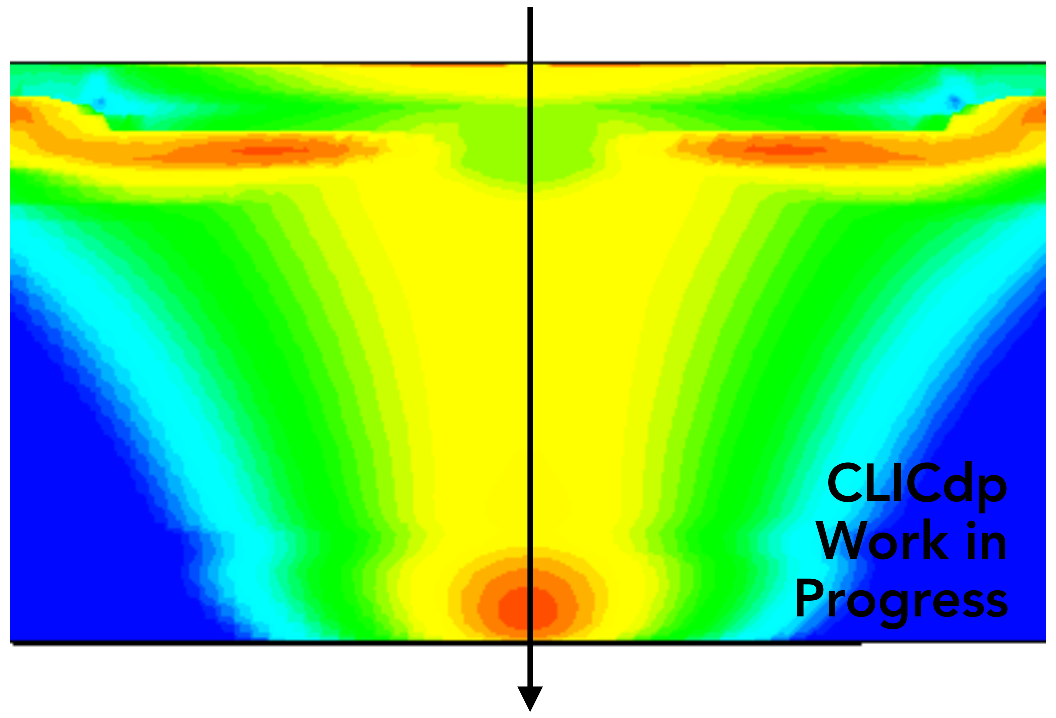


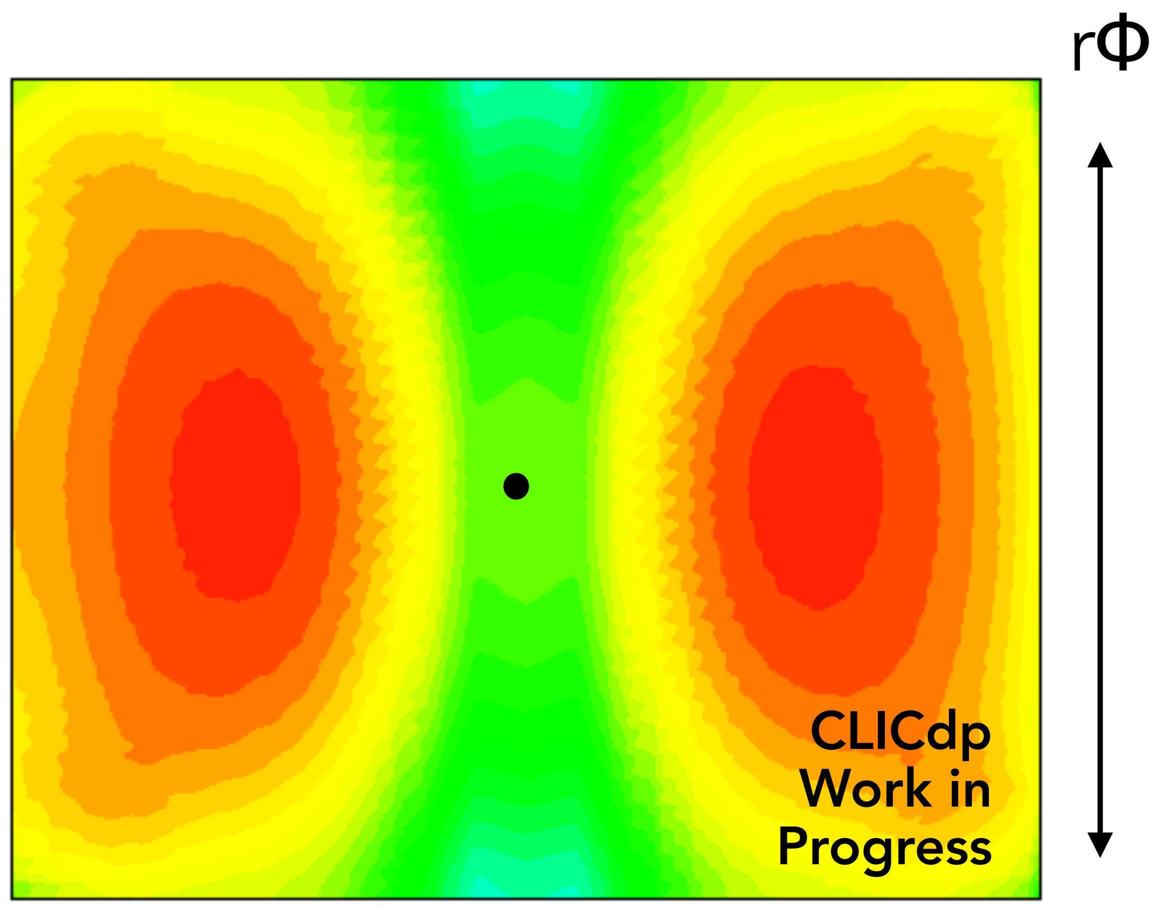
Gap in both dimension:





Gap only in z dimension:

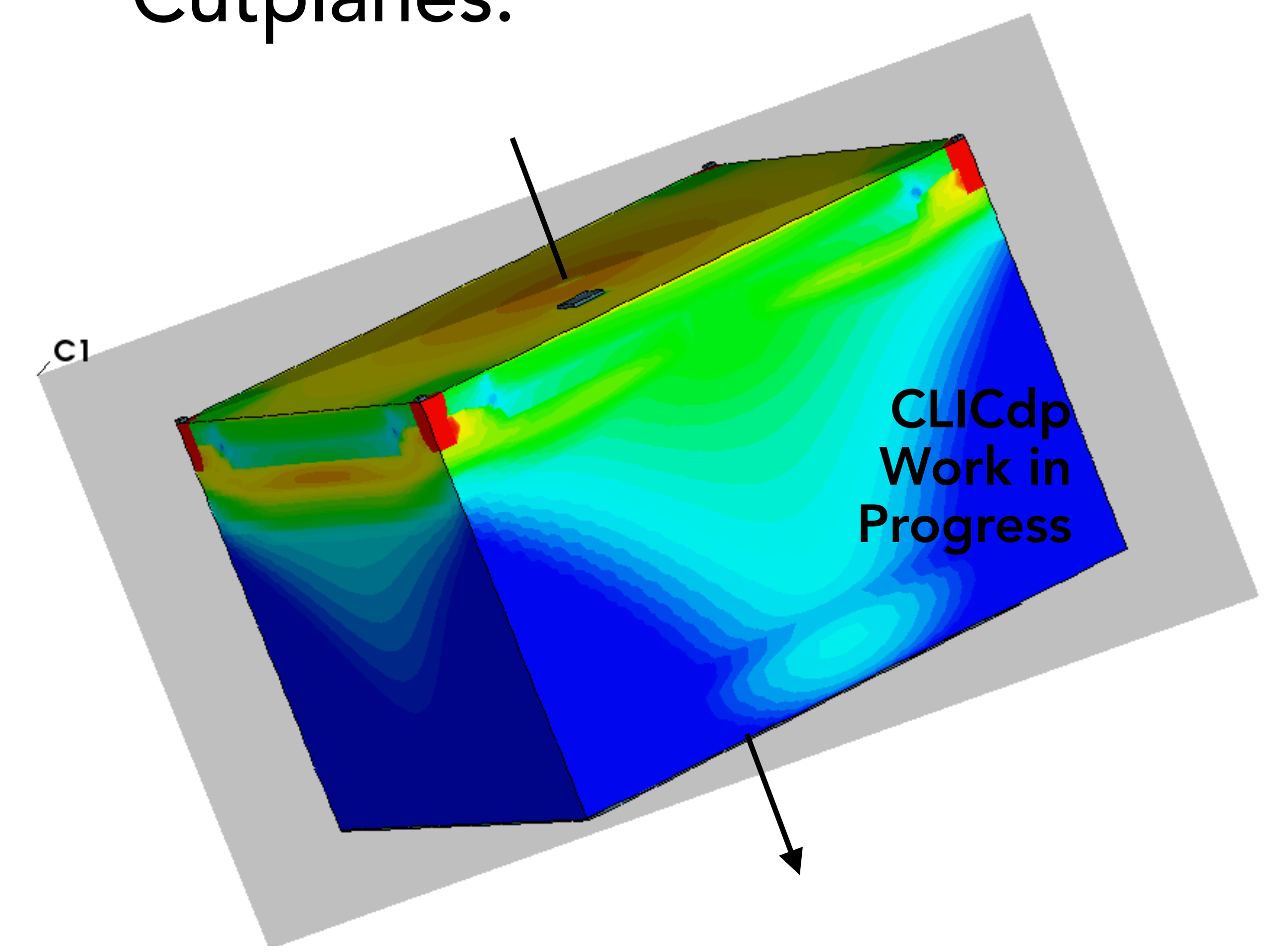


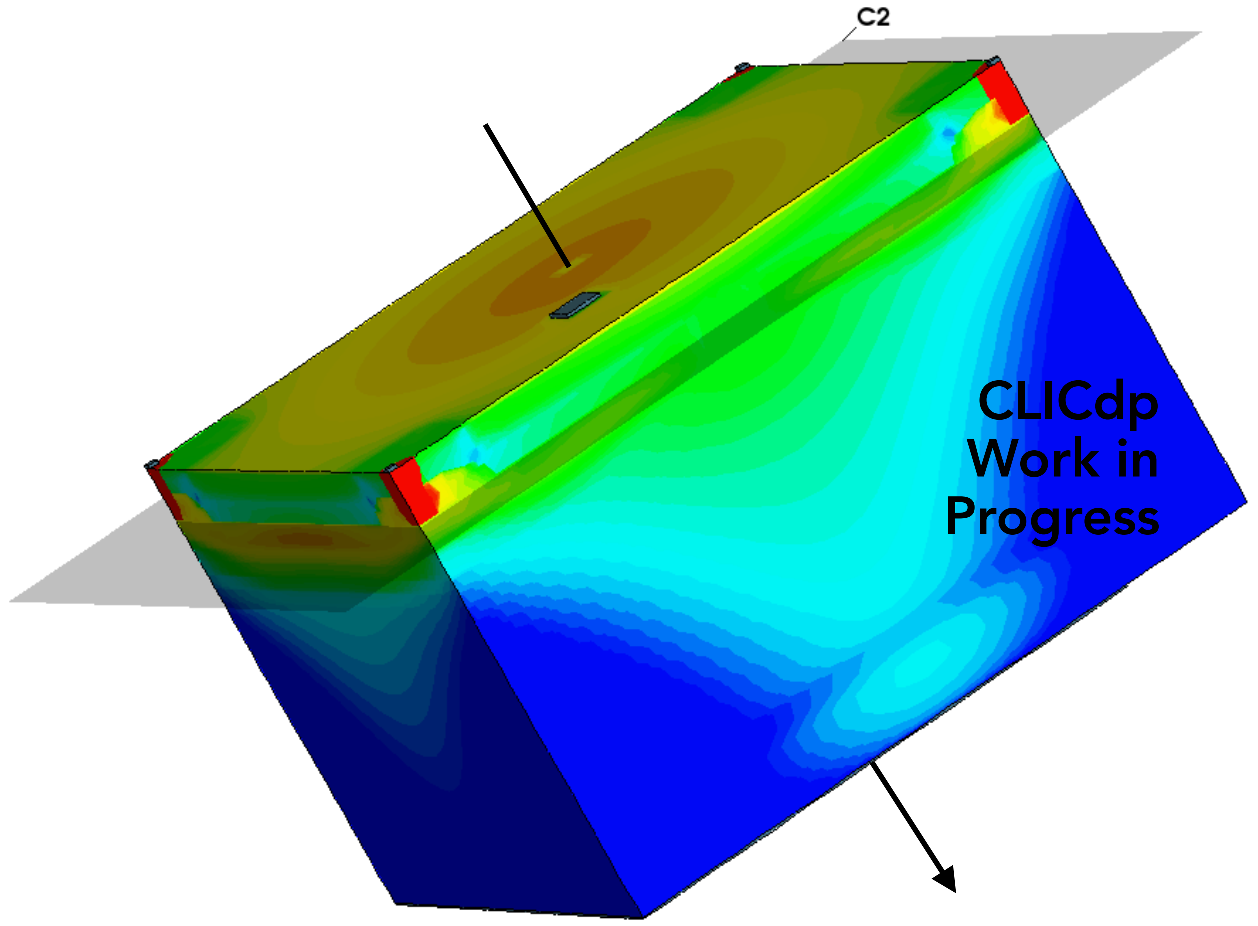


Charge sharing along rΦ is less effected compared to gap in both dimensions

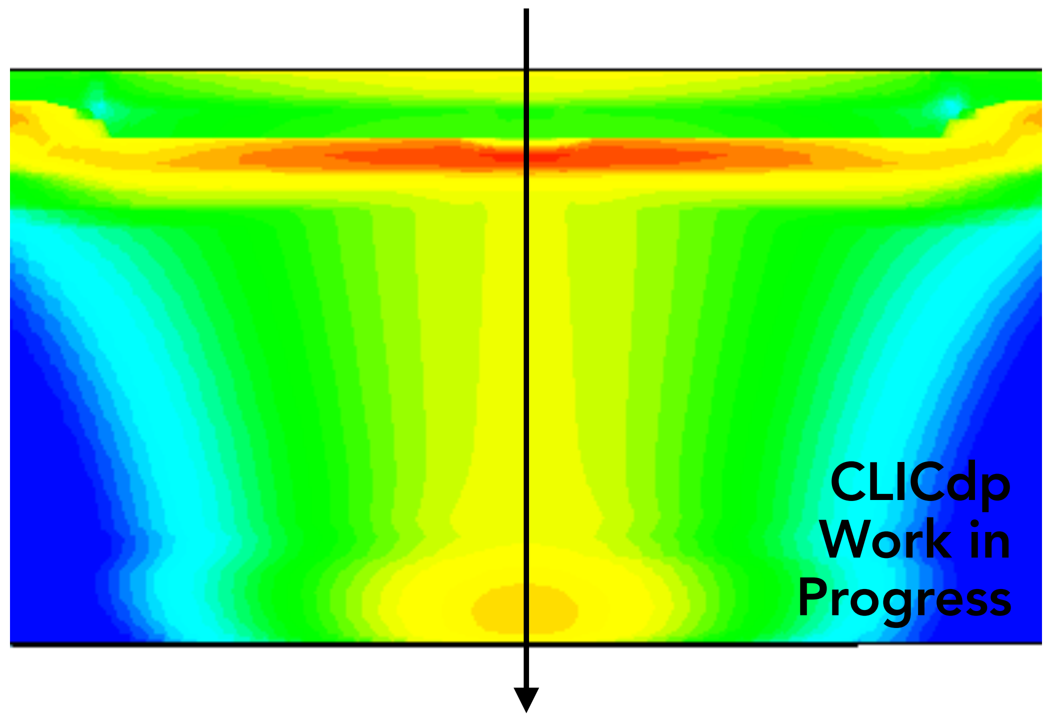
Transient / electron density 6 ns after particle incident

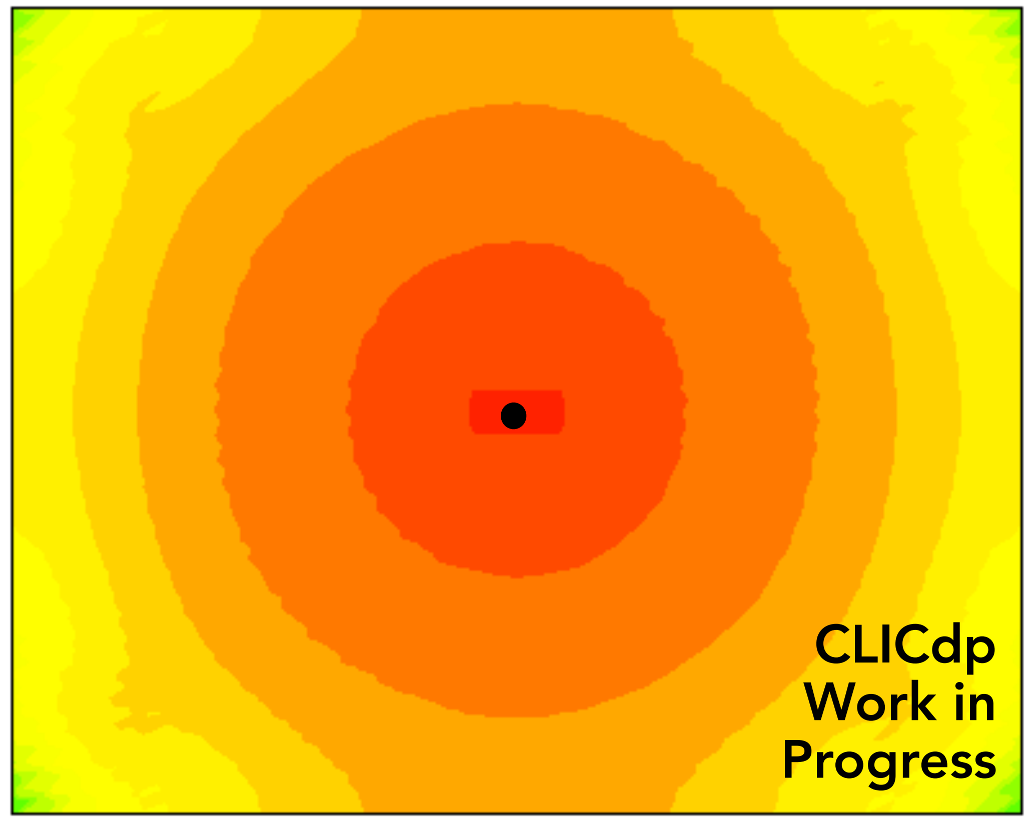
Cutplanes:



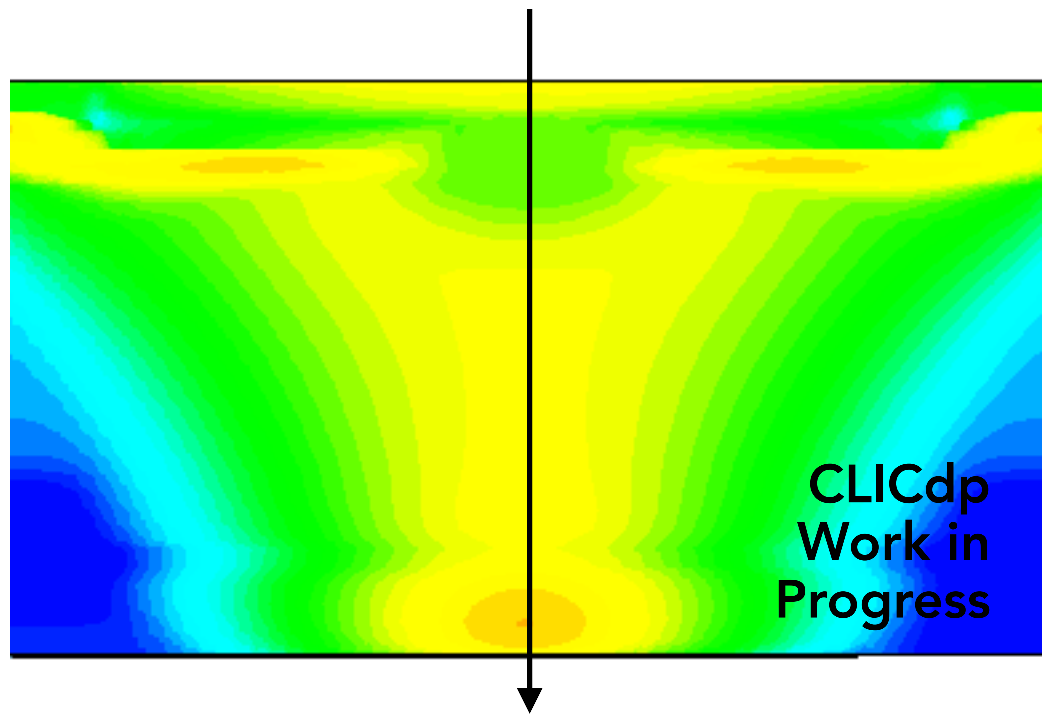


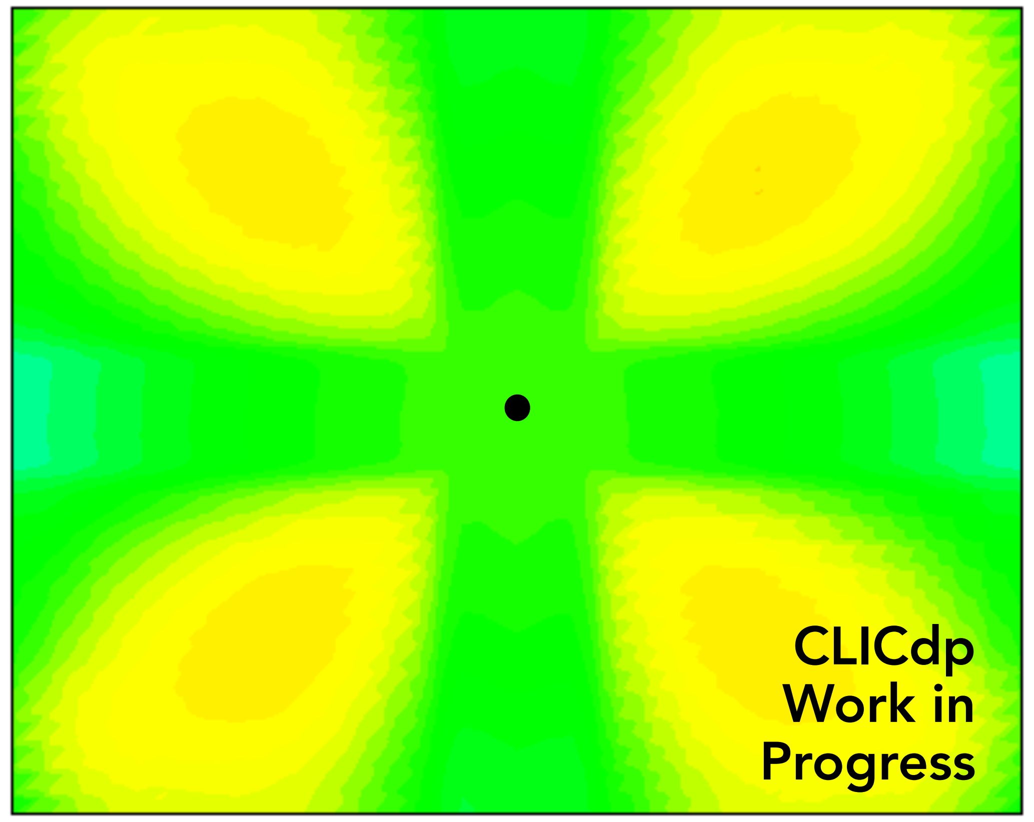
Modified process:



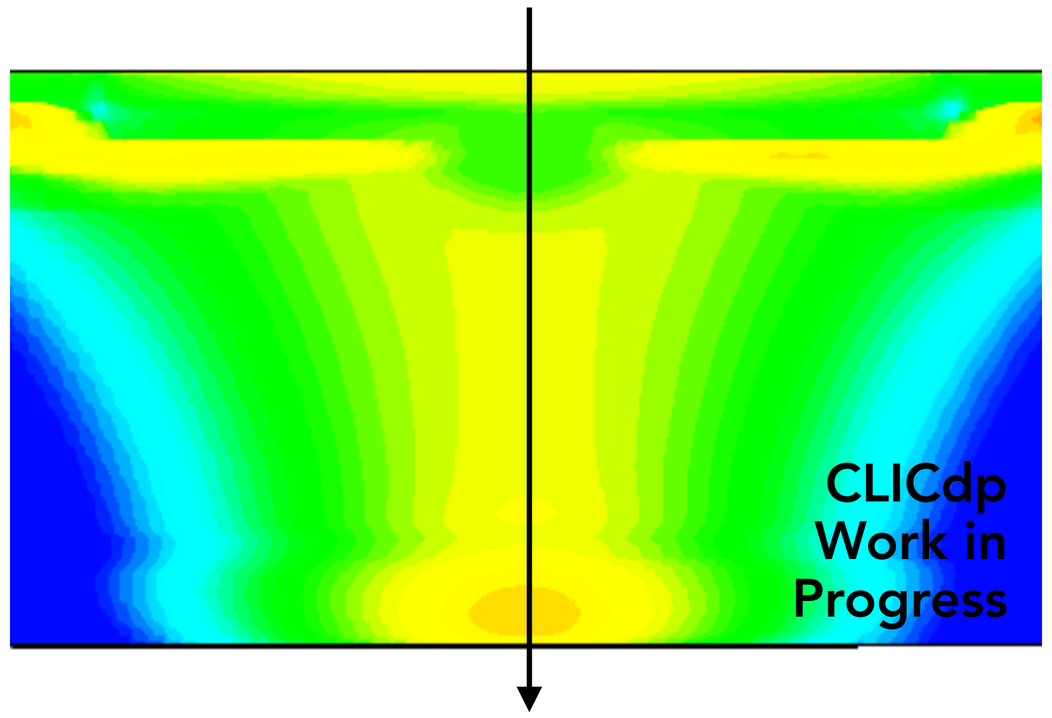


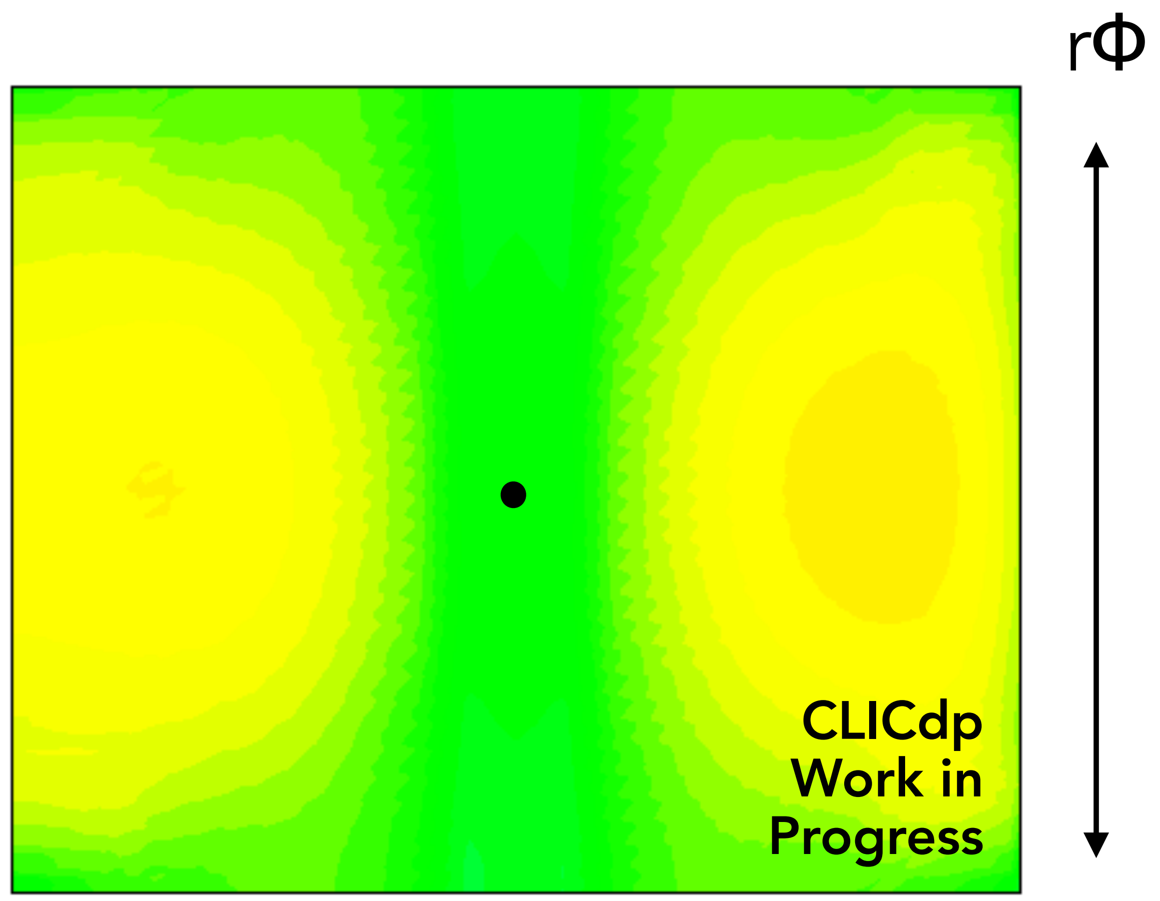
Gap in both dimension:





Gap only in z dimension:

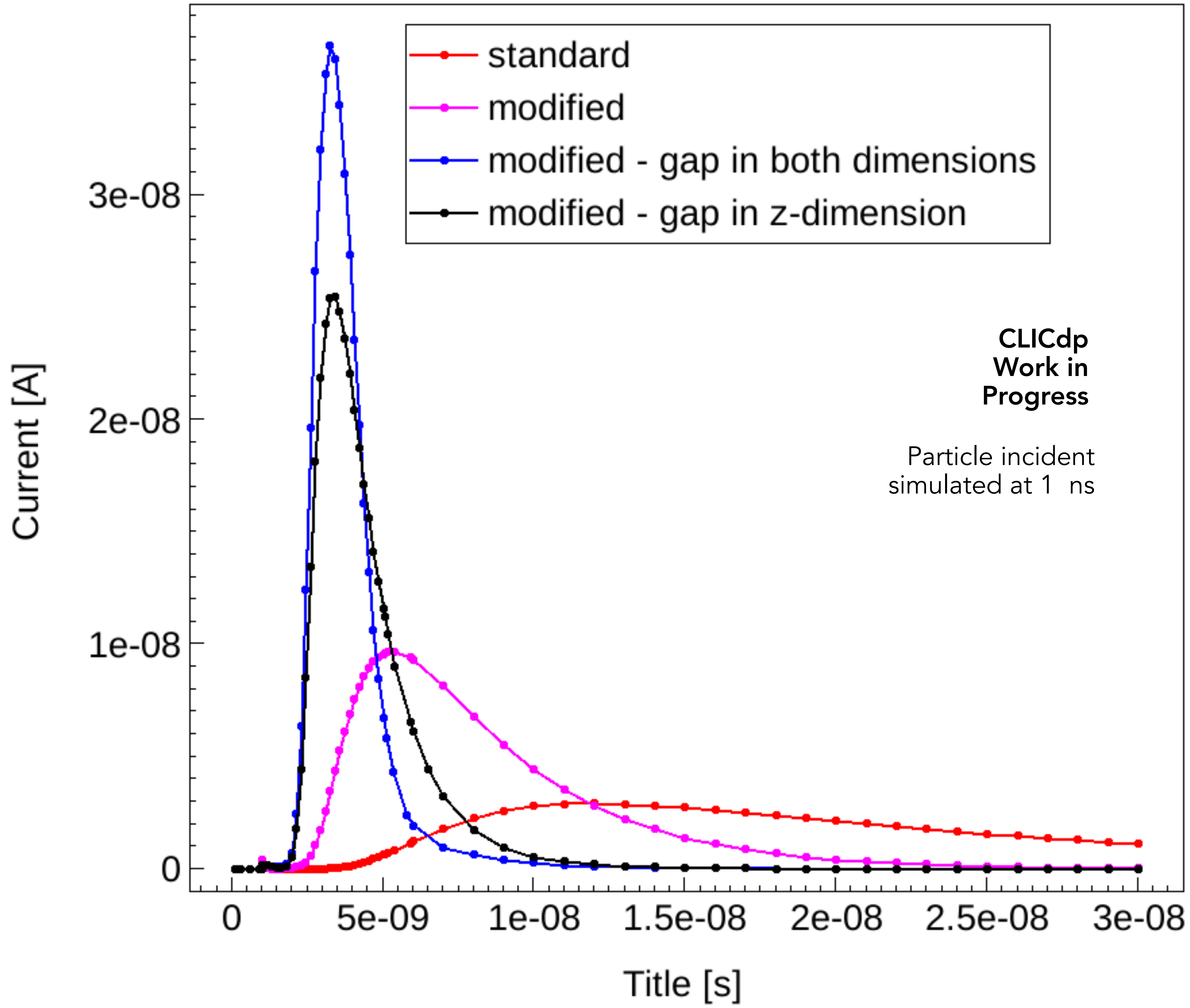




Charge sharing along rΦ is less effected compared to gap in both dimensions

Transient / current pulses for different sensor designs

Current induced on single pixel
(corner —> equal distance to incident particle):

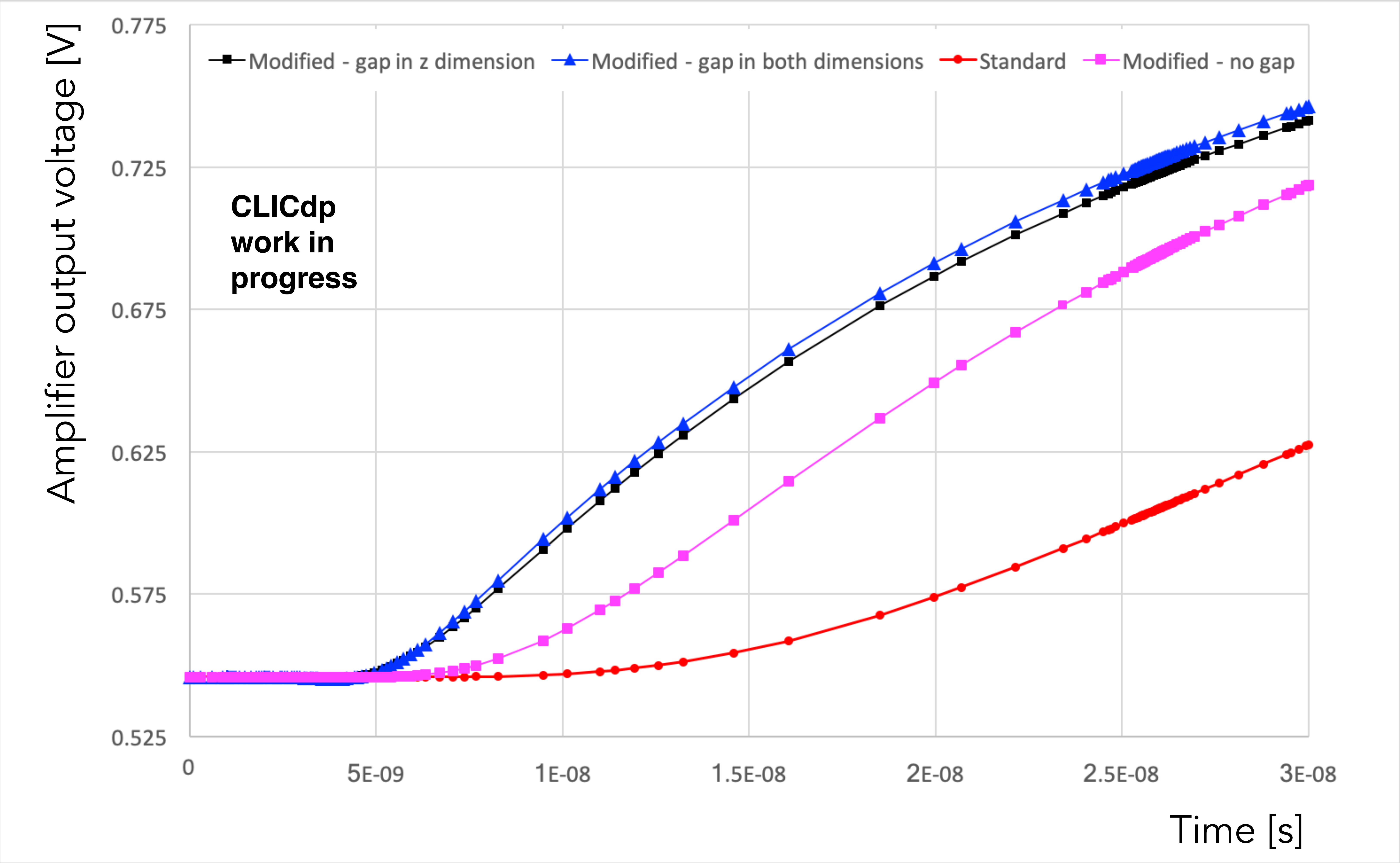


Faster charge collection ↓

- Standard process
- Modified process
- Modified process with gap only along z
- Modified process with gap along both dimensions

Transient / amplifier response for different sensor designs

Use current pulses from 3D transient TCAD as input for analogue front-end simulation (Rafael Ballabriga):



Bench mark of worst case:

- Incident at pixel corner with lowest field
- Input capacitance of 2.5 fF

Gap only in z-dimension:

Timing very similar to gap in both dimensions

Best timing for modified process with gap in n-layer

Allpix Squared simulation setup

Motivation:

- Determine impact of different sensor layout on spatial resolution

Simulation concept:

- MonteCarlo simulation using static electric field from TCAD to calculate charge propagation path
- Charge calculated as number of charge carriers that arrive at the collection electrode (induced current not taken into account)

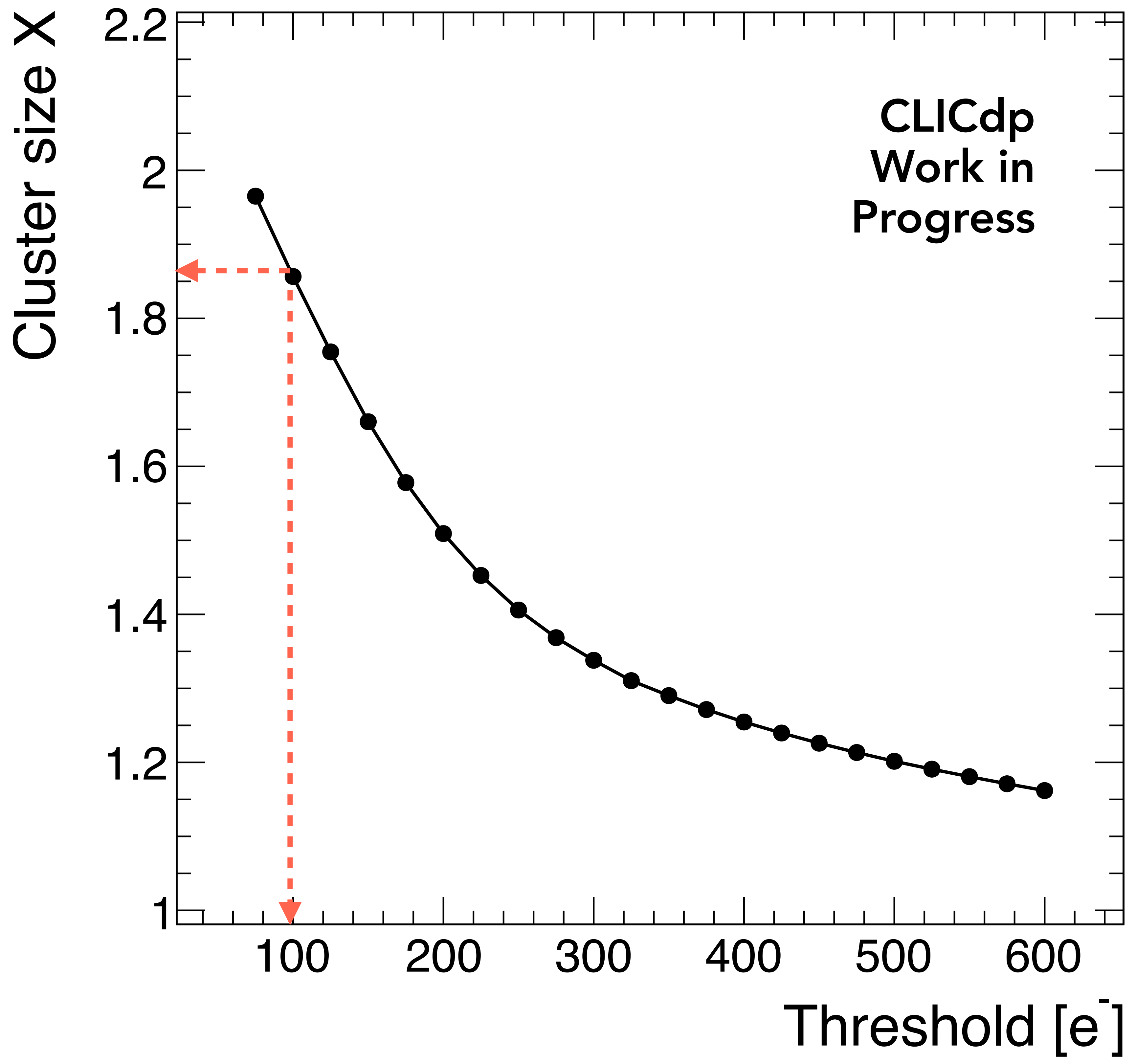
Parameters:

- Noise of 10 e^-
- Total thickness of 100 µm
- Thickness of epitaxial layer of 25 µm

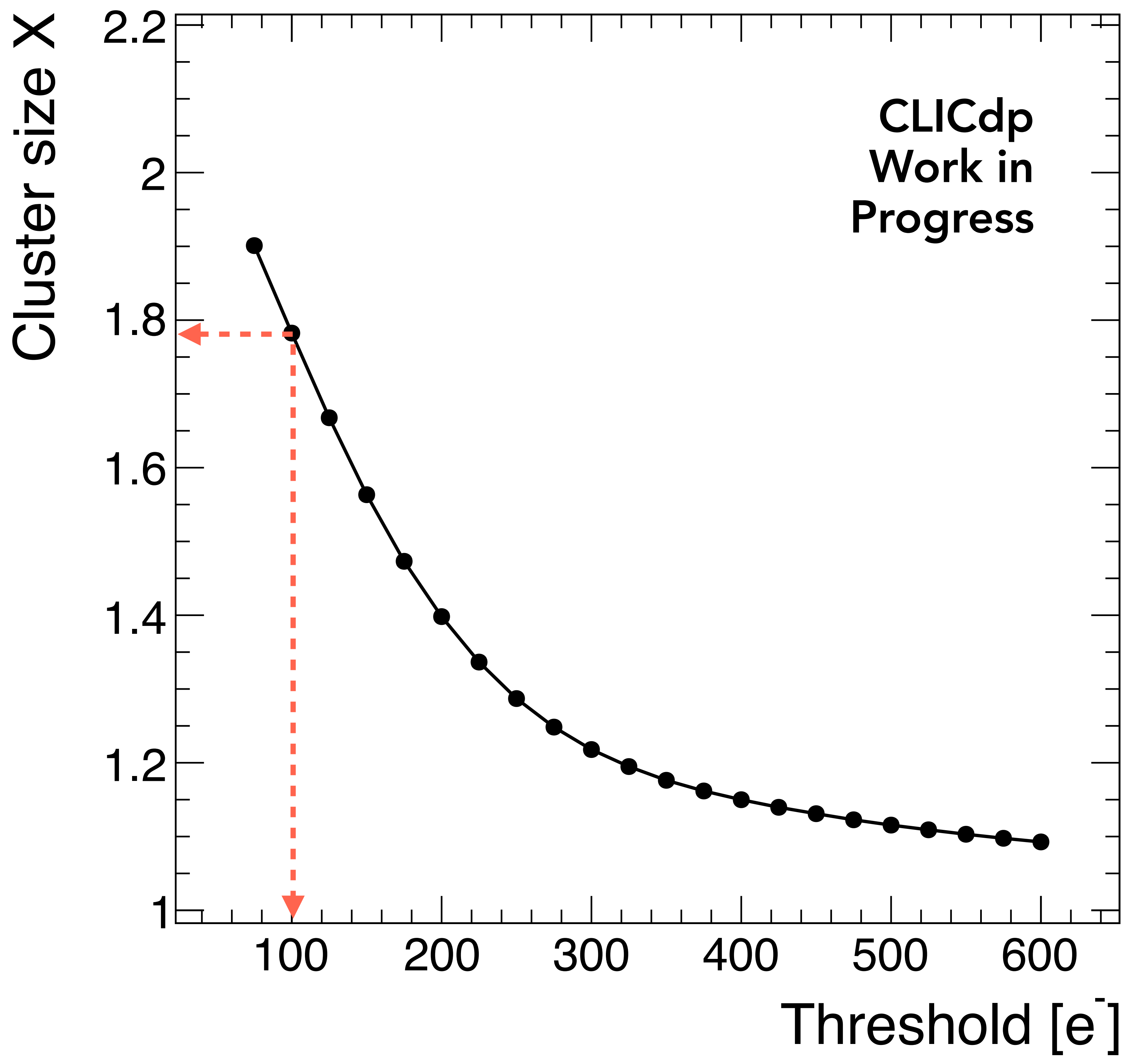
→ ***Homogenous illumination of large pixel matrix (high statistics) and modelling of Landau fluctuations***

Allpix Squared simulation results - charge sharing in rΦ

Modified process:



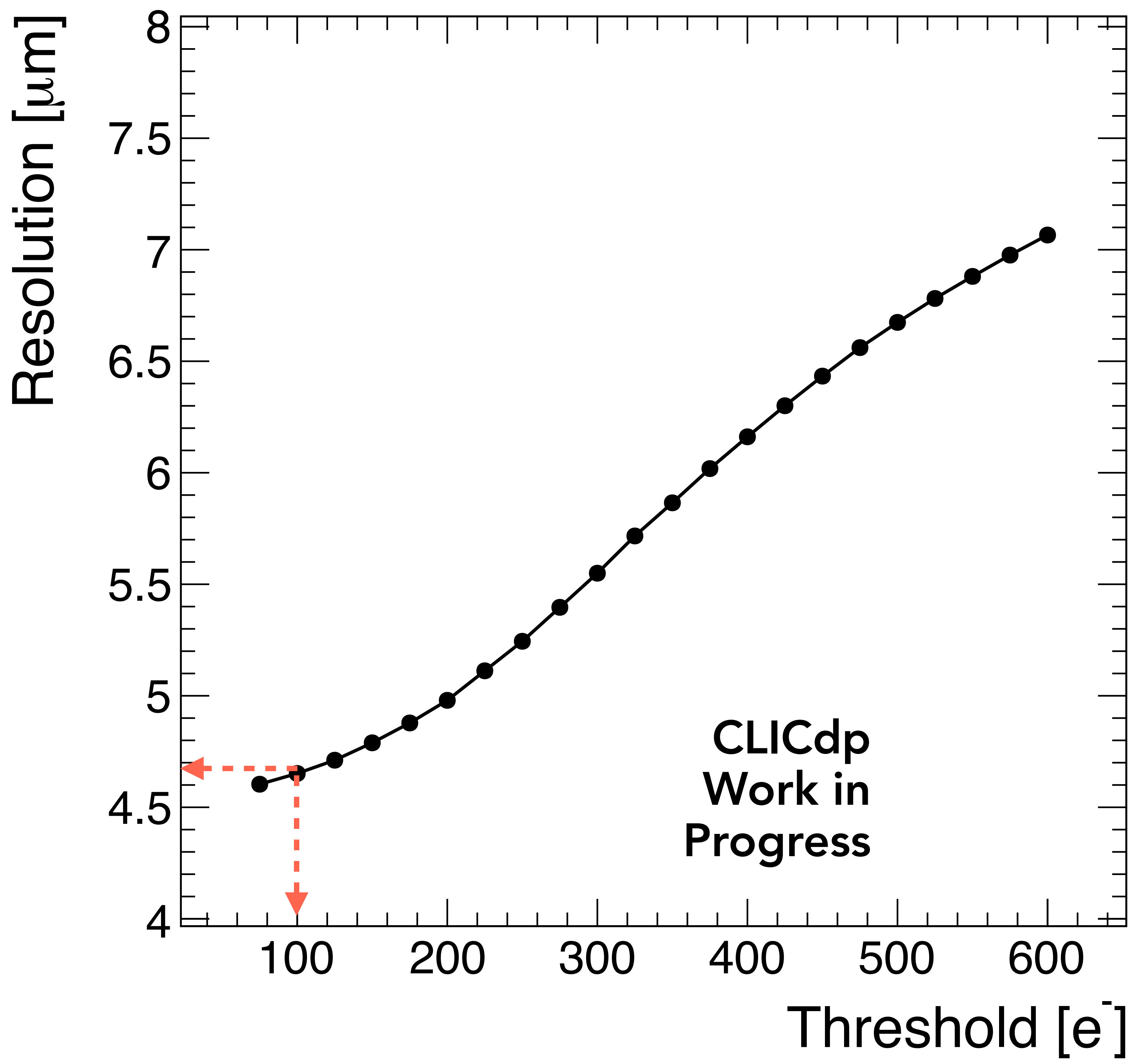
Modified process with gap in n-layer:



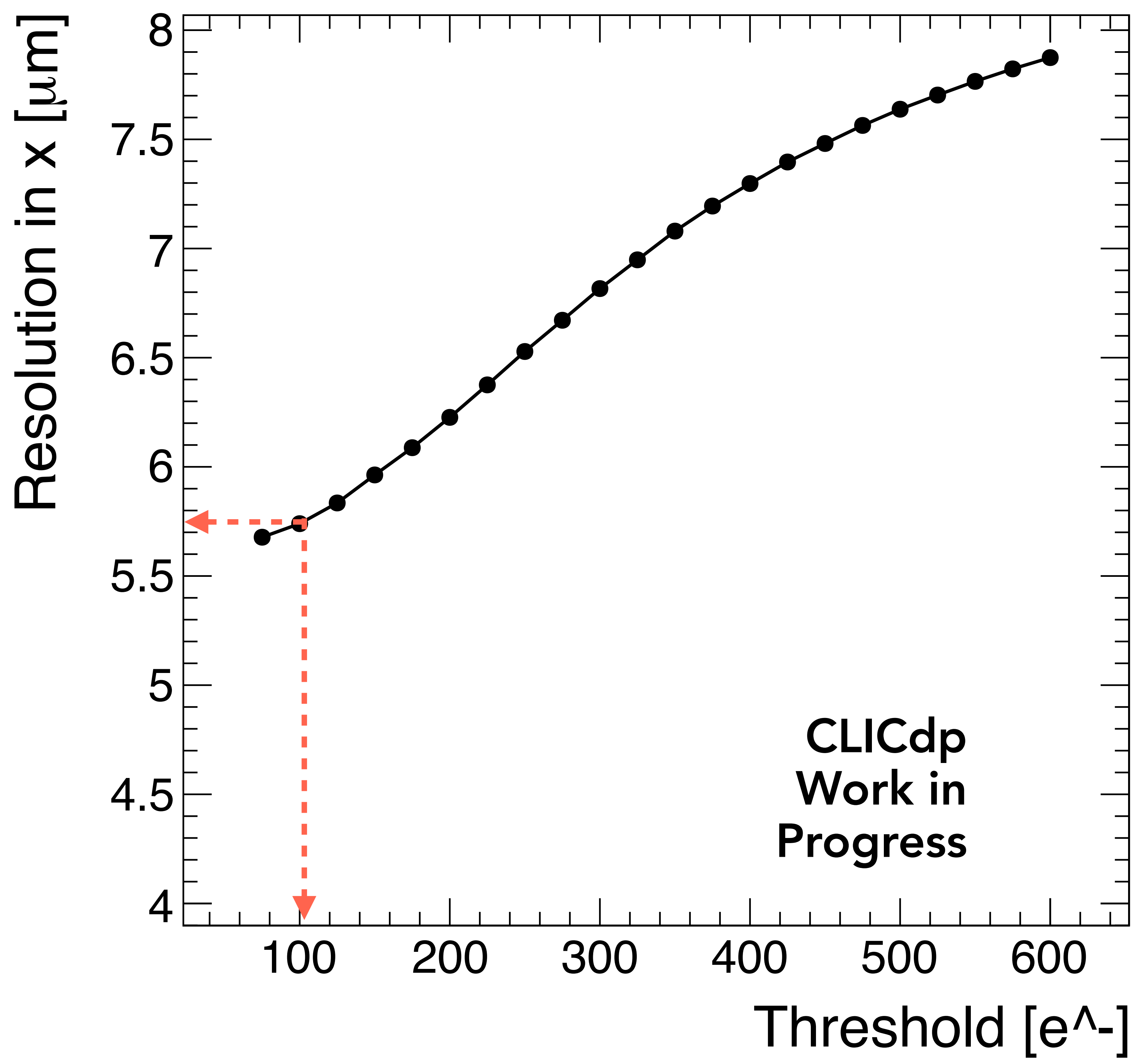
→ **Reduced charge sharing with gap in N-layer**

Allpix Squared simulation results - resolution in rΦ

Modified process:



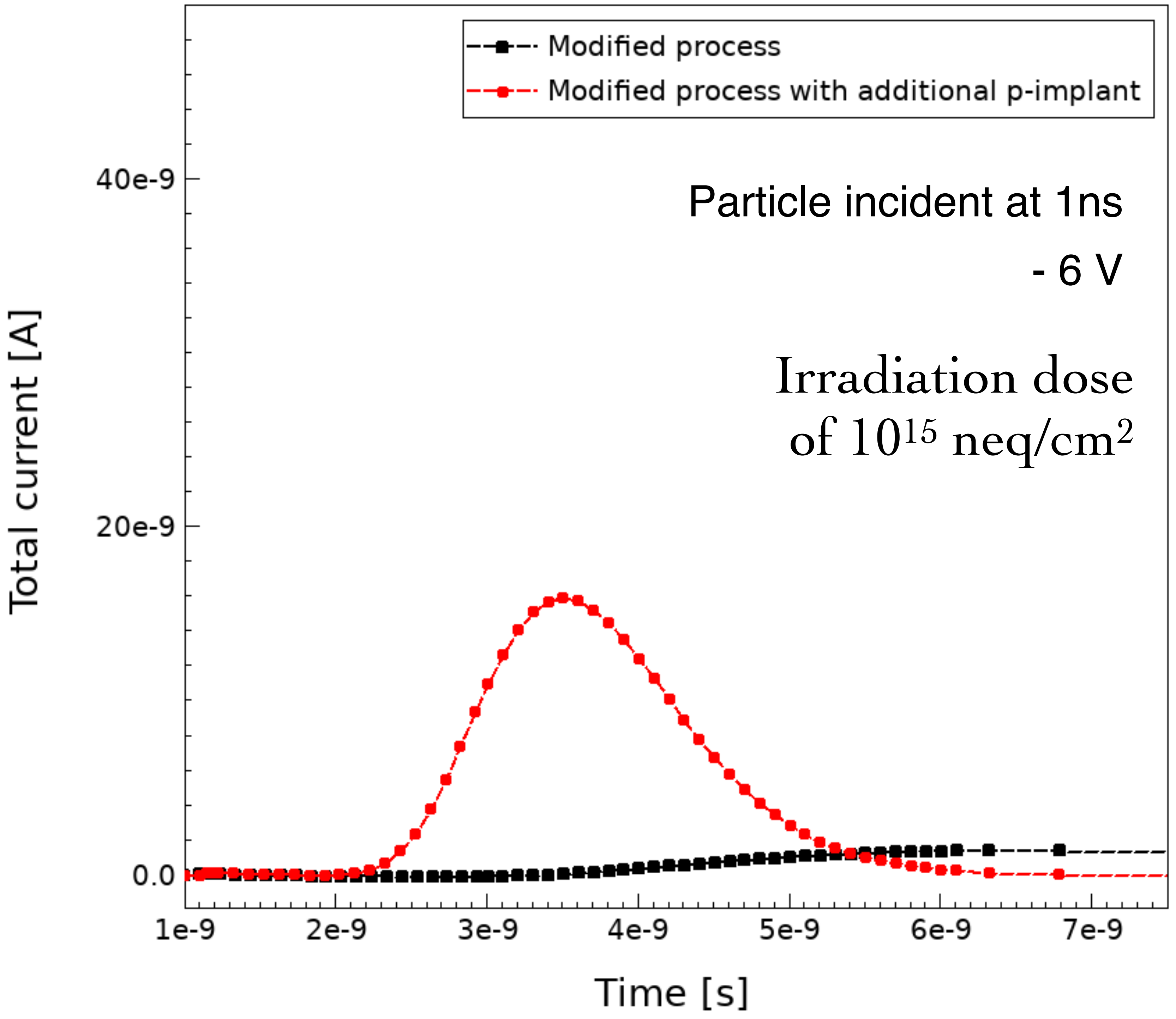
Modified process with gap in n-layer:



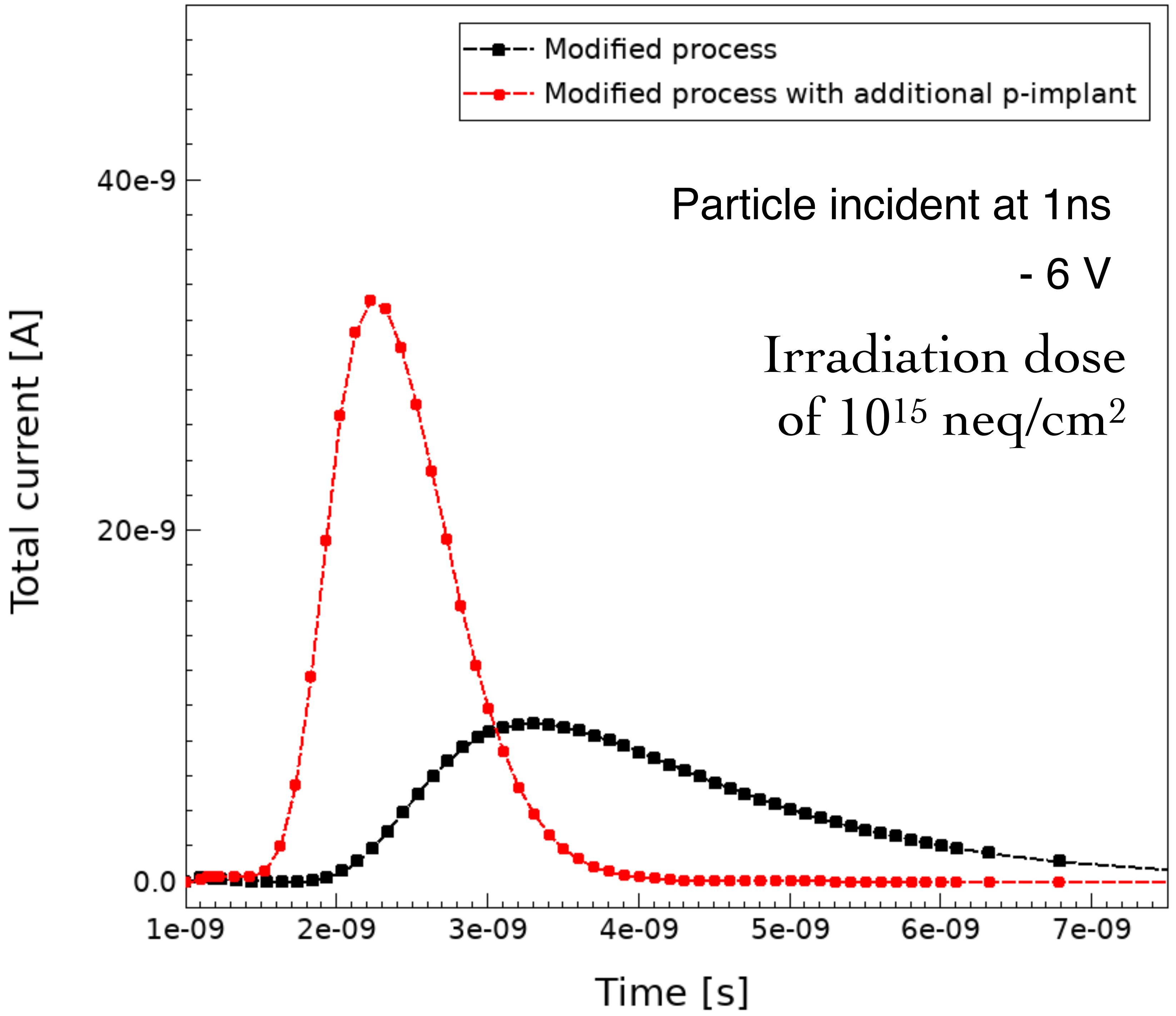
→ **Reduced spatial resolution with gap in N-layer**

A word on future perspectives of the new sensor concepts

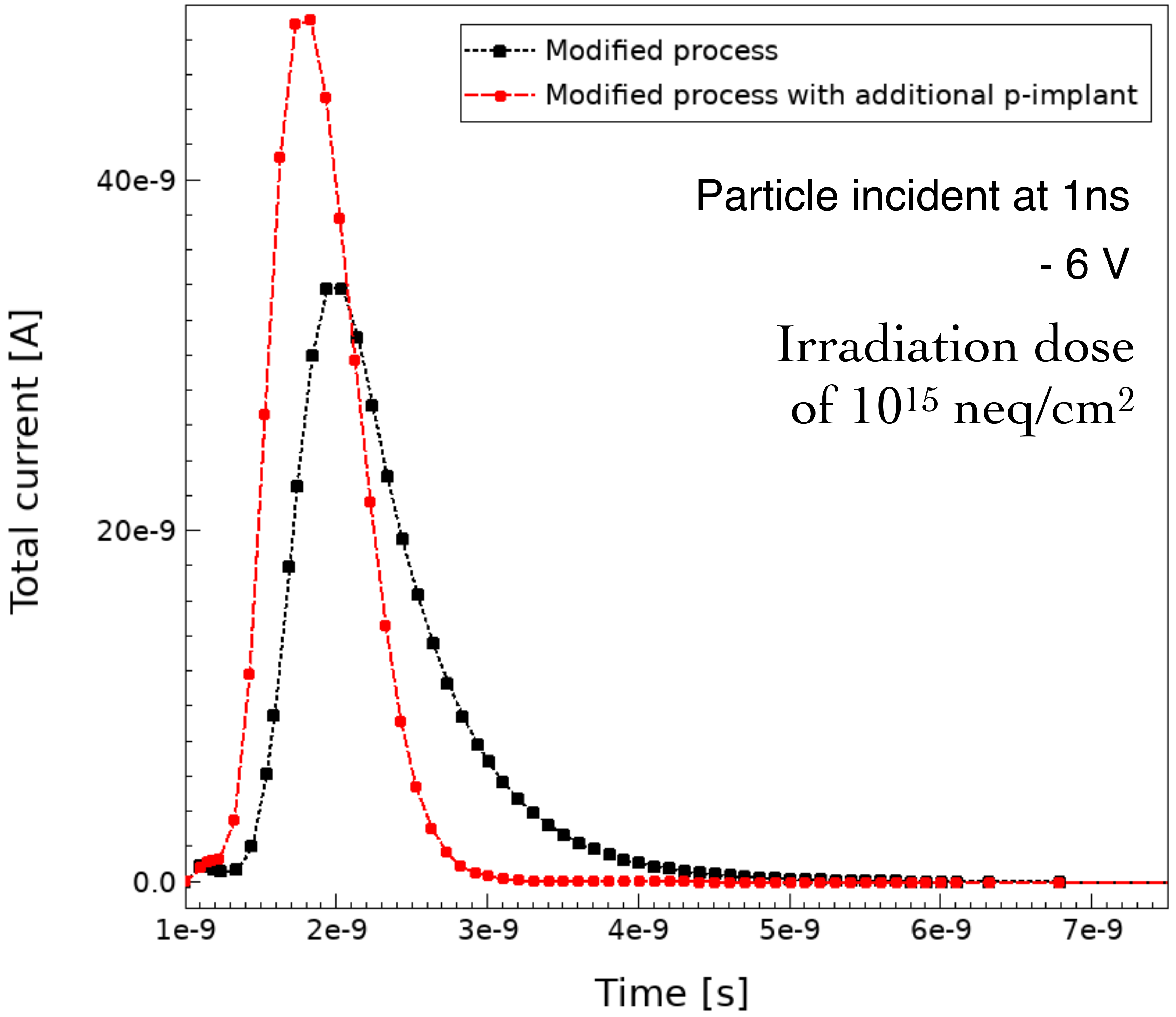
Pixel size 36.4 x 36.4 μm²:



Pixel size 28 x 28 μm²:

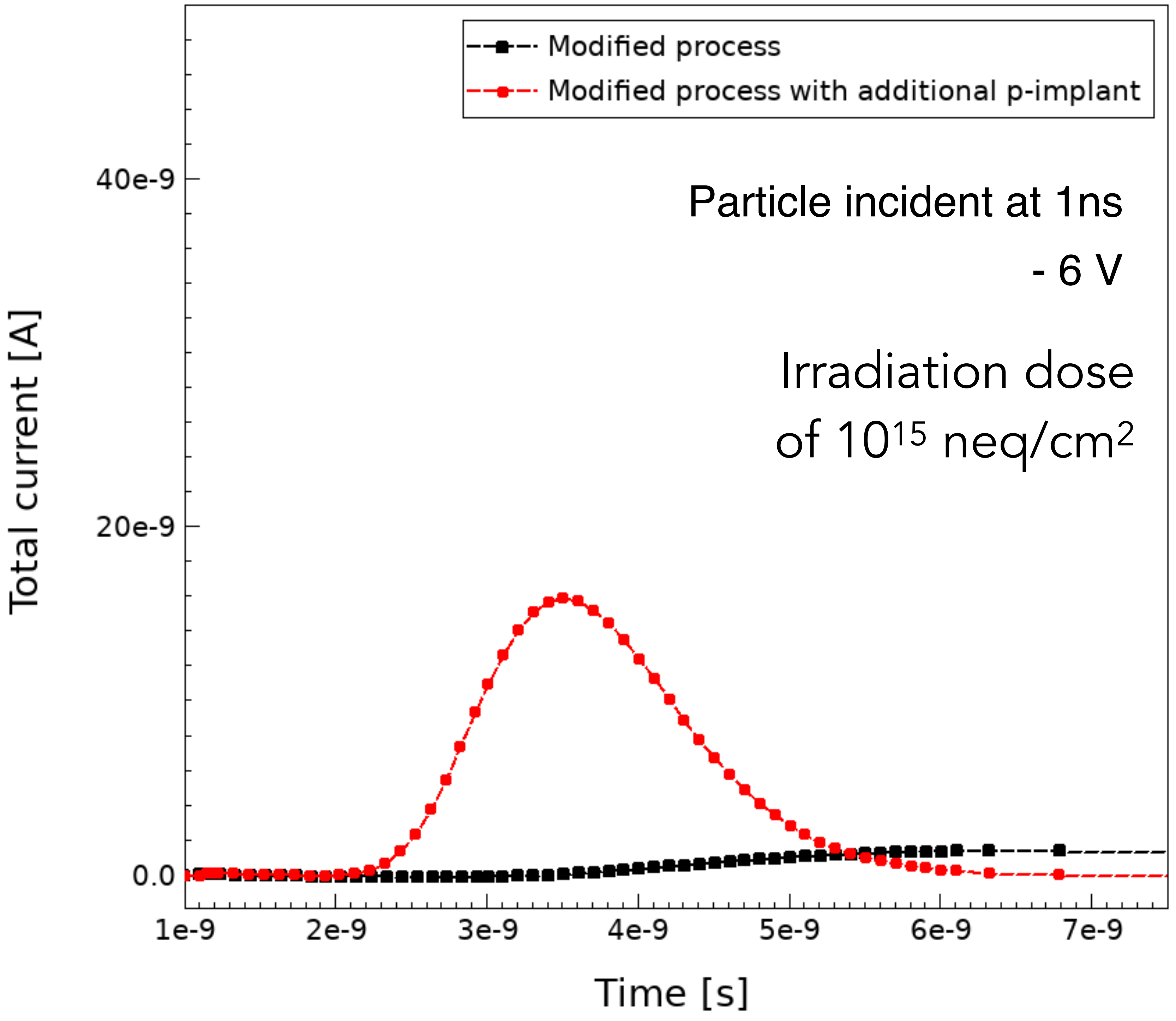


Pixel size 20 x 20 μm²:

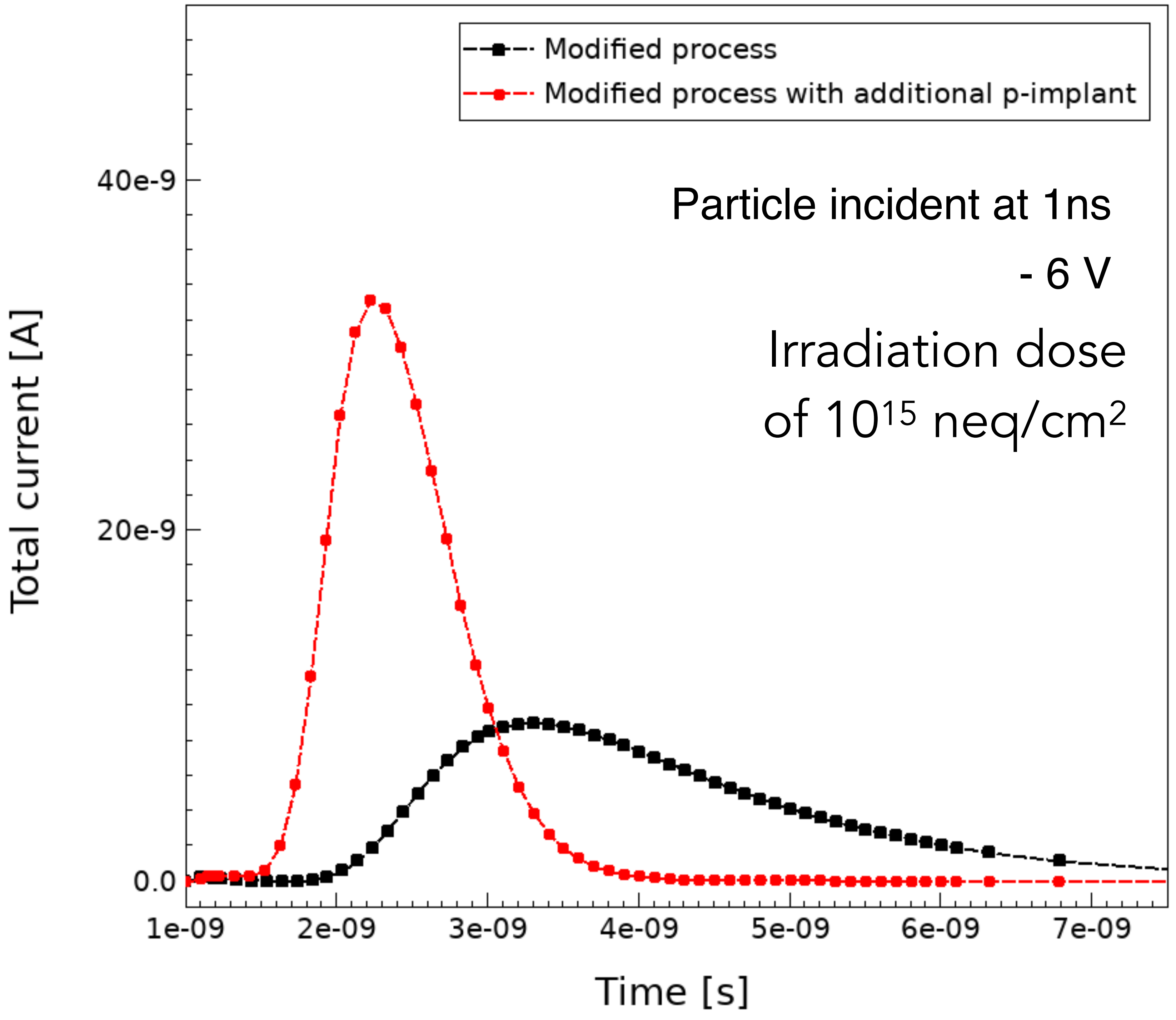


A word on future perspectives of the new sensor concepts

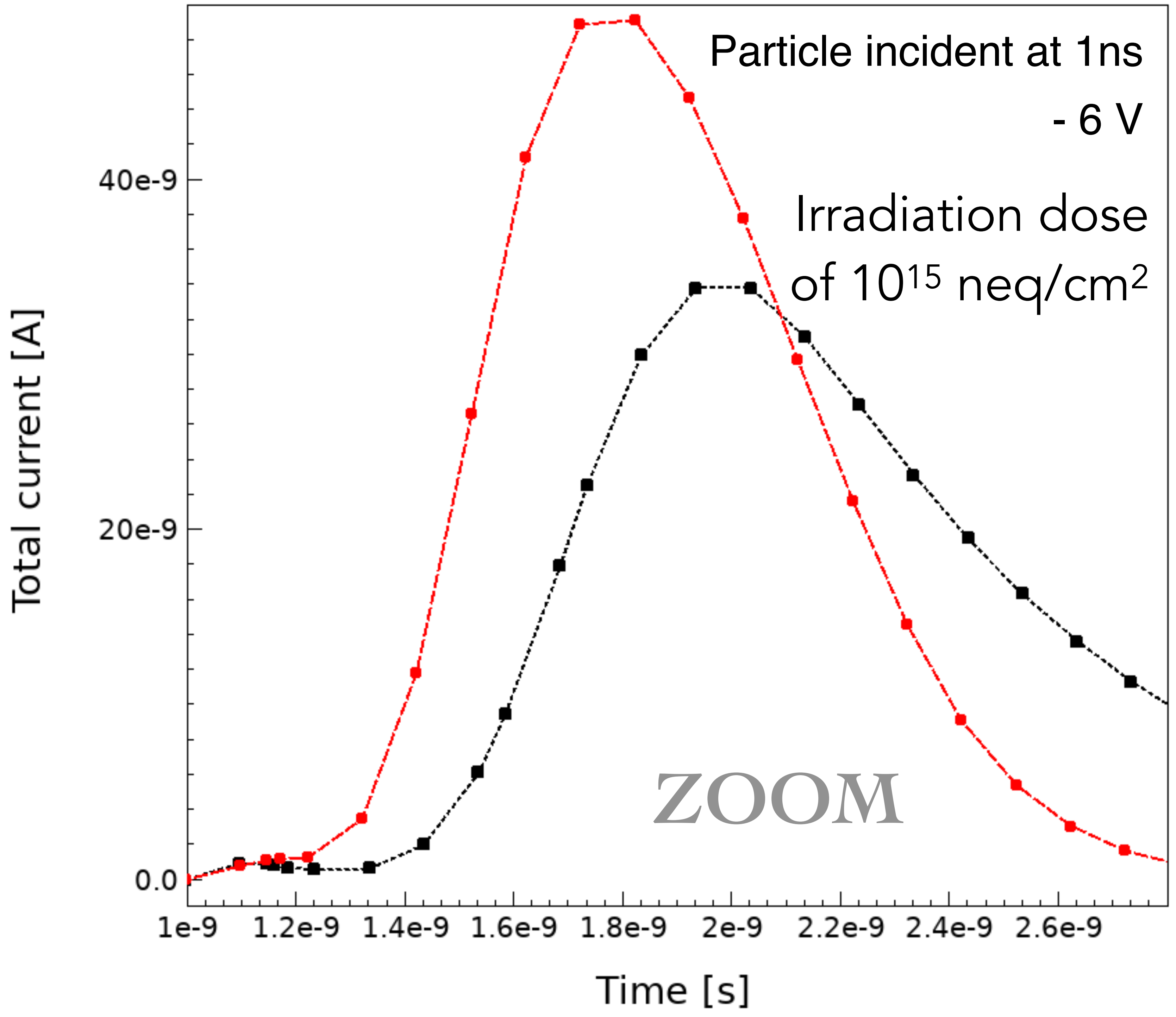
Pixel size 36.4 x 36.4 μm²:



Pixel size 28 x 28 μm²:



Pixel size 20 x 20 μm²:



—> Even for very small pixel size of 20 μm the additional modifications improve significantly the rise and fall time of the current pulses

—> Potential for future technologies —> sub-nanosecond timing (room for further improvement)

Conclusion and outlook

Different sensor layouts have been simulated and studied for a CLICTD tracker chip implemented in a HR CMOS process with a small collection electrode:

↳ The **modified process with a gap in the N-layer only along the z-dimension** has been found to be the best design to reach a fast charge collection while less impacting the charge sharing in r**Φ**

↳ Next step: Implement design with gap only in z-dimension in Allpix Squared

Conclusion for CLICTD submission:

↳ Process split with two different n-layer masks, resulting in two separate sets of wafers:
1.) Modified process
2.) Modified process with a gap in the N-layer only along the z-dimension

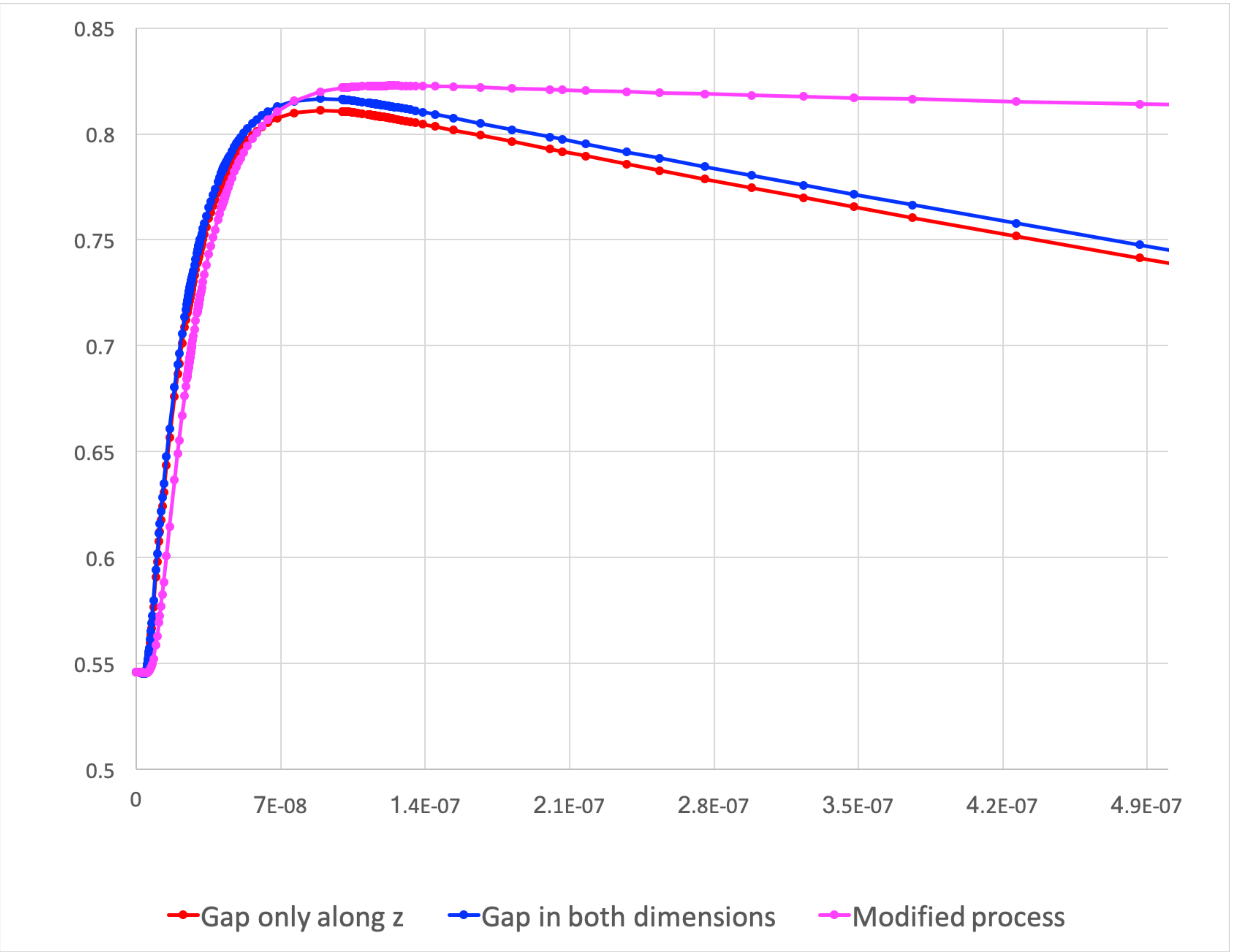
Conclusion for new sensor designs:

↳ Promising in view of improving charge collection time —> potential for future developments

Looking forward to exciting next year 2019:

- First prototypes of new sensor designs, currently being tested
- First fully fully monolithic chip for CLIC tracker with new features (elongated pixels), submission 11.02.2019

Backup


0.85
0.8
0.75
0.7
0.65
0.6
0.55
0.5
0
7E-08
1.4E-07
2.1E-07
2.8E-07
3.5E-07
4.2E-07
4.9E-07
Gap only along z
Gap in both dimensions
Modified process