CLICTD status and plans

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I. Kremastiotis, R. Ballabriga, N. Egidos

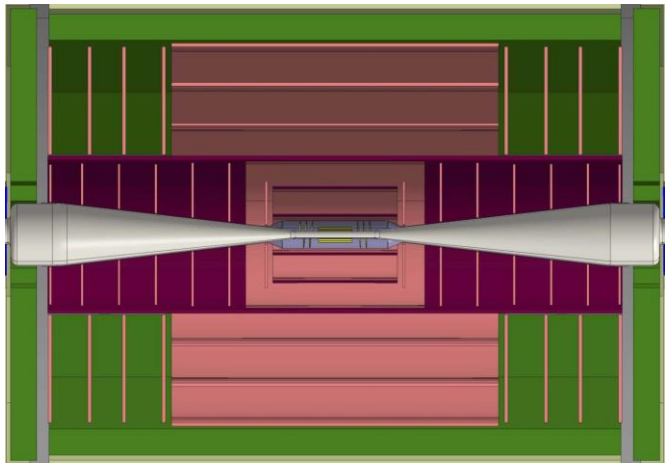
Outline

- Requirements
- The process
- The CLICTD detector channel
- Chip interface
- Summary and status

Requirements

- Requirements for a monolithic chip for the CLIC silicon tracker:

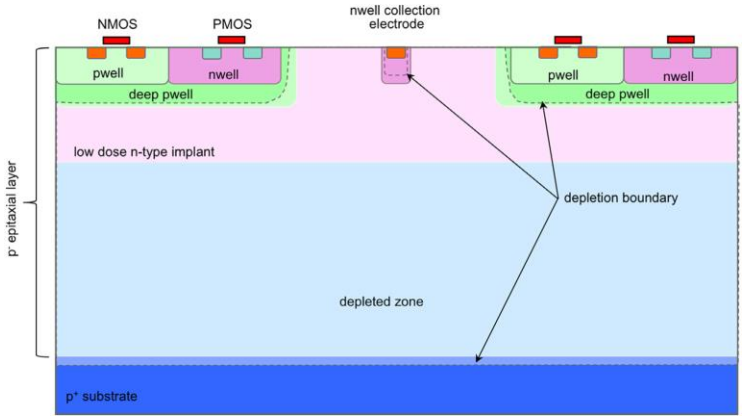
- Channel dimensions:
  - Single point resolution in one dimension $\leq 7\ \mu m$
  - Length of short strip/long pixel: $1\ -10\ mm$
- Energy measurement (Time over Threshold):
  - 5-bits resolution
  - For time walk correction and improving spatial resolution
- Time measurement (Time of Arrival):
  - 10 ns bin, 8-bits
  - No multi-hit capability
- Material budget 1 – 1.5% X_0
  - $\sim$200 µm for silicon detector and readout
- Power consumption below $150\ mW/cm^2$
  - Power pulsing, duty cycle $\sim$ 500 ns / 20 ms



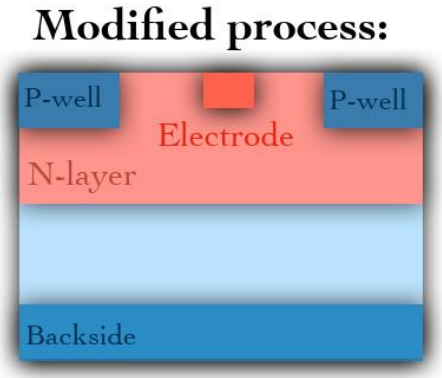
Requirements available at CLICdp-Note-2017-002 (D. Dannheim, A. Nurnberg): https://cds.cern.ch/record/2261066

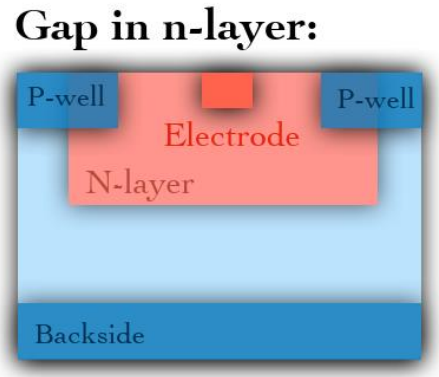
The process

- Design of monolithic active pixel sensor in TowerJazz 180 nm CMOS imaging process



- Segmenting the n-layer is expected to increase the lateral field in the pixel corner and result in improved timing resolution



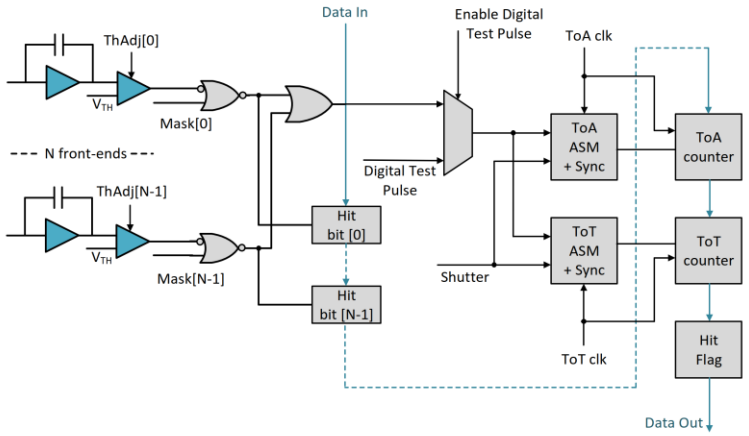


W. Snoeys, M. Munker

The CLICTD detector channel

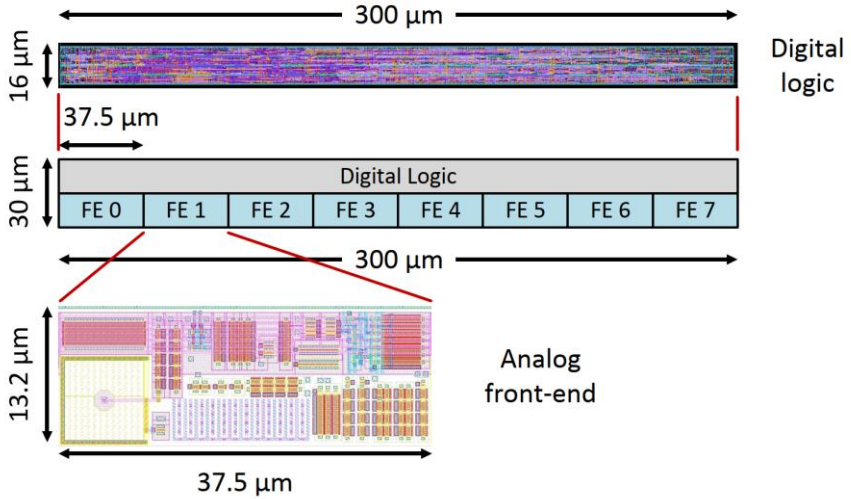
- The detector channel consists of an elongated pixel of $30 \times 300\ \mu m^2$

- The analog part is segmented in 8 front-ends (diode + CSA + discriminator + 3-bit tuning DAC)
  - To ensure prompt charge collection in the diodes



- Digital part: $\sim 16 \times 300\ \mu m^2$
- Clock frequency 100 MHz (measurement) / 40 MHz (readout)
- Readout with zero compression (at channel level) is available
  - Data output:
    - Hit flag (1 bit)
    - ToT (5 bits)
    - ToA (8 bits)
    - In-channel hit map (8 bits)

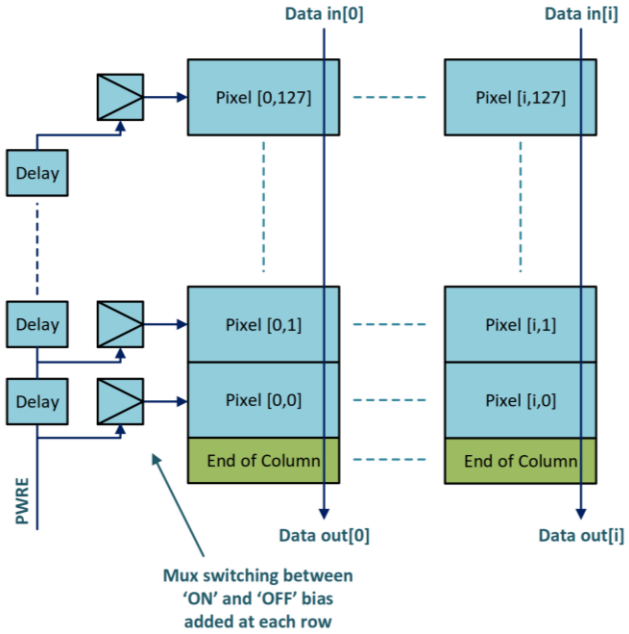
Mode	Description
Nominal	8 bits ToA + 5 bits ToT
Long counter	13 bits ToA
Photon counting	13 bits photon counting

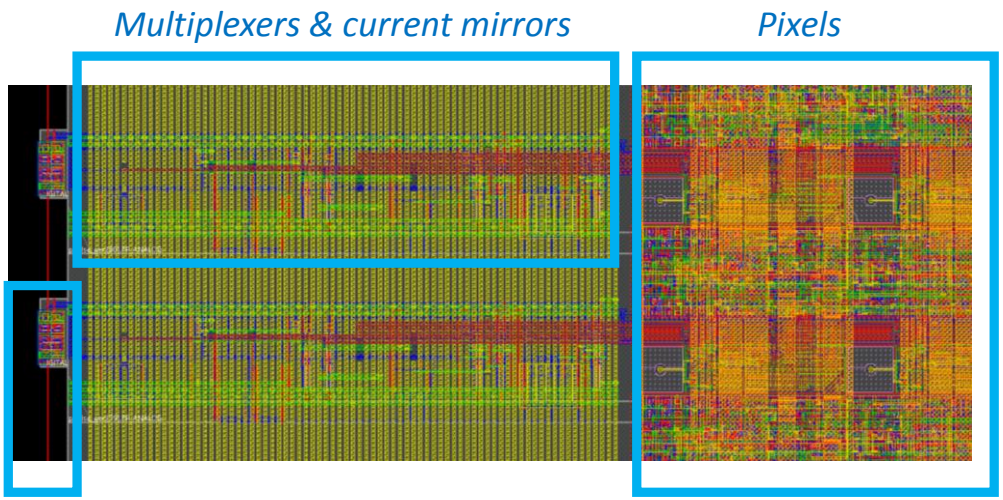


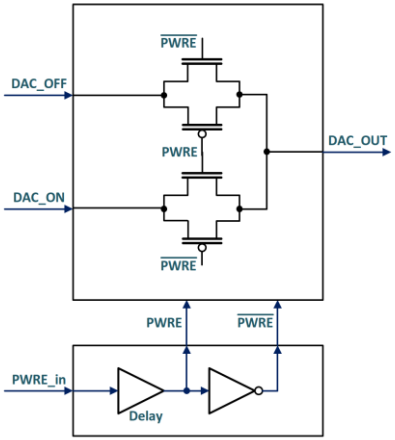
Column / matrix integration

- The CLICTD pixel matrix contains 16 columns
  - Total sensitive area: $4.8 \times 3.84\ mm^2$
  - Each column consists of 128 channels and one End-of-Column
  - Test pulse can be enabled only for selected columns
  - Analog biasing signals are connected to the side of the matrix

- Power pulsing
  - Analog: Multiplexing between “ON” and “OFF” DAC values
  - Digital: Power pulsing signal delayed (<1 ns) between consecutive rows
  - Cells are placed to the left side of the matrix

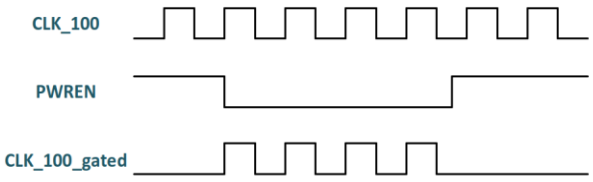




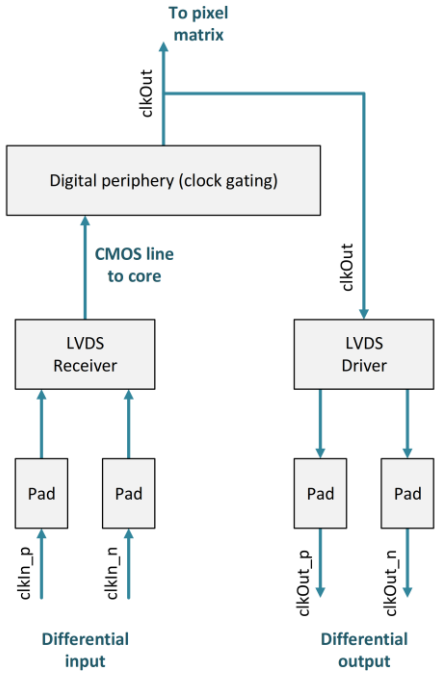


Clock distribution

- Two clocks are provided as inputs to the CLICTD chip
  - Measurement clock (100 MHz), Readout clock (40 MHz)
  - Clocks are multiplexed before arriving to the pixel matrix. Multiplexing is performed at the “End-of-Column” block, placed at the bottom side of each column
  - The slow control clock line (SCL) is treated as a different, lower frequency clock
- The **100 MHz** (measurement) clock is gated with the power pulsing signal
  - No clock distributed in matrix when in standby
- The **40 MHz** (readout) clock is gated in the digital periphery
  - Enabled in the matrix only during readout / configuration
- Constraints are added between the DATA_OUT / ENABLE_OUT pins and CLK_OUT
  - Delay from clock to data output is constrained to < 3 ns

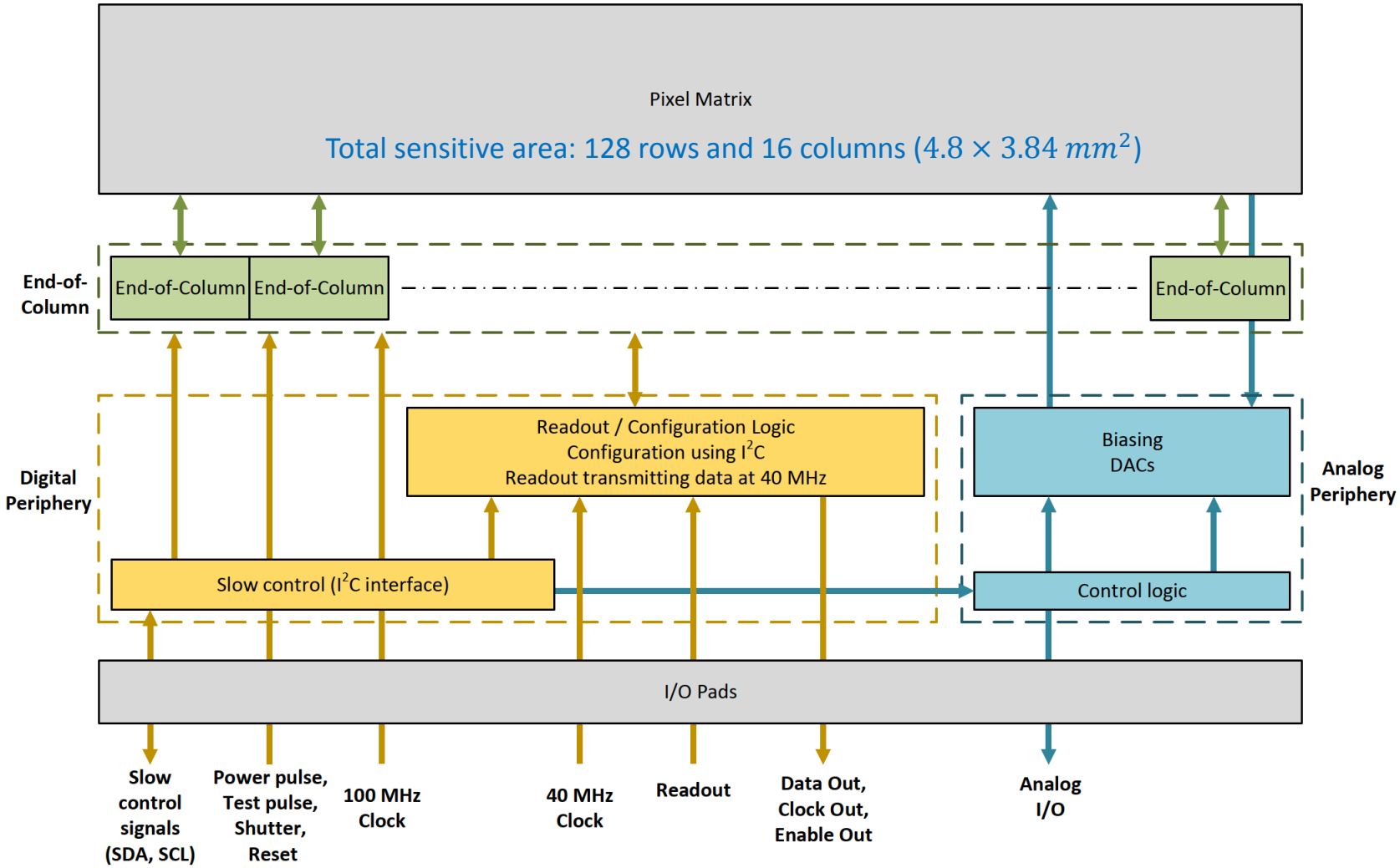


100 MHz clock



40 MHz clock

CLICTD chip block diagram

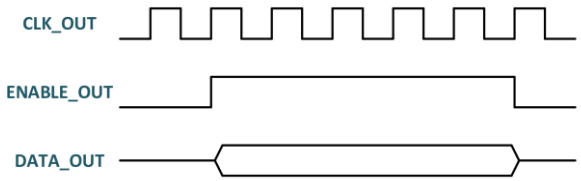


Chip interface

- I^2C interface is used for the slow control of the CLICTD chip

- Configuration data are shifted in the matrix using the slow control interface (I^2C)
  - A total of 41 configuration bits is shifted in per channel
    (in two stages, since the area does not allow for 41 flip-flops)
  - Total configuration time: ~1.9 s

- Serial readout at 40 MHz
  - Compressed readout at channel level:
    - 22 bits are read out for channels that have been hit
    - 1 bit read out for channels that are not hit
    - Readout time ~ 70 µs (for CLICTD matrix size, using compression, 1% occupancy)
  - ENABLE_OUT signal is used to synchronise with DAQ (along with clock output)
  - CLK_OUT, DATA_OUT and ENABLE_OUT are differential outputs



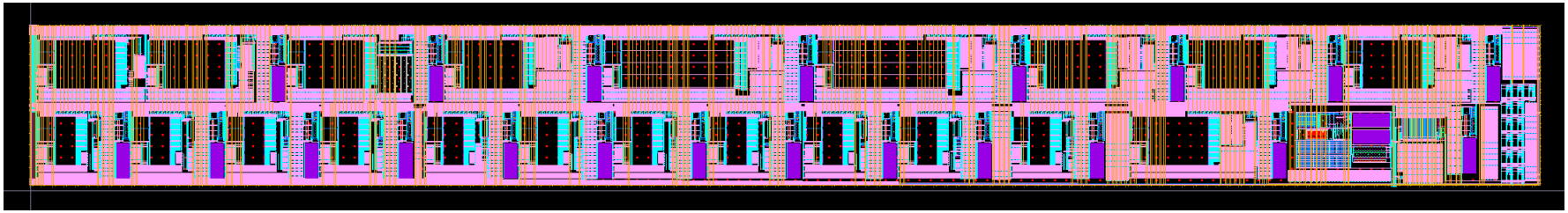
- Differential signals:
  - 2 LVDS receivers (CLK_100, CLK_40)
  - 3 LVDS drivers (CLK_OUT, DATA_OUT, ENABLE_OUT)
  - Blocks re-used from ALPIDE libraries

Analog periphery

- Biasing DACs (binary weighted current source)
  - Option to overwrite one of the internally generated biasing voltages by an external voltage (ANALOG_IN pin)
  - Option to monitor one of the internally generated voltages (ANALOG_OUT pin)

- Bandgap reference
  - Block re-used from ALPIDE libraries
  - Option to overwrite the internal reference by an externally provided voltage (REF pin)

- Analog periphery dimensions: $\sim 3800 \times 400\ \mu m^2$



I/O interface

- Wire-bond pad dimensions: $88 \times 150\ \mu m^2$
- Pitch: 100 µm

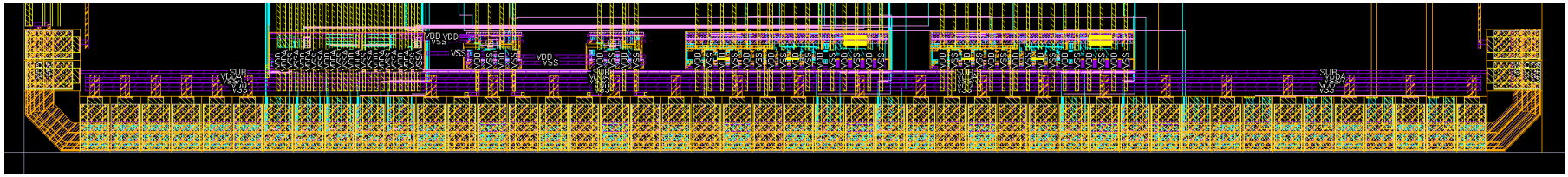
Pin	Dir.	Domain	Description
SDA	I/O	Digital	I^2C data line
SCL	I	Digital	I^2C clock line
PWREN	I	Digital	Power pulsing enable signal (set to '1' for standby)
TPULSE	I	Digital	External test pulse signal
READOUT	I	Digital	External pin to issue readout
SHUTTER	I	Digital	Shutter signal
RSTN	I	Digital	Reset signal (active low)
ENABLE_OUT	O	Digital	Enable data output (differential line)
CLK_100	I	Digital	100 MHz acquisition clock (differential line)
CLK_40	I	Digital	40 MHz readout clock (differential line)
DATA_OUT	O	Digital	Serial data output (differential line)
CLK_OUT	O	Digital	Clock output (differential line)
ANALOG_IN	I	Analog	Analog input
REF	I	Analog	Reference voltage
ANALOG_OUT	O	Analog	Analog output
VDDA	I	Analog	Analog power supply (6 pins)
VSSA	I	Analog	Analog ground (6 pins)
VDDD	I	Digital	Digital power supply (7 pins)
VSSD	I	Digital	Digital ground (7 pins)
PWELL	I	PWELL	P-well bias (2 pins)
SUB	I	SUB	Substrate bias (2 pins)

CMOS I/O

LVDS I/O

Analog I/O

Power Supplies



Power consumption

- Pixel matrix :
  - Analog → Power pulsing
    - Analog front-end is set to “Power Off” mode between subsequent bunch trains
    - Sufficient time should be provided for the circuit to power on before acquisition
    - Analog power consumption for the pixel matrix in continuous power mode: $\sim 100\ mW/cm^2$
    - A factor of ~ 50 lower power consumption can be achieved after power pulsing
    - Average analog power consumption over the CLIC cycle: $\sim 2 \frac{mW}{cm^2}$
  - Digital → Clock gating
    - During acquisition, the clock is enabled only for the channels that detect a hit
    - During readout, the clock is enabled only for the column that is being shifted out
    - Power consumption values extracted using simulation data
    - Average digital power consumption over the CLIC cycle: $\sim 2.63 \frac{mW}{cm^2}$
- Periphery:
  - Differential drivers and receivers are the dominant consuming blocks in the CLICTD chip (22 mW/driver and 2.5 mW/receiver, at maximum bias)
  - Additional power consumed by the analog and digital periphery blocks

Update on CLICTD verification

Implemented using UVM (Universal Verification Methodology):

- Large number of operation scenarios are simulated (randomized stimuli)
- Result collection is automated
- Digital-oriented simulation environment and stimuli
- Simulations with RTL netlist successfully completed; work in progress using post-layout extracted netlist

Simulated scenarios include the chip main operation modes:

- Reset
- Configuration (matrix, acquisition mode, readout mode…)
- Applying test pulses or forcing hits at the matrix
- Readout (configuration values or acquired hits)
- Writing and reading slow control registers
- Power pulse control

Status of the verification:

- Some functional bugs have been spotted and corrected
- Some timing issues have been spotted and fixed
- Work ongoing on the latest version of the post-layout extracted netlist

Summary and status

- The CLICTD chip:
  - Simultaneous 8-bit ToA and 5-bit ToT measurement
  - Cell dimensions: $300 \times 30\ \mu m^2$
  - Sensitive area: $4.8 \times 3.84\ mm^2$ (16 columns, 128 rows)
  - Chip dimensions: $5 \times 5\ mm^2$ (including seal ring)

- Design status:
  - All blocks designed
  - Final verification (functional and physical) in progress
  - Final steps for chip integration
  - Metal and active area filling to be performed
  - Plan to submit two versions with different n-layer geometry
    - Version 1: continuous n-layer
    - Version 2: gap in n-layer
    - Segmenting the n-layer is expected to result in faster charge collection
  - Submission plan: mid-February 2019
    First GDS version to be prepared by the end of January