

# SOI detector testbeam analysis

Roma Bugiel

University of Science and Technology

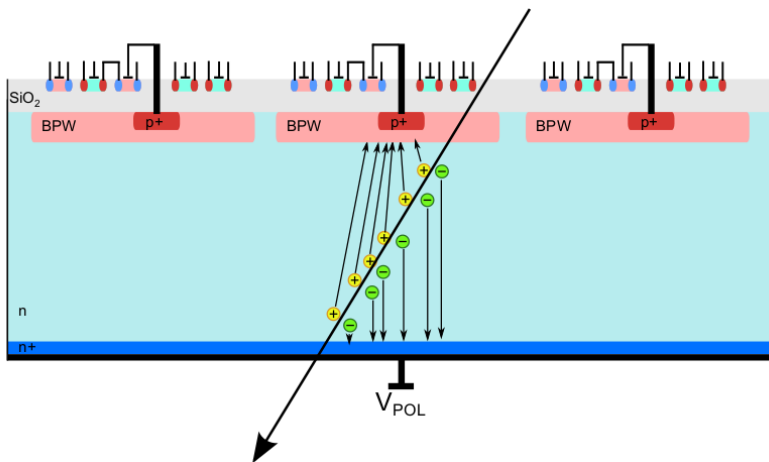
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# Introduction

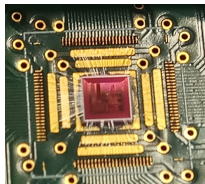
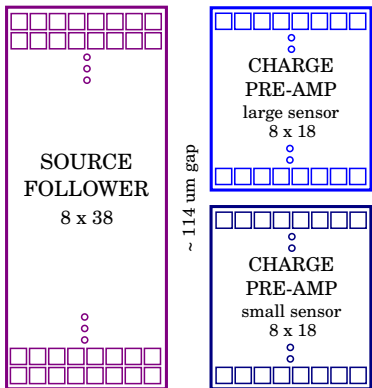


- In this talk **the monolithic detector prototype** designed in Lapis 200 nm Fully-Depleted Low-Leakage SOI CMOS technology (see Szymon's talk) is presented
- Second prototype designed in Cracow targeted to **fulfill CLIC vertex detector spatial resolution requirement**

# Detector overview

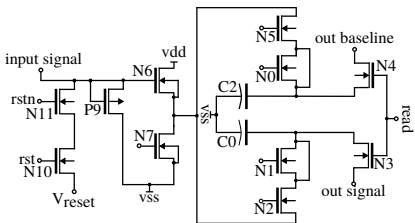
## Detector/chip general overview:

- Monolithic SOI CMOS technology used for this detector
- Two types of pixel readout architectures:
  - source follower (SF)
  - charge preamplifier (CPA) with two different sensing diode (BPW) sizes
- In total  $16 \times 38$  pixels per matrix ( $8 \times 38$  pixels for each SF and CPA)
- $30 \mu\text{m} \times 30 \mu\text{m}$  pixel size
- rolling shutter readout (integration time for one frame:  $\sim 60 \mu\text{s}$  and  $\sim 130 \mu\text{s}$ )
- Different wafer types used:
  - Float Zone (FZ-n) -  $500 \mu\text{m}$  -  $12\text{k}\Omega\text{cm}$
  - Double SOI (DSOI-p) -  $300 \mu\text{m}$  -  $> 2\text{k}\Omega\text{cm}$



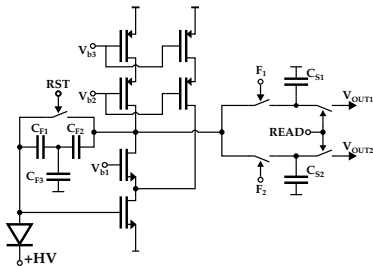
# Pixel readout electronics architectures

## SOURCE FOLLOWER



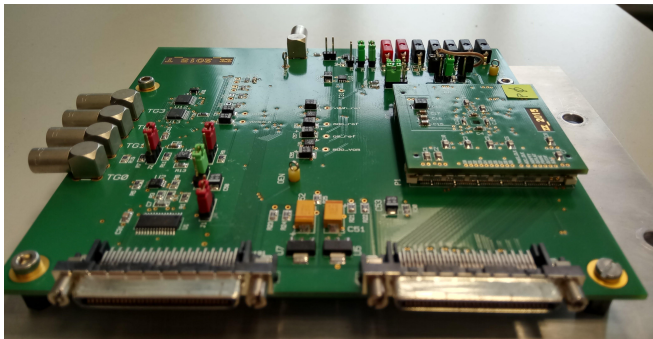
- Only the source follower at the input stage
- Correlated Double Sampling (CDS)
- $16 \mu\text{m} \times 16 \mu\text{m}$  size sensor implant (30x30 pixel size)
- Dedicated for FZ(n) wafer
- Sensitive for detector capacitance: simple architecture benefits in reducing sources of electronics noise

## CHARGE PREAMPLIFIER



- A telescopic amplifier with additional current source in input stage
- Correlated Double Sampling (CDS)
- $5 \mu\text{m} \times 5 \mu\text{m}$  and  $29 \mu\text{m} \times 29 \mu\text{m}$  sensor implants
- "T-shape" capacitor structure in feedback to decrease capacitance ( $\sim 6 \text{ fF}$ ) and increase gain

# SOI detector measurement setup



- Main readout PCB + mezzanine board with prototype SOI chips
- 12-bit external ADC on the PCB
- FPGA  $\Leftrightarrow$  PC via Ethernet
- DAQ Software using mainly ROOT 6

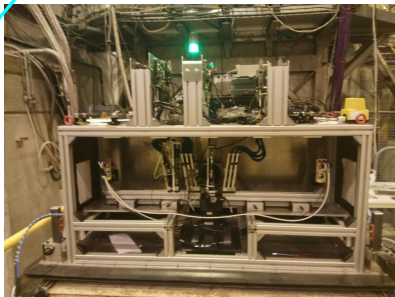
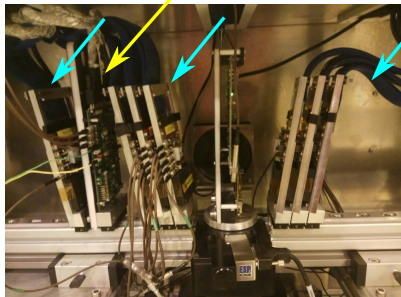
# Measurement and test-beam setup

## CERN testbeam - summer 2017

SOI chips designed in Cracow were tested on CLICdp Timepix3 telescope in the SPS-H6 beamline in June and August beam tests using 120 GeV pion beam. Three FZN and three DSOI detectors were tested.

**SOI detector**

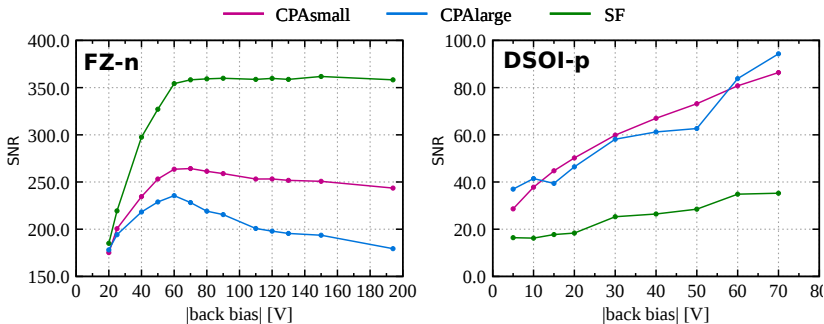
**telescope planes**



# GENERAL DETECTOR PERFORMANCE



# Signal-to-noise ratio



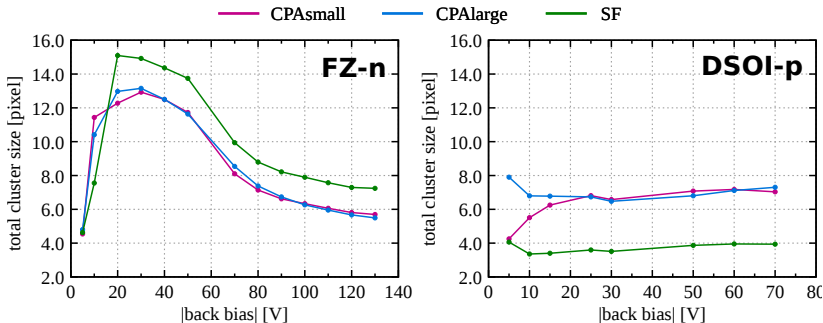
## FZ-n:

- Best SNR for SF (above 350 for full depletion)
- Good performance also for CPA matrices (CPA small:  $\sim 250$ , CPA large:  $\sim 200$ )
- Even at very low back bias voltages the SNR is high
- Fully depleted around 70 V (corresponding resistivity  $\sim 12.3 \text{ k}\Omega\text{cm}$ )

## DSOI-p:

- Not fully depleted, bias only up to  $\sim 70 \text{ V}$  (leakage of unknown source prevented higher bias)
- SNR in the range 20-100
- Charge preamplifier performance better than source follower (due to detector capacitance)

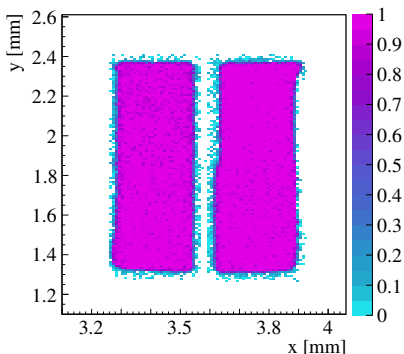
# Cluster size



- Cluster size shown for 2-Threshold-Method of clusterization (seed: 10, neighbour: 2)
- For FZ-n: high cluster size below full depletion and starts to saturate above 70V. The cluster size is relatively large: around 3 pixel in each direction for full depletion.
- For DSOI-p cluster is around 7 for CPA.

# DETECTOR EFFICIENCY

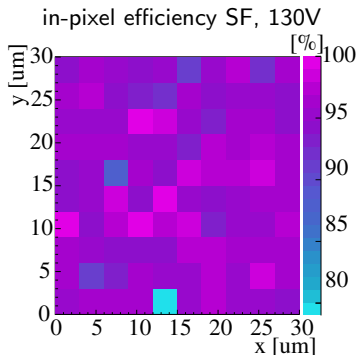
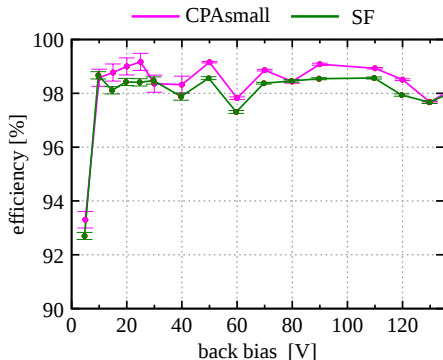
# Efficiency map



$$\text{efficiency} = \frac{\text{correlated DUT hits}}{\text{all tracks}} \quad (1)$$

- Calculated in the "inner" region of efficiency map, shown above, to be free from border effects.
- Final efficiency is taken as a mean value from the inner region of efficiency map.
- Efficiency is uniform among the matrix, showing only the drop on the edges what is expected effect.

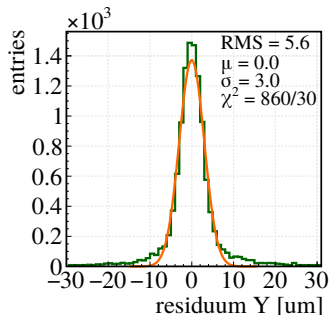
## Efficiency vs back bias voltage



- At full depletion average values are:  
 CPAsmall  $\Rightarrow$  97.98%      SF  $\Rightarrow$  96.80%
- The same results for DSOI-p above 50 V
- Within pixel efficiency looks uniform
- Inefficiency is caused most probably by the dead time in the rolling shutter readout (reset phase)

# DETECTOR SPATIAL RESOLUTION

# Fitting method



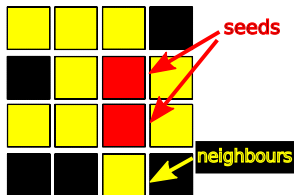
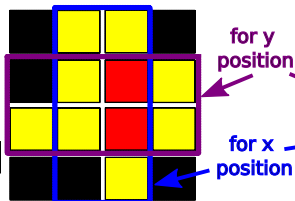
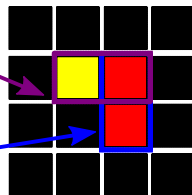
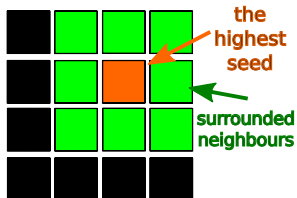
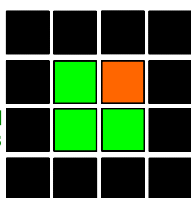
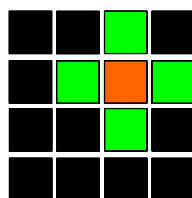
As a DUT measured resolution  $\sigma_{meas}$  the sigma of Gaussian fit make to 95.5% of the statistics is taken. The DUT final resolution is calculated as:

$$\sigma_{DUT} = \sqrt{\sigma_{meas}^2 - \sigma_{tel}^2} \quad (2)$$

where  $\sigma_{tel}$  at DUT point is  $2\mu\text{m}$ .

Just to give on overview: for example shown above RMS is  $5.6\mu\text{m}$  and  $\sigma_{DUT}$  is  $2.23\mu\text{m}$ . Fitting sum of two Gaussian (one covering the tails and one for "inner" entries), the resolution of inner Gaussian gives  $\sigma_{inn}$   $1.67\mu\text{m}$ .

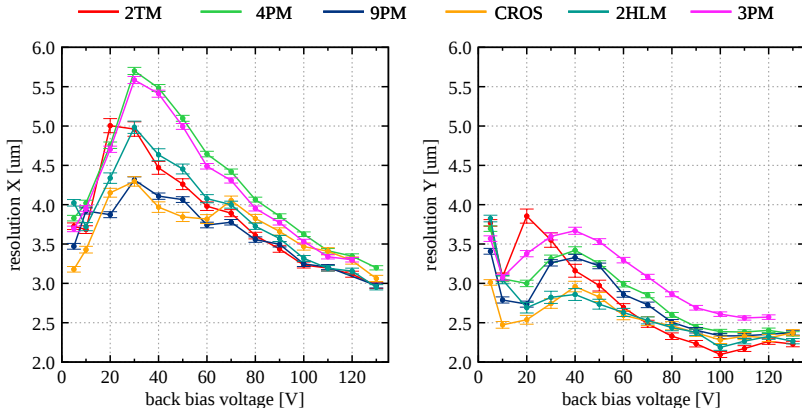
# Clusterization algorithms

TWO THRESHOLD - **2TM**TWO HIGHEST LINES - **2THL**THREE PIXELS - **3PM**NINE PIXEL - **9PM**FOUR PIXEL - **4PM****CROSS**

We have tested various options of cluster forming and its influence on spatial resolution performance.

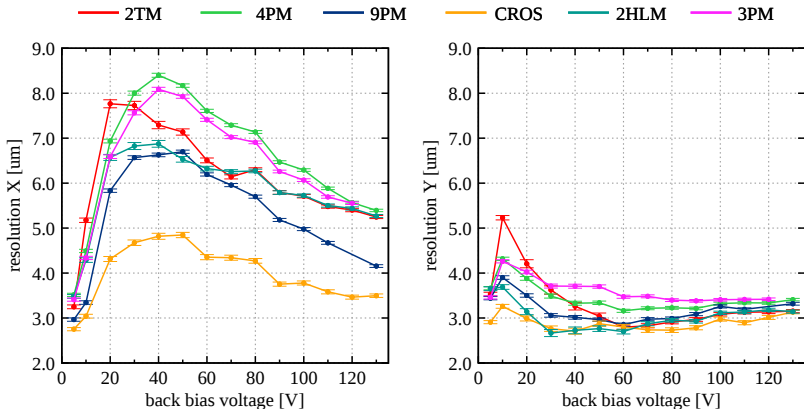


## Clusterization methods vs spatial resolution - SF



- Example presented for **source follower on FZ-n**
- x-coordinate much worse, most probably because layout of the pixel (cross-talk).
- Trends similar for all methods, absolute values may differ significantly.
- Above full depletion it is hard to distinguish which method gives better results...
- But one may notice, that for low back bias voltage taking a method limiting the cluster size benefits a lot on spatial resolution.

# Clusterization methods vs spatial resolution - CPA

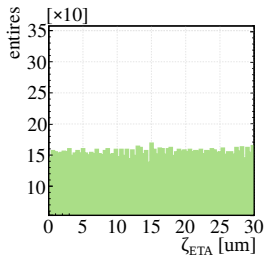
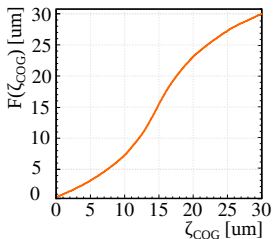
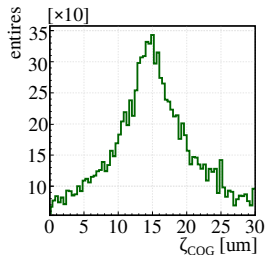


- Example presented for **charge-preamplifiers small sensing diode on FZ-n**
- The general conclusion is that the symmetric method limiting the cluster size is universal in terms of providing reasonable results for different matrices and different wafers (verified for DSOI-p).
- Thus, CROSS method (5-pixel cluster) is taken for the final results.

## Eta correction for multi-pixel clusters - SF, FZ-n example

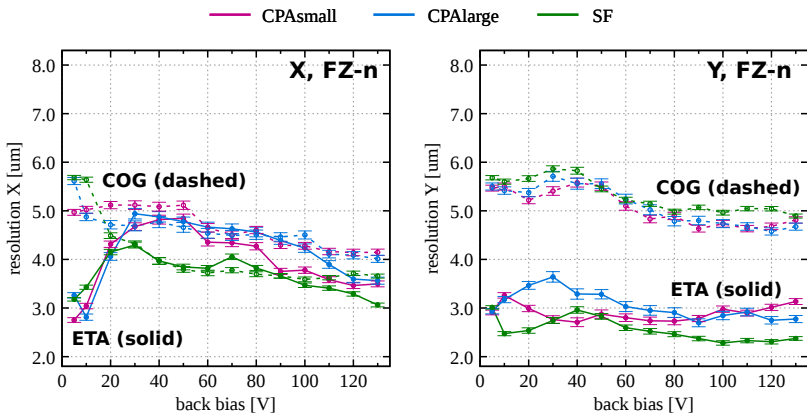
Multi-pixel cluster  $\eta$ -correction

Due to diffusion in sensor the charge sharing between neighbouring pixels is not linear. Eta correction of hit position is proposed, projecting the COG hit position onto pixel pitch and assuming that this distribution should be uniform.



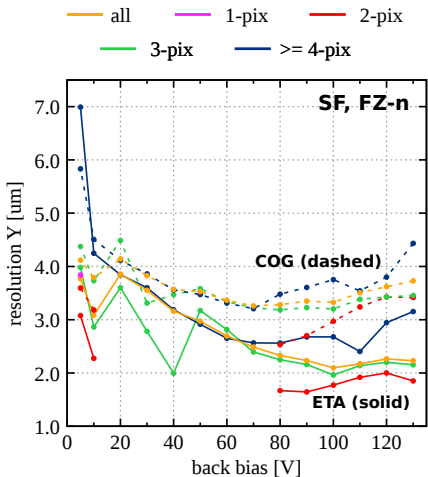
- Lets introduce variable  $\zeta_{COG} = y\%p$  as a COG hit-position projected on the pixel pitch and plot the  $\zeta_{COG}$  distribution  $P(\zeta_{COG})$ .
- Using cumulative function  $F(\zeta_{COG})$  of  $P(\zeta_{COG})$  a uniform distribution of the projected hit position  $\zeta_{COG}$  is obtained.

# $\eta$ -correction application



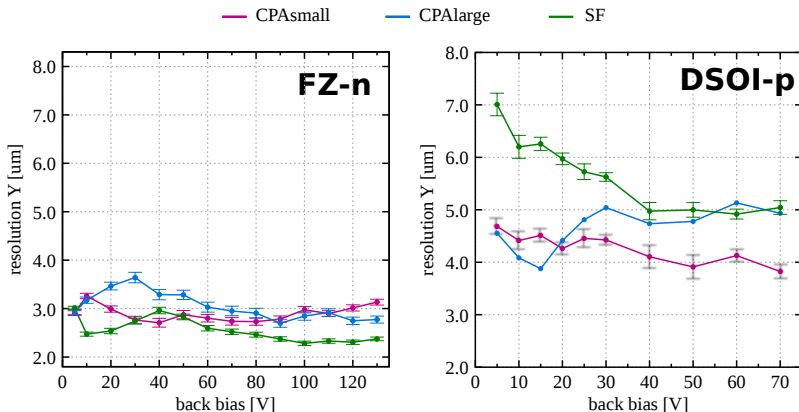
- The general influence of applied  $\eta$ -correction is shown.
- There is a significant improvement for all back bias voltages and all matrices of even about  $3 \mu\text{m}$  in y coordinate.
- For x coordinate, where cross-talk occurs, there is almost no improvement of results using  $\eta$ -correction.

# $\eta$ -correction influence on different cluster sizes



- The resolution for different cluster sizes (2TM) is presented before (dashed) and after (solid)  $\eta$ -correction.
- Proposed correction improves the resolution for all cluster types.
- The best spatial resolution performance is obtained for 2-pixel clusters.
- The resolution is worsened by 4- and more pixel clusters, probably having a high contribution from delta electrons.

## Spatial resolution summary



- the best matrix for **FZ-n**: SF giving  $2.3 \mu\text{m}$  in the best case (on  $500 \mu\text{m}$  wafer)
- the best matrix for **DSOI-p**: CPAsmall giving  $3.8 \mu\text{m}$  in the best case (on not fully depleted  $300 \mu\text{m}$  wafer)
- for FZ-n: CPAsmall and SF show below  $3 \mu\text{m}$  for almost all back bias voltages

## Conclusion

- Prototype SOI **monolithic pixel detectors** (source followers and charge-preamplifiers) have been developed and studied on the SPS beam line in 2017.
- Good **efficiency better than 97%** has been measured.
- Measurements show the **spatial resolution of 2.5  $\mu\text{m}$**  can be achieved on  $30 \times 30 \mu\text{m}^2$  pixels on 500  $\mu\text{m}$  Float-Zone wafer.

THANK YOU FOR ATTENTION!