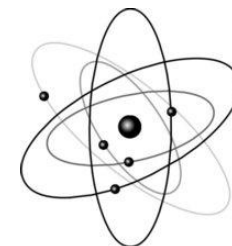
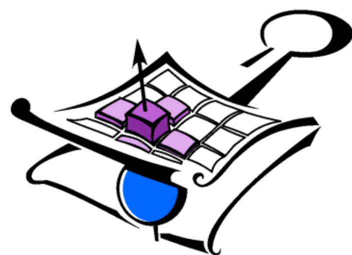




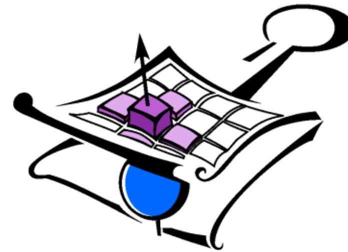
CLIPS

CLIc Pixel Soi

Status of CLIPS Monolithic SOI CMOS chip

Szymon BUGIEL

MOTIVATIONS



CLIPS
CLIc PIXEL SOI

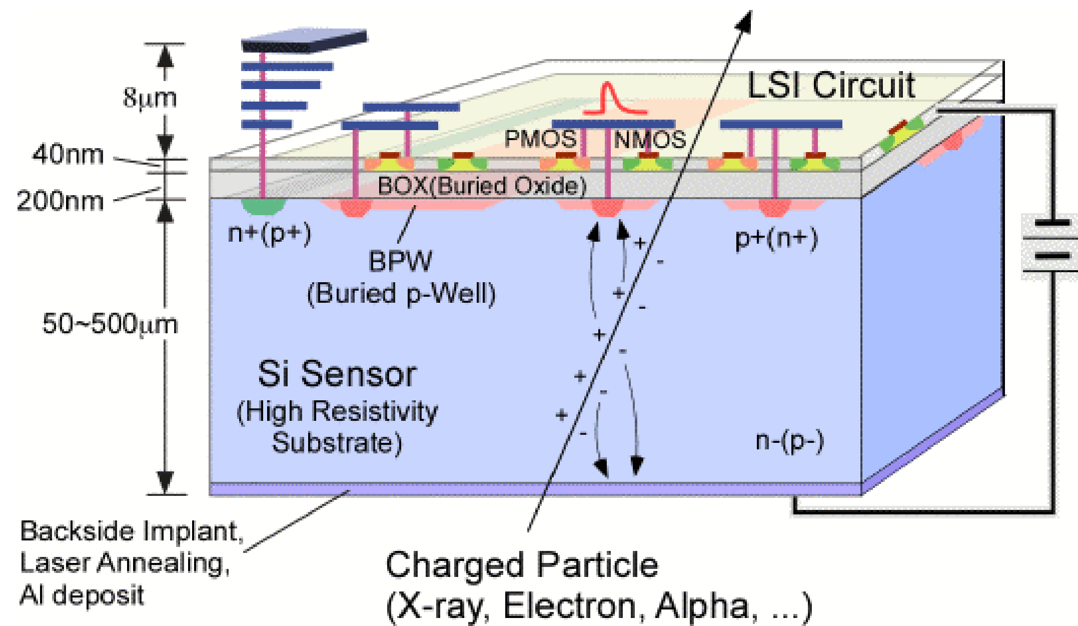
- **Specification:**
  - Targeting CLIC Vertex requirements:
    - spatial resolution < 3 um
    - timing resolution < 10 ns
    - power consumption limits not considered for this prototype (no power pulsing)
  - Snapshot readout mode
  - Variable active time (50 ns – 200 us)
  - On chip trigger to reduce the data rate
  - Analog outputs → external ADC
  - Input charge range up to 1 fC
  - Sensor thickness 100 um

- **Technology:**
  - Lapis Semiconductor
  - 200 nm Fully Depleted SOI CMOS
  - Targeting mainly double-SOI wafer (but others are still interesting)
  - p-type substrate (for DSOI wafer)

SOI TECHNOLOGY

SOI - a CMOS technology that implements the insulator layer (BOX) between the handle wafer and electronics layer

- ✓ **Reduction of parasitic capacitance**
  → power saving, higher speed
- ✓ **Reduction of leakage currents**
  → power saving
- ✓ **Elimination of latch-up effects, reduction of SEU**
- ✓ **The possibility of designing monolithic pixel detectors with high resistivity bulk, which may be thinned down to 50 um**



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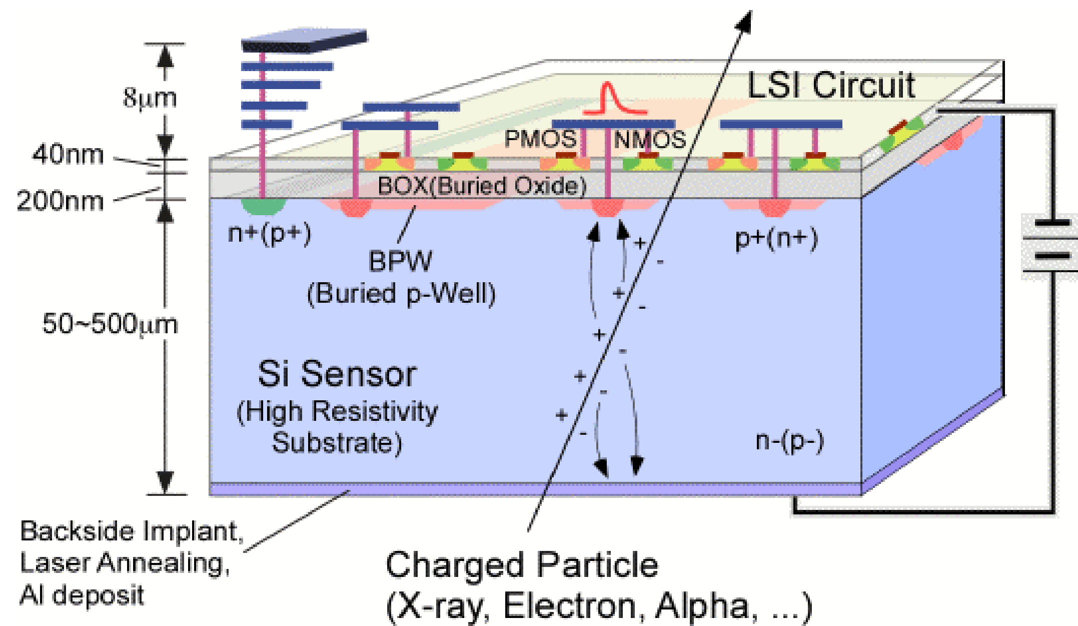


- ❑ **Radiation hardness ??**
  → Fortunately CLICs environment is not highly demanding

Available Substrates

Available substrate wafers:

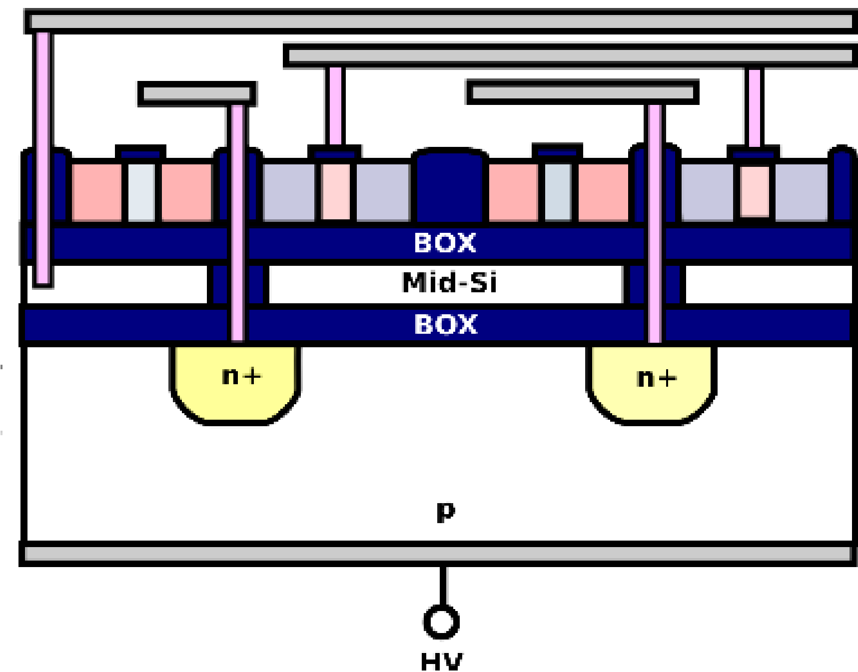
- CZ(n) > 0.7 kΩcm
- FZ(n) > 2 kΩcm (12 k Ωcm)
- FZ(p) > 4 kΩcm
- DSOI(p) > 2 kΩcm

- Design optimized for the DSOI(p) wafer, but unfortunately some problem with this substrate occured during manufacturing.

Double SOI:

- Allows to apply a proper voltage on Mid-Si to compensate the radiation effects
- Improved radiation hardness

Double SOI implements an additional BOX layer between electronics layer and handle wafer.

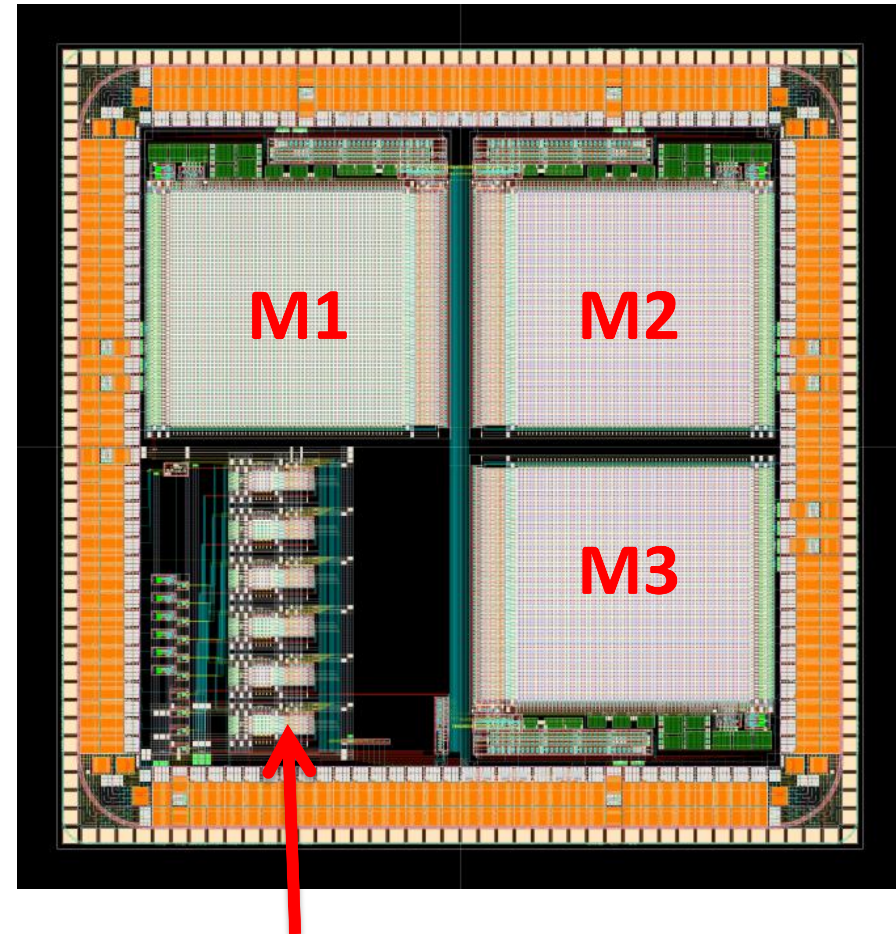


Design Overview

Design Overview

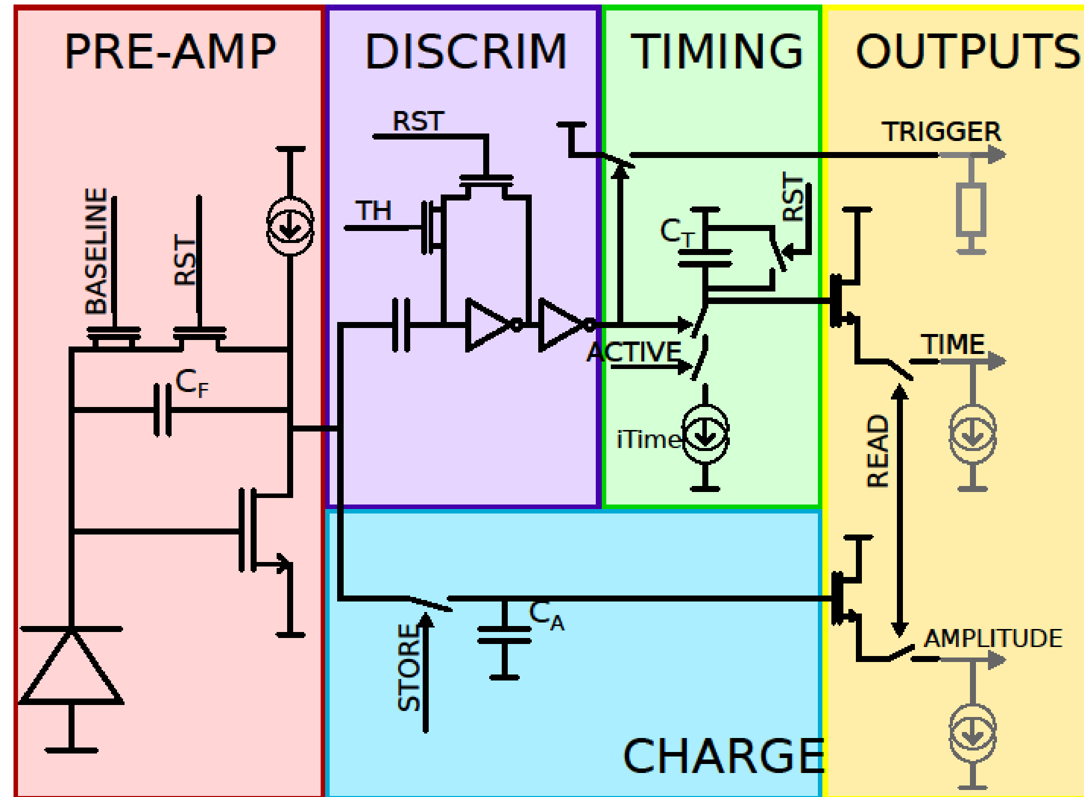
- **Matrices:**
  - Three types:
    - M1 – basic design
    - M2 – different sensor design
    - M3 – different pre-amp feedback
  - 64 x 64 pixels each
  - pixel size **20 x 20 um²**

- **Test structures:**
  - Six small 5x5 matrices:
    - Three different feedback approaches
    - With and without sensor connection
  - Test pulse injection
  - Continuous monitoring of chosen pixel behaviour



Pixel Design

- **Pre-amplifier**
  - common source architecture
  - non-resistive feedback
  - high gain: C_F ~ 1 fF (plus parasitic capacitance)
- **Time information**
  - Fine on pixel timing + global time counter on peripheries
  - No clock tree distributed over the matrix
- **Charge information**
  - Pre-amp output voltage stored on C_A



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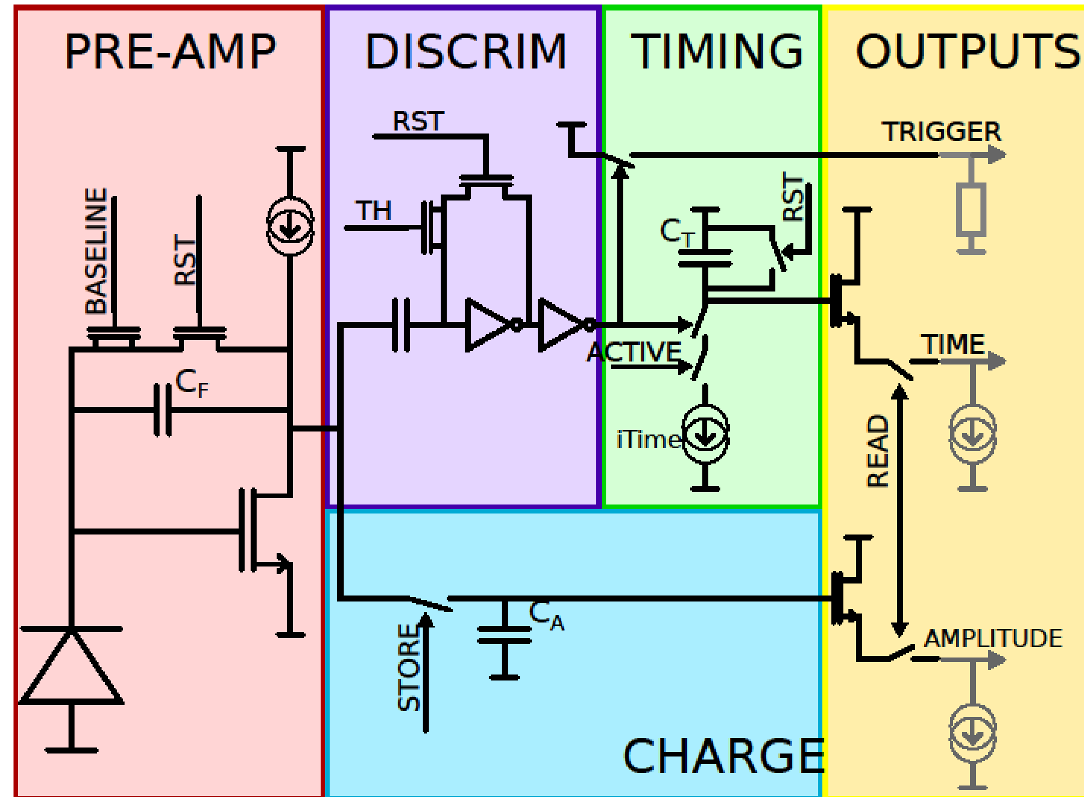
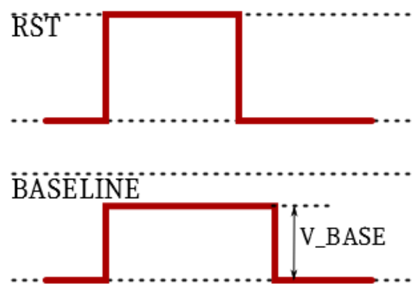
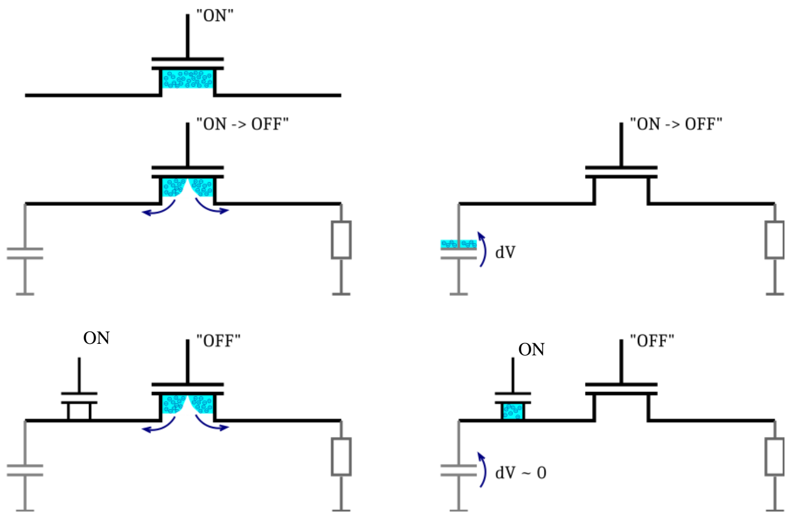
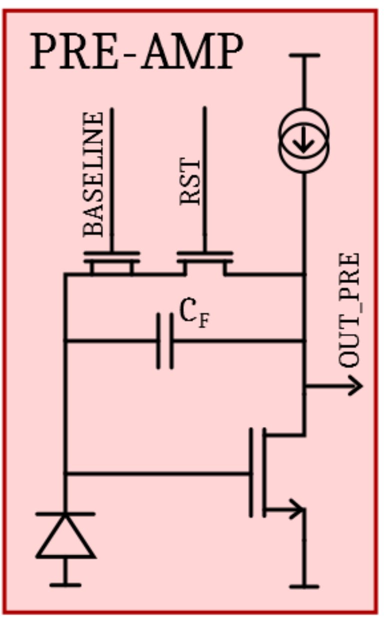


Very limited pixel size → Custom on-pixel electronics approaches

Baseline Adjustment

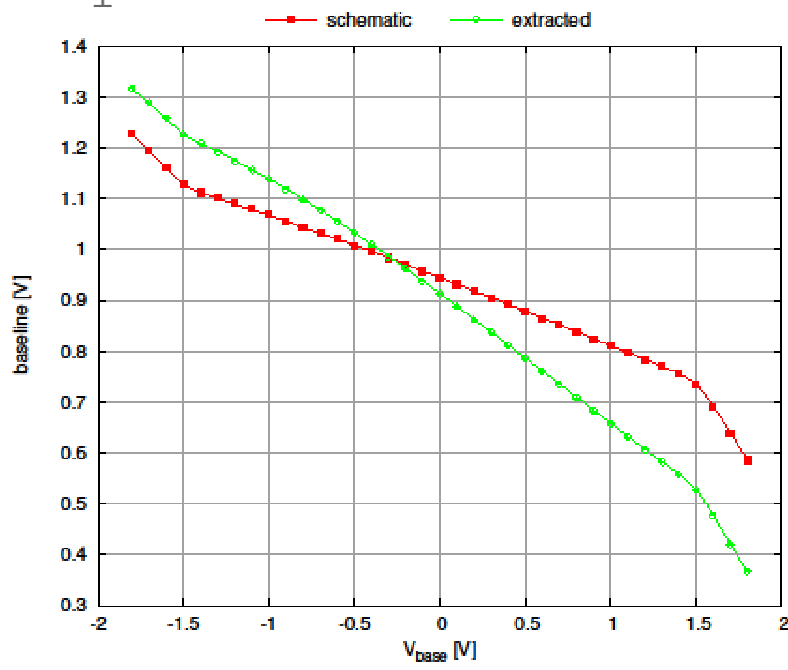






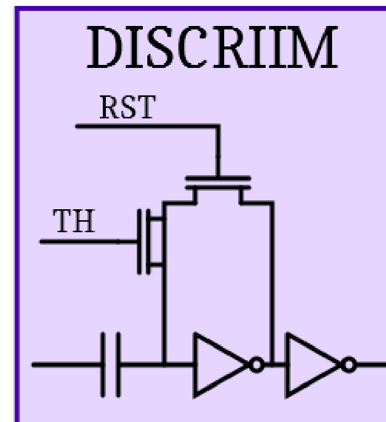
- Baseline adjustment exploits only a single transistor
- Charge injected from reset transistor induces signal
- Dummy transistor usually used to suppress this effect

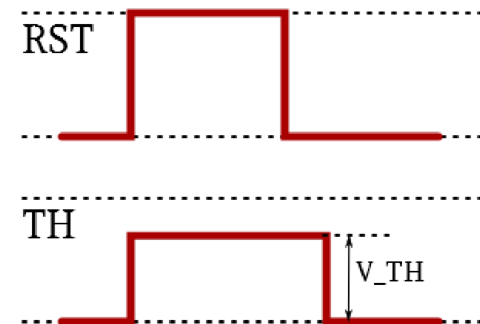
- Amount of channel charge proportional to the voltage applied to the gate
- Same mechanism may be used for the baseline adjustment
- Baseline adjustment allows for the **maximization** of the **dynamic range** as well as the operation with **both signal polarities**

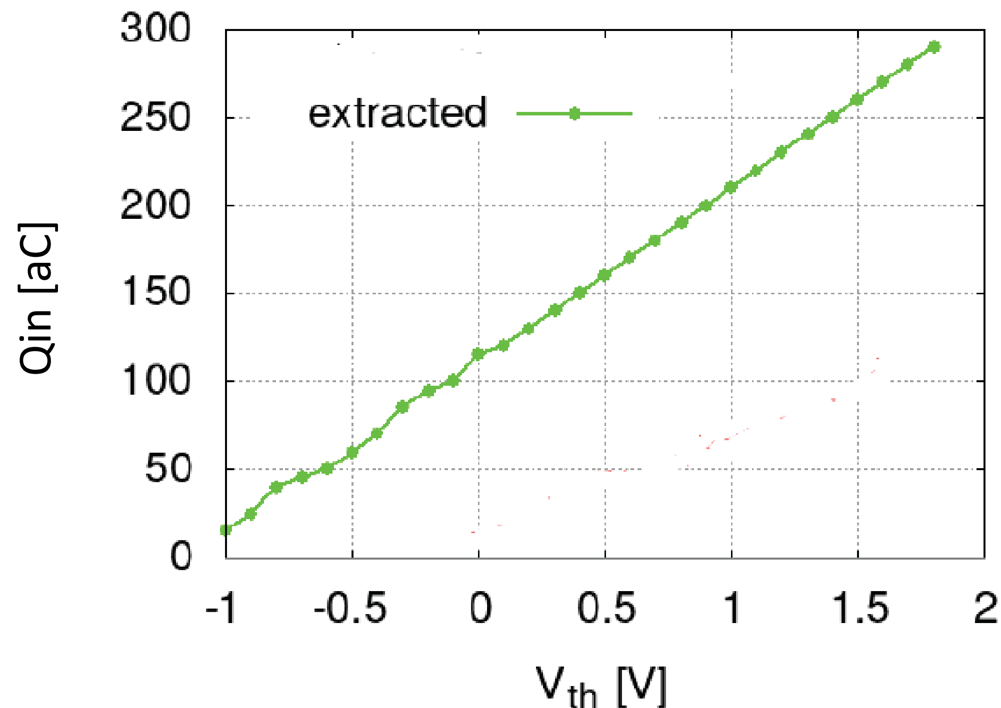


Timing: Discriminator

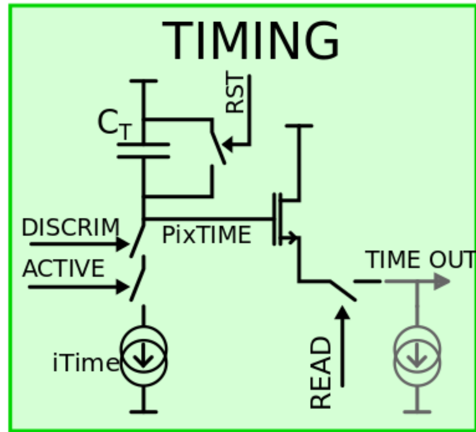
- Minimalistic architecture
  → only 6-transistors + capacitance
- Adjustable threshold
- Similar charge injection procedure as for the baseline adjustment used
- Threshold range from (0– 300 aC)

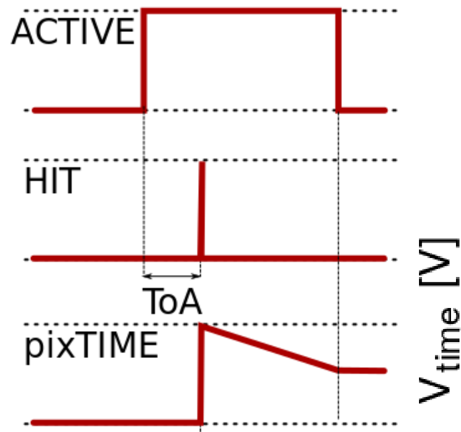


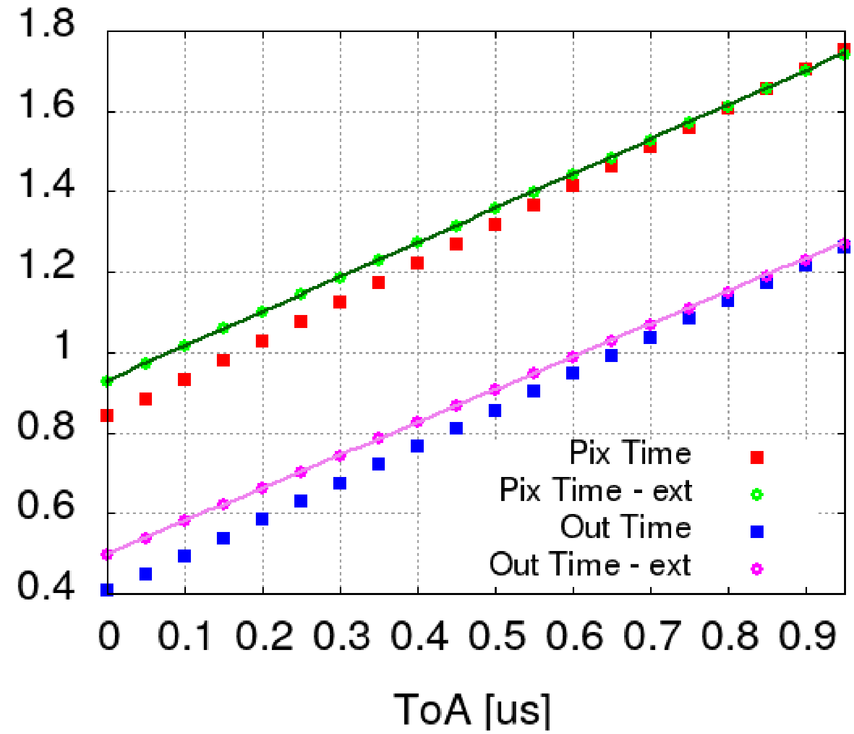




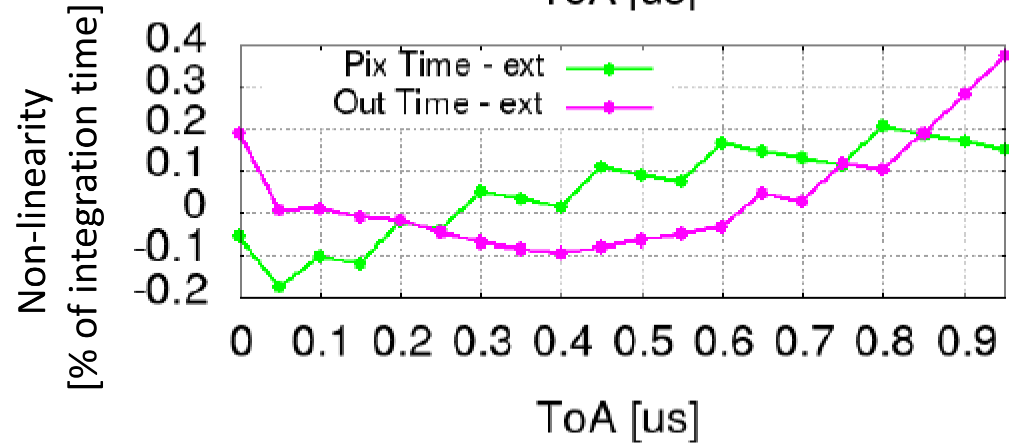
TIMING: TIME MEASUREMENT





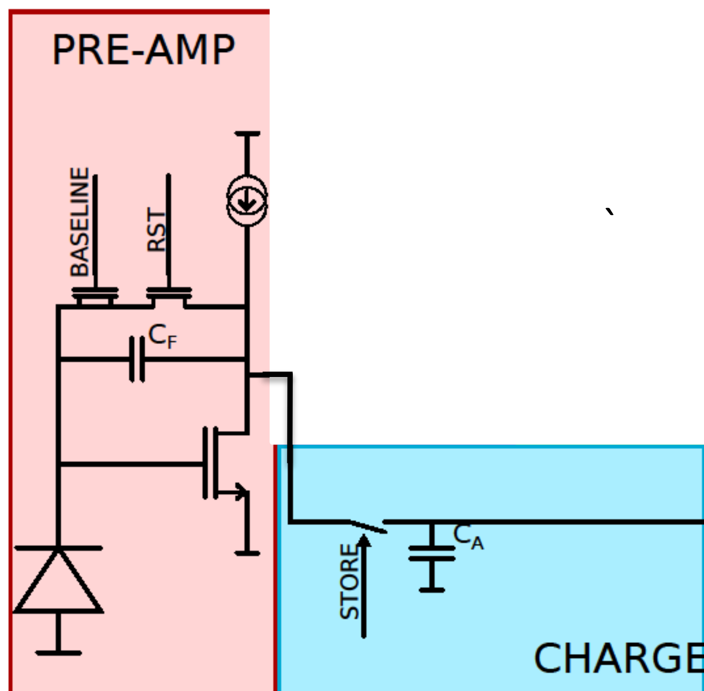


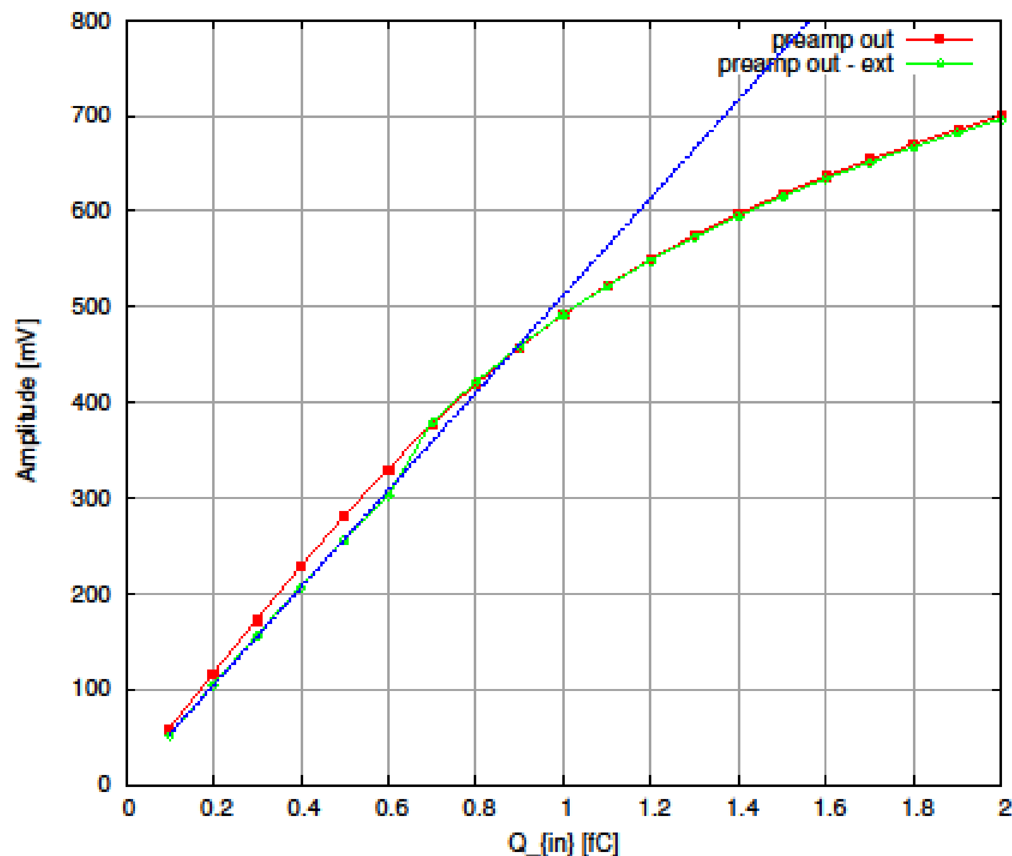
- Discharging C_T capacitance with the constant *iTime* current after hit detection
- ToA stored in analog form on C_T
- Adjustable active time
  → from 50 ns - 200 us
- Timing resolution depends on active time
- Simulations done for 1 us of active time shows non-linearities below 0.5%
  → already below 5 ns



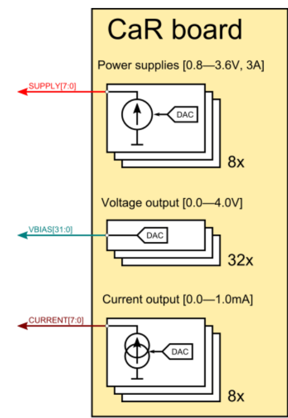
Charge measurement

- Pre-amplifier output voltage, corresponding to the input charge, stored on C_A capacitance
- Expected input dynamic range up to 1 fC → corresponding to MIP signal after thinning
- above 1 fC starts to saturate





READOUT IDEA



CaR board based readout

- Support all chip requirements
- Simultaneous readout of all three matrices

CaR board utilization

- Power supply 8 / 8
- V bias 24 / 32
- I bias 8 / 8
- CMOS in 10 / 10
- CMOS out 13 / 14
- LVDS 16.5 / 17

(12 directly, 5 converted to 10 CMOS lines)

- ADC 6 / 16

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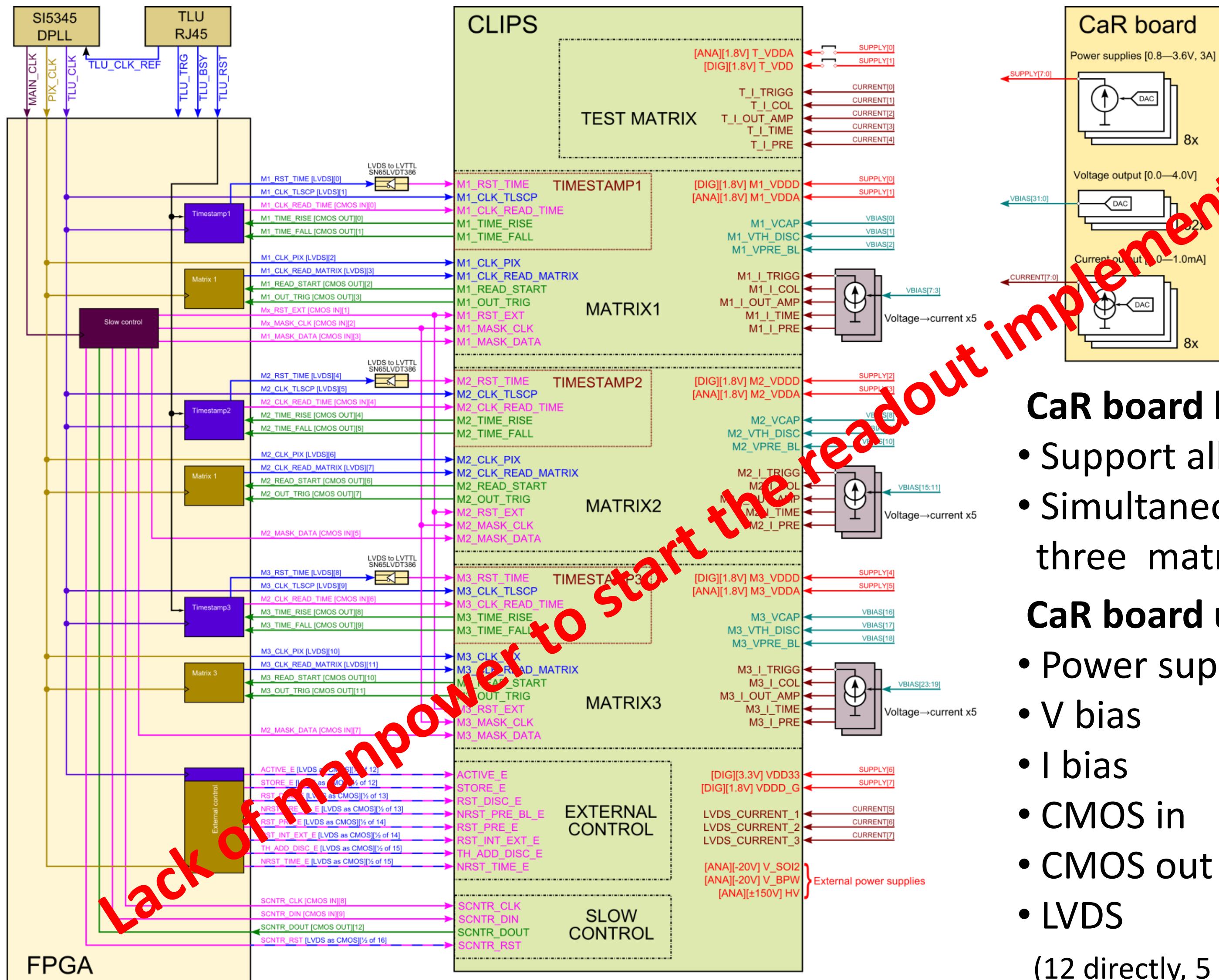

Lack of manpower to start the readout implementation !

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- Support all chip requirements
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(12 directly, 5 converted to 10 CMOS lines)

• ADC	6 / 16

Summary

- **CLIPS** detector design was **submitted** in the end of **November 2017**
- Designed to fulfill most crucial **CLIC Vertex requirements**
- There are problems with a Double SOI wafer during fabrication, but chips on **CZ(n)**, **FZ(n)** and **FZ(p)** wafers already **available**
- Status of Double SOI wafers still unclear
- First concept of **integration with CaR board** outlined
- **Readout needs to be developed** to start the measurements

Thank You for Attention!