TCAD Process and device simulation of OVERMOS, a CMOS 180nm MAPS detector

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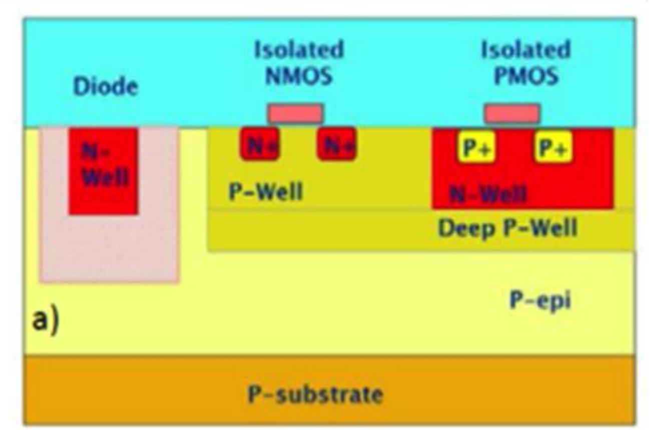
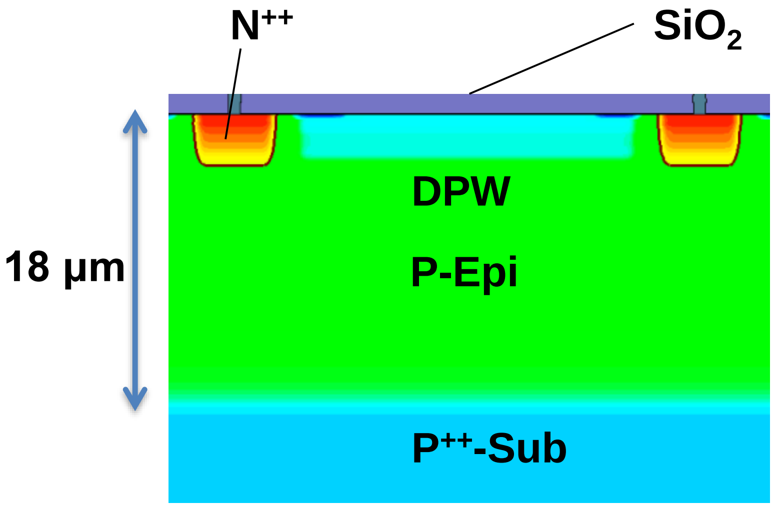
Overview

- OVERMOS description
- Charge collection of OVERMOS using calibrated laser
- TCAD simulation: comparisons of TCAD simulations with non irradiated OVERMOS devices
- Conclusions and next steps

OVERMOS description

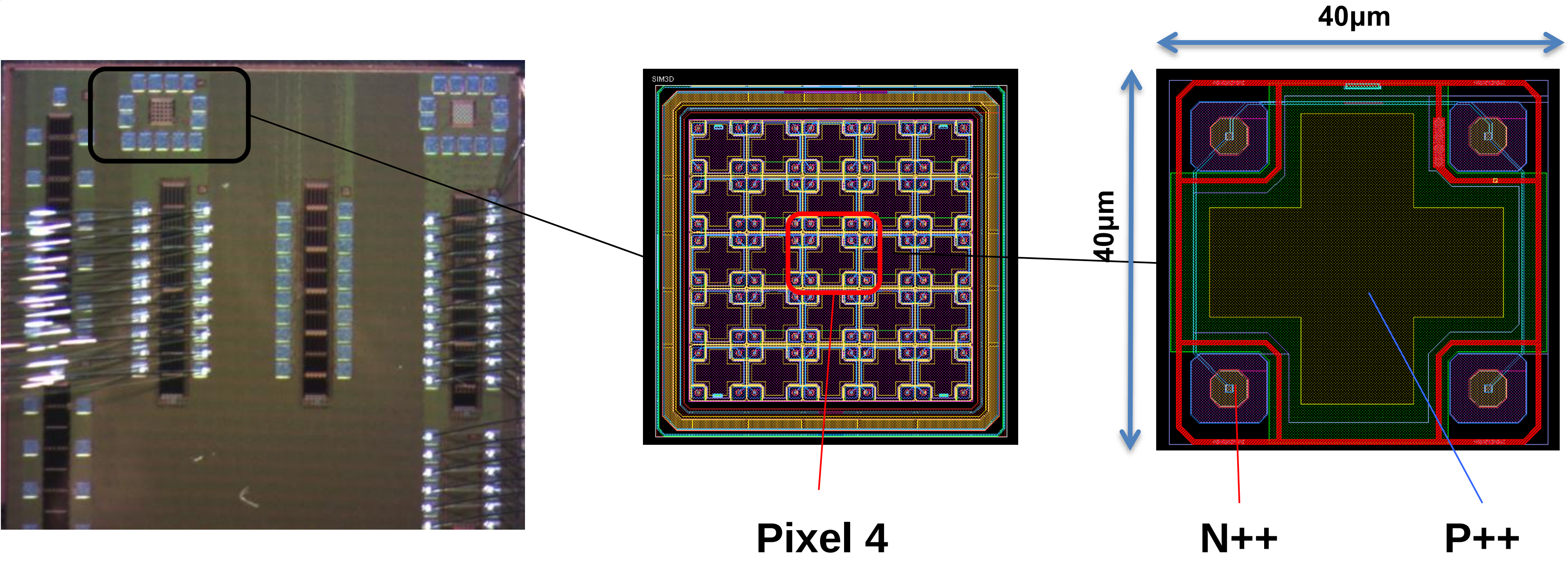




OVERMOS is a CMOS MAPS project demonstrator fabricated using:

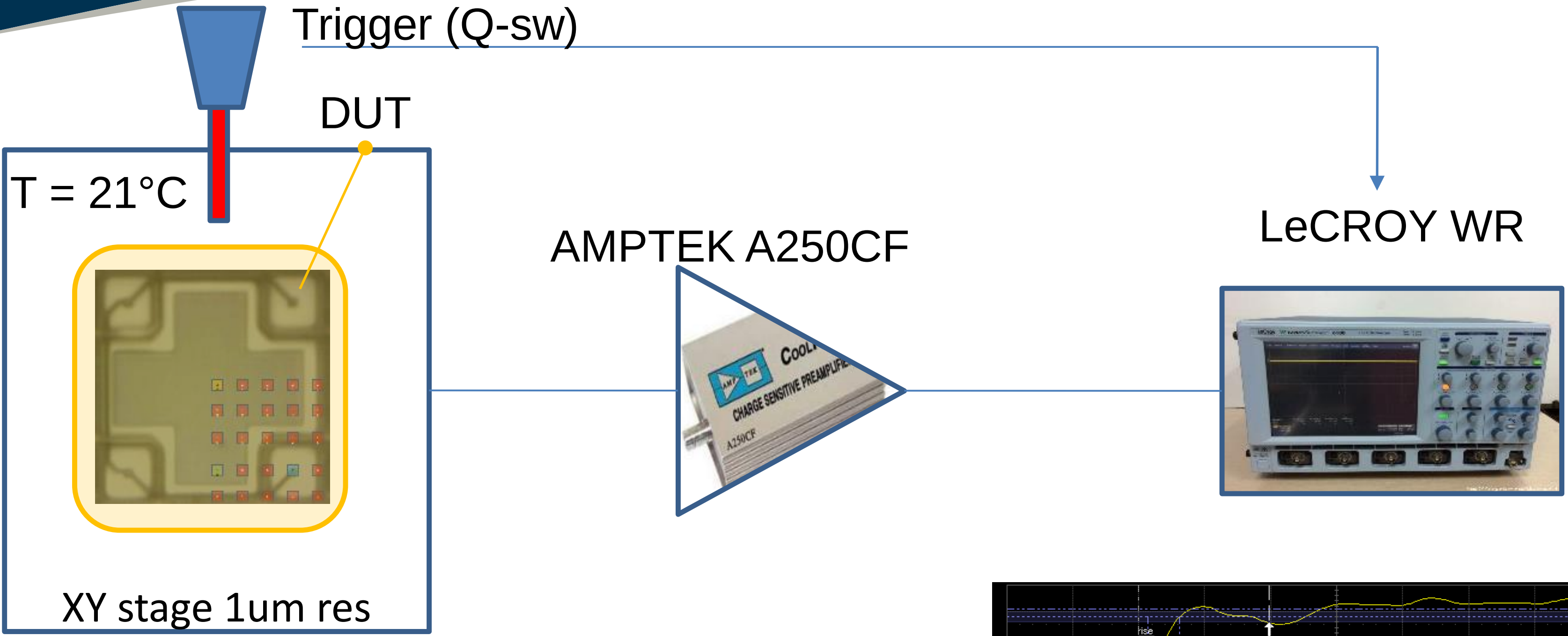
- TJ 180 nm Hi-res 18 µm thick epitaxial layer 1kOhm – cm
- Small (3.5x3.5 μm^2) n-collecting nodes
- Multi diode arrangements within pixel
- CMOS DPW ~ originally proposed for DECAL of ILC

OVERMOS description



- A TCAD modelling of fabrication process of OVERMOS has been developed to investigate and predict its performances
- OVERMOS devices have been n-irradiated to Φ [1e13,5e13,1e14,5e14]

OVERMOS Laser Test



Trigger (Q-sw)

DUT

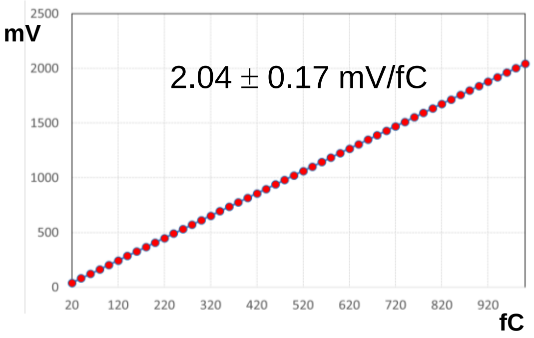
T = 21°C

AMPTEK A250CF

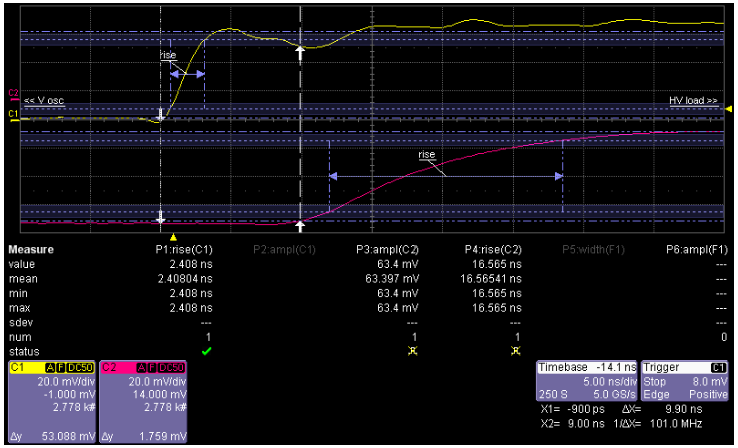
LeCROY WR

XY stage 1um res

Nd:YAG Trilite Laser



2.04 ± 0.17 mV/fC



Measure	P1:rise(C1)	P2:ampl(C1)	P3:ampl(C2)	P4:rise(C2)	P5:width(F1)	P6:ampl(F1)
value	2.408 ns		63.4 mV	16.565 ns		---
mean	2.40804 ns		63.397 mV	16.56541 ns		---
min	2.408 ns		63.4 mV	16.565 ns		---
max	2.408 ns		63.4 mV	16.565 ns		---
sdev	---		---	---		---
num	1		1	1		0
status	✓		✗	✗		

C1 A F DC50
20.0 mV/div
-1.000 mV
2.778 k#
Δy 53.088 mV

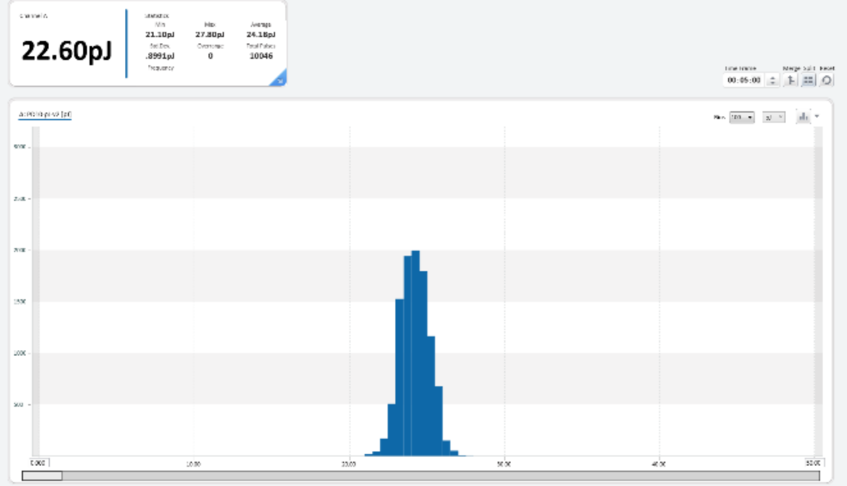
C2 A F DC50
20.0 mV/div
14.000 mV
2.778 k#
Δy 1.759 mV

Timebase -14.1 ns
5.00 ns/div
250 S 5.0 GS/s

Trigger C1
Stop 8.0 mV
Edge Positive

X1= -900 ps ΔX= 9.90 ns
X2= 9.00 ns 1/ΔX= 101.0 MHz

OVERMOS Laser Test



22.60pJ

Min 21.10pJ

Max 27.80pJ

Average 24.18pJ

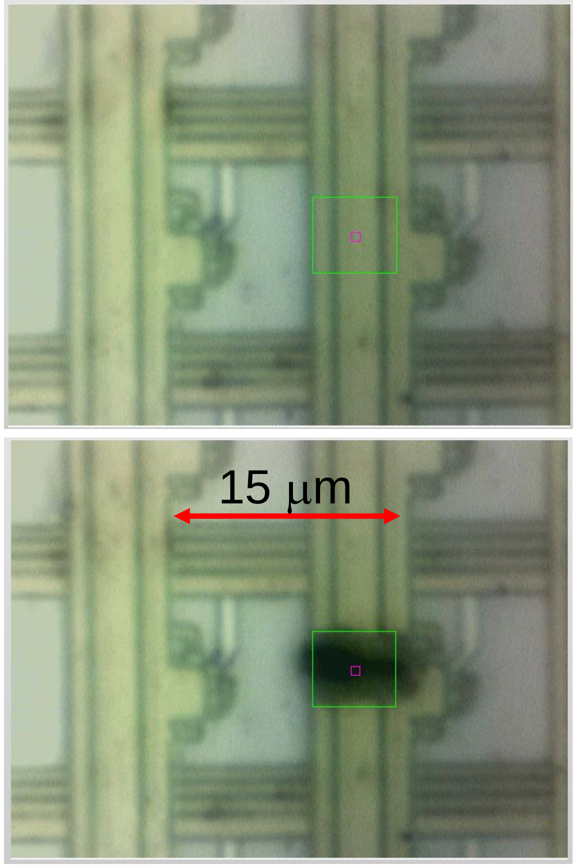
.8991pJ

0

10046

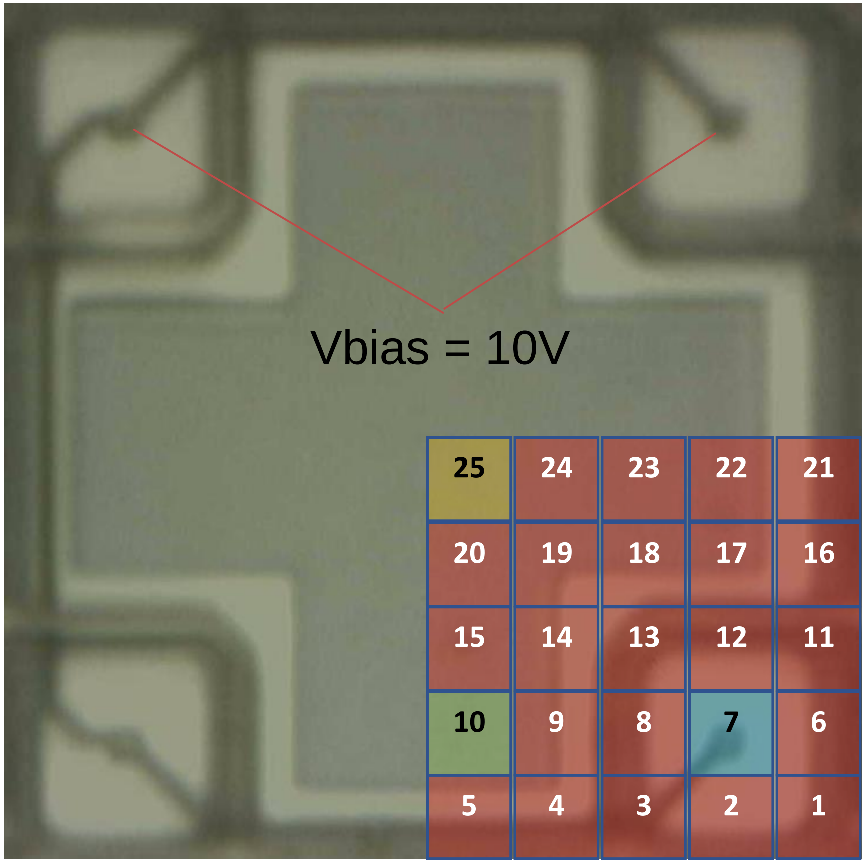
Laser energy settings, measured with Pd10-pJ:
- ~ 25 ± 0.9 pJ @ 1064 nm
- 5 ns pulse width,
- 50Hz

Shutter size set to 5 x 5 µm^2



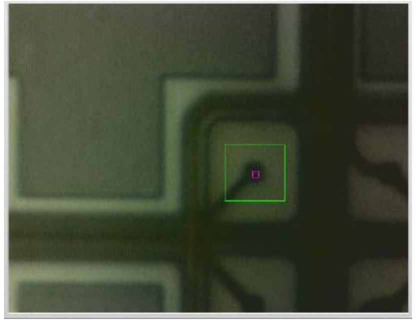
OVERMOS Laser Test

OVERMOS



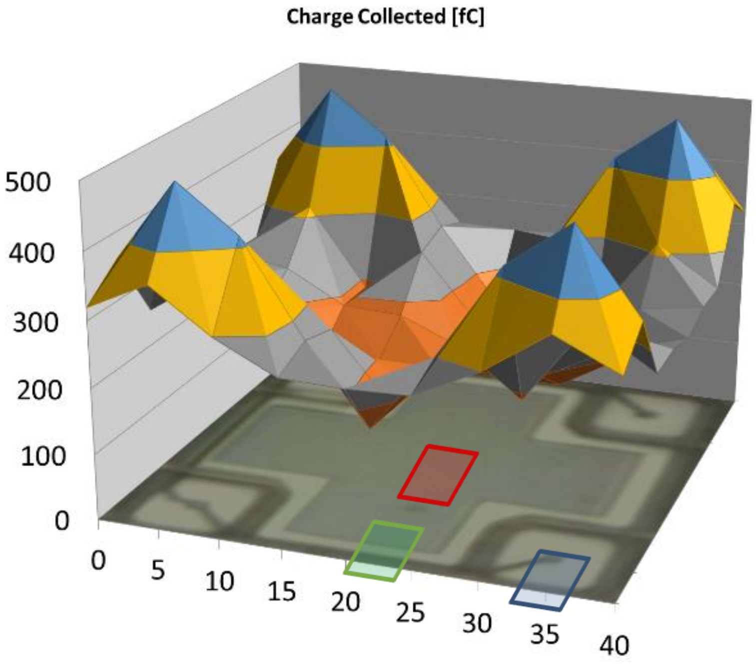
Vbias = 10V

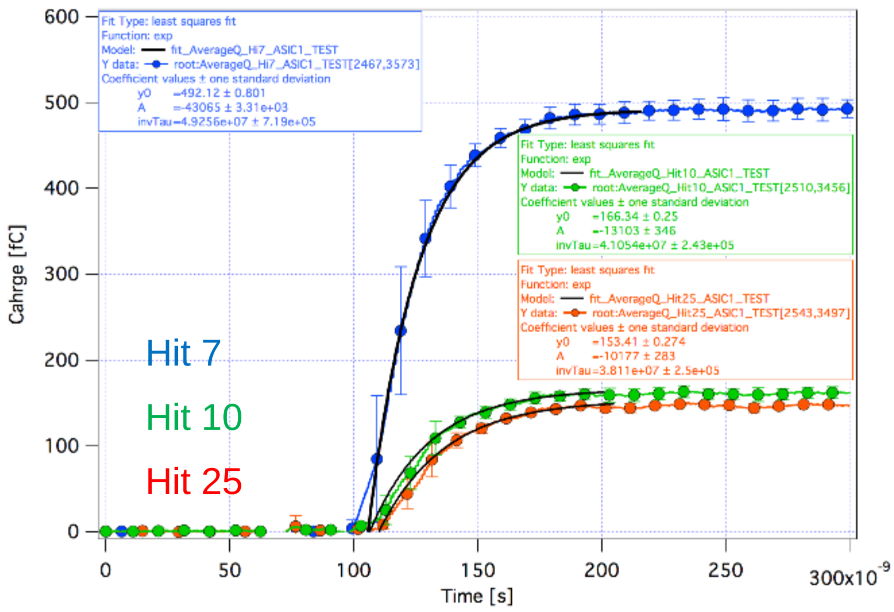
Cu shielded OVERMOS



OVERMOS Laser scan 5 x 5 μm^2 beam size
25 points, repeated over entire pixel area to give map of collected charge
The dynamics of charge collection of three points (7,10,25) is compared with TCAD simulations

OVERMOS Laser Test





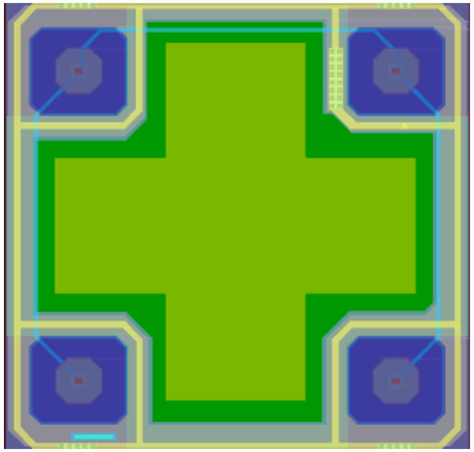
<Q> = 492.1 [fC] Collection time: 44.6±0.36 ns

<Q>= 166.34 [fC] Collection time: 53.5±0.31 ns

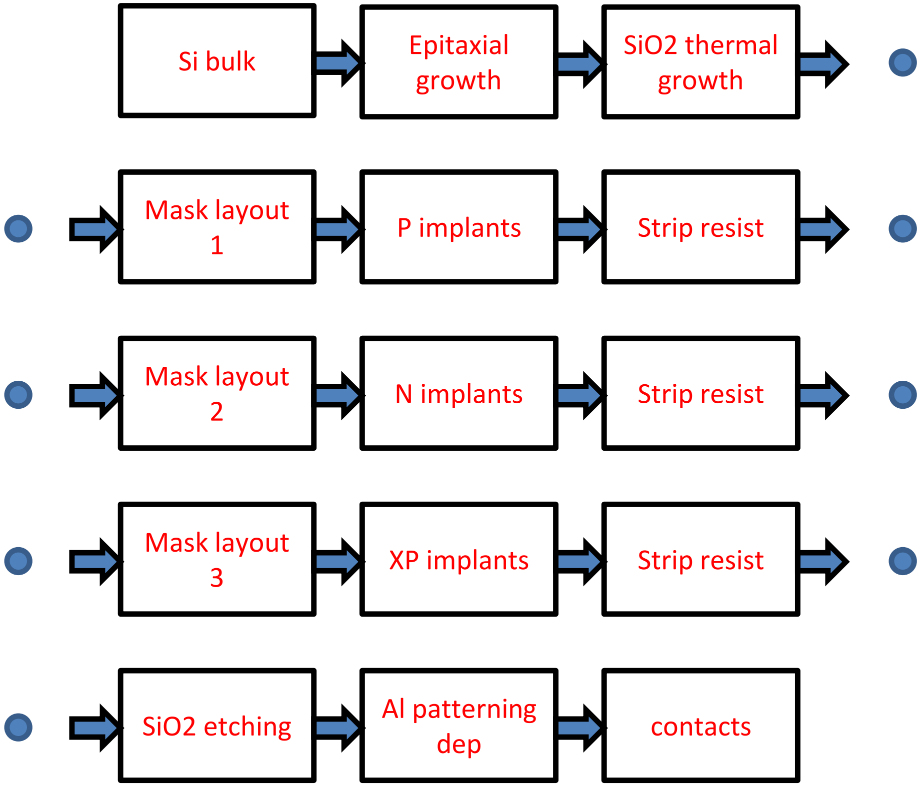
<Q>= 153.4 [fC] Collection time: 57.6±0.52 ns

OVERMOS Laser scan 5 x 5 μm^2 beam size
10 non –irradiated pixels Laser Test results

TCAD simulation



Pixel .gds



Si bulk → Epitaxial growth → SiO2 thermal growth →

Mask layout 1 → P implants → Strip resist →

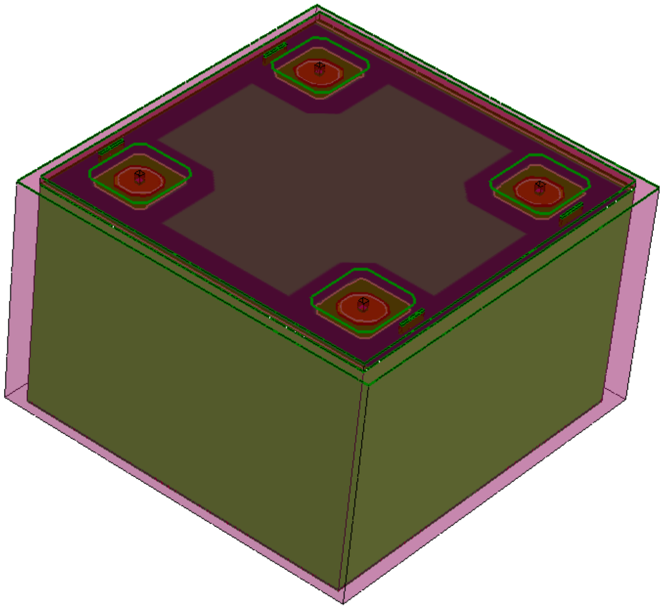
Mask layout 2 → N implants → Strip resist →

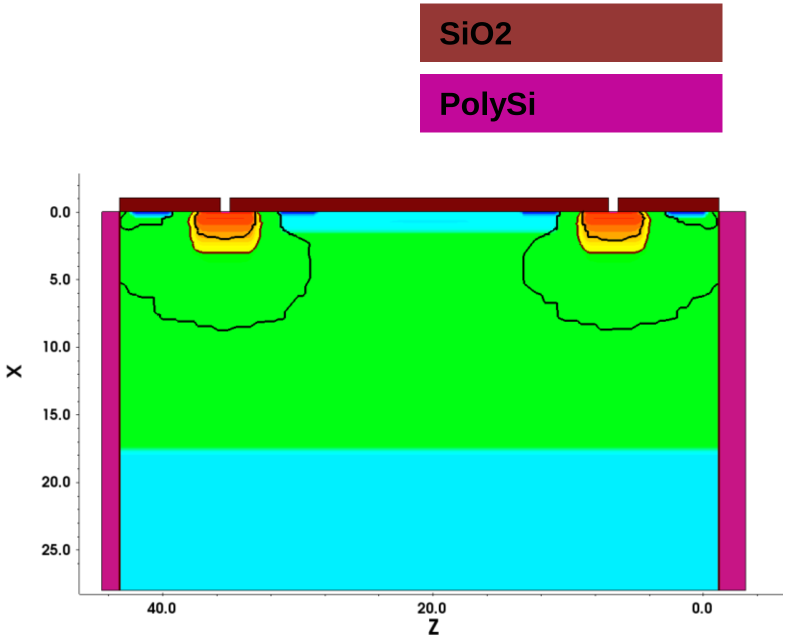
Mask layout 3 → XP implants → Strip resist →

SiO2 etching → Al patterning dep → contacts

- A simplified TJ CMOS fabrication process of OVERMOS has been implemented in SPROCESS
- Around 15 simulated steps, which include epitaxial growth on Si bulk, SiO_2 thermal growth, N/P implant, etching, thermal annealing, metal deposition, contacts placement

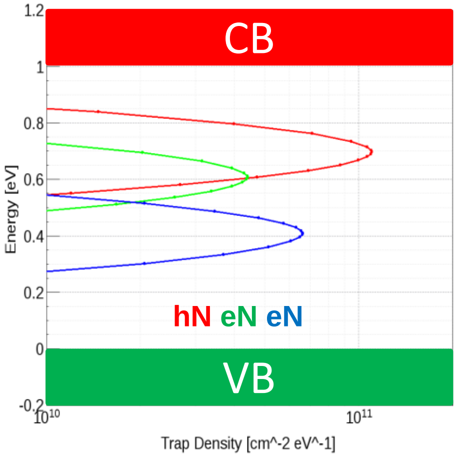
TCAD simulation

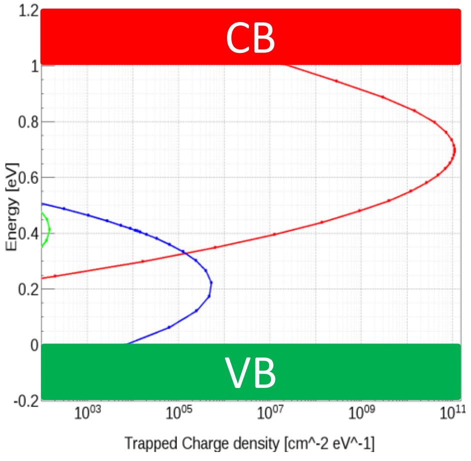




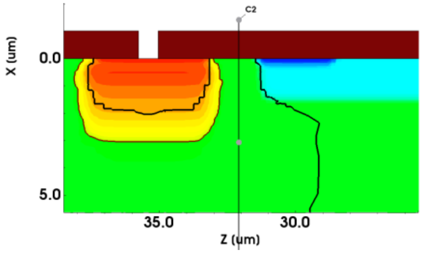
- For CC studies using Laser light, an extra PolySi box surrounds the pixel, with high SRV to simulate non-reflecting boundaries (added as an SDE directive within SPROCESS)
- Thermally grown 8.1 nm SiO_2 for interface traps effects
- Thick deposited SiO_2 for better Delaunay meshing/optical attenuation/reflection
- Emulation of $CoSi_2$ silicide for optical attenuation in non-NS regions

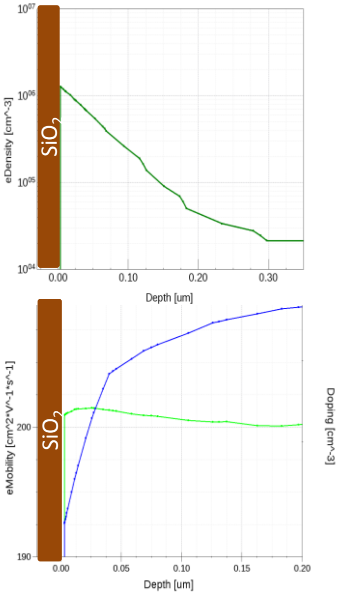
TCAD simulation





1.2e11 Oxch [0.007,10,10]





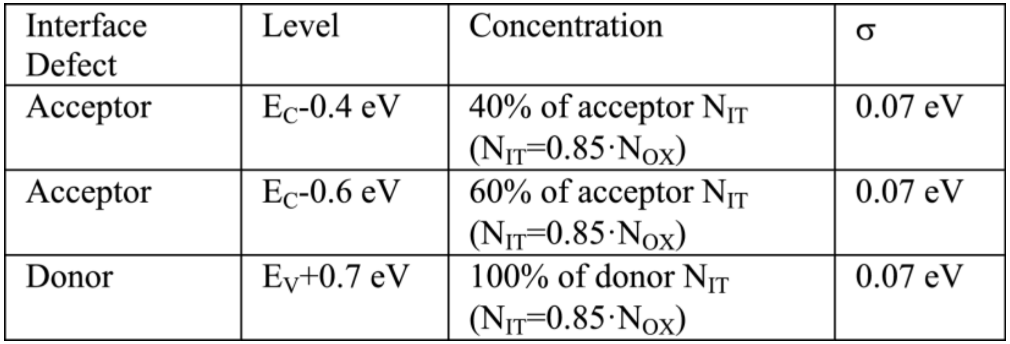
Fixed oxide-charge (**Oxch**) density and interface traps (**Oxint**) included

Interface traps distributed among 3 energy levels, Gaussian , σ = 70meV

Ratio Oxint/Oxch ~ 0.9

Simulations 1.2e11 Oxch

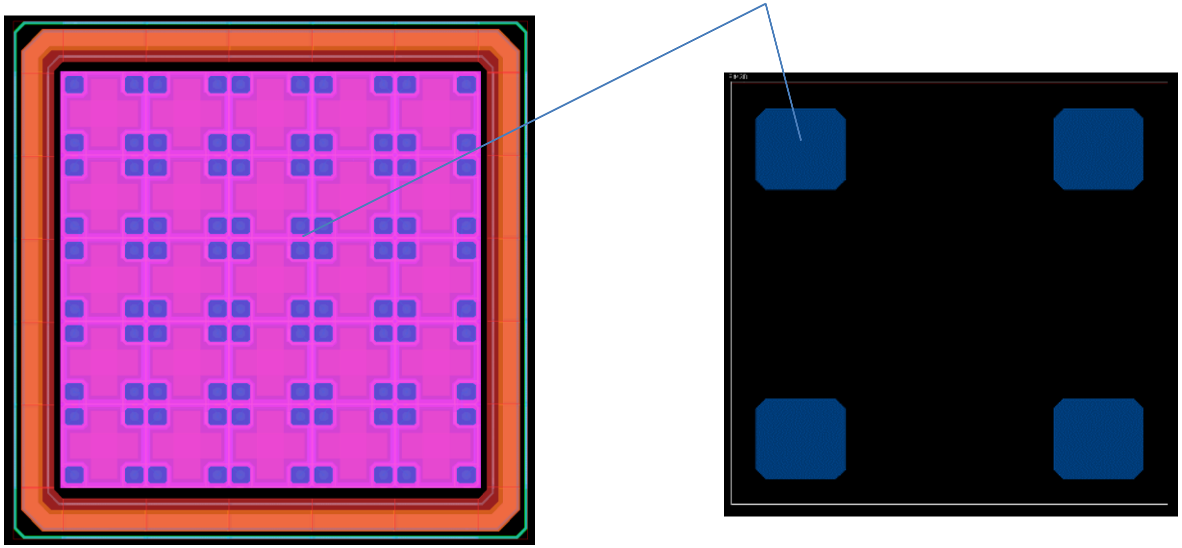
Xsection 1E-15 cm^-2

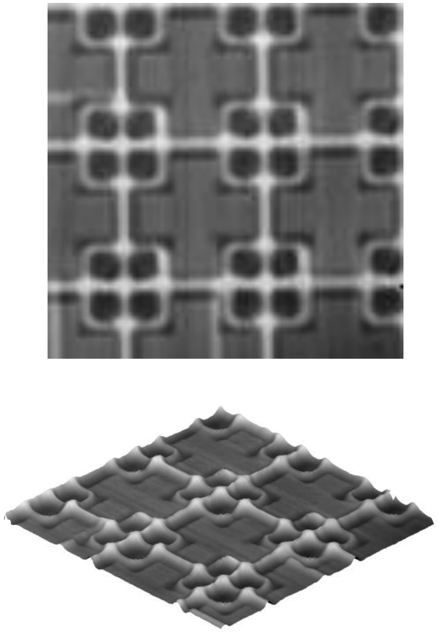


Interface Defect	Level	Concentration	σ
Acceptor	E_C-0.4 eV	40% of acceptor N_{IT} (N_{IT}=0.85·N_{OX})	0.07 eV
Acceptor	E_C-0.6 eV	60% of acceptor N_{IT} (N_{IT}=0.85·N_{OX})	0.07 eV
Donor	E_V+0.7 eV	100% of donor N_{IT} (N_{IT}=0.85·N_{OX})	0.07 eV

* ***Effects of Interface Donor Trap States on Isolation Properties of Detectors Operating at High-Luminosity LHC***, *DOI:* 10.1109/TNS.2017.2709815

TCAD simulation

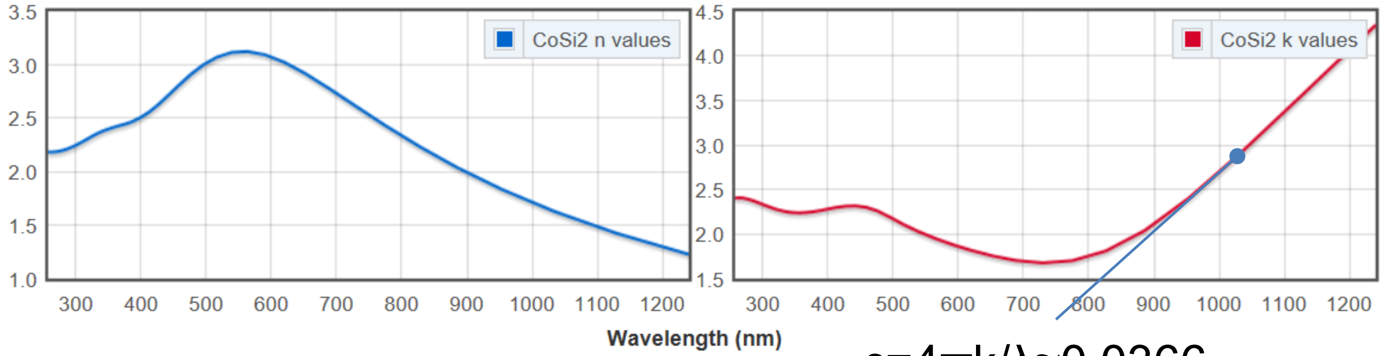




TJ 180nm SL uses $CoSi_2$ for lower delay lines
$CoSi_2$ attenuates light, reducing generated charge
Scanning using confocal microscope revealed ‘height differences’ with respect to non−NS regions

TCAD simulation

ε of $CoSi_2$



$\varepsilon = 4\pi k/\lambda \approx 0.0366$

$\exp(-0.0366 * 40) \approx 0.23$

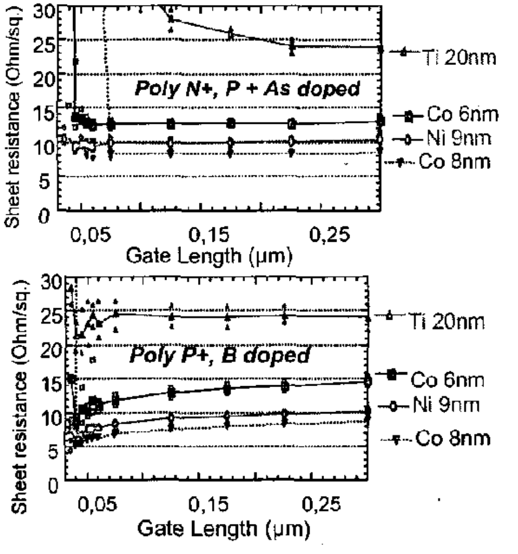


Figure 7: Poly N+ doped (top) and P+ doped (bottom)

$CoSi_2$: Actual attenuation at 1064 nm depends on real $CoSi_2$ thickness
~ inferred from TJ STEM
<u>Assumed to be 40 nm</u>

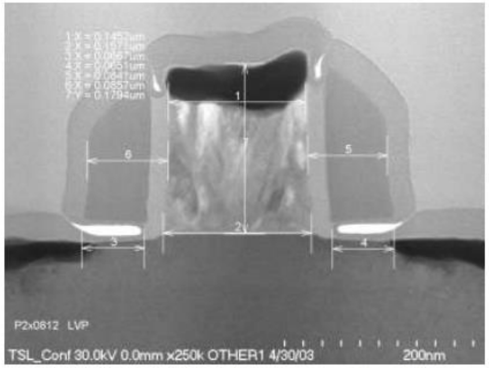
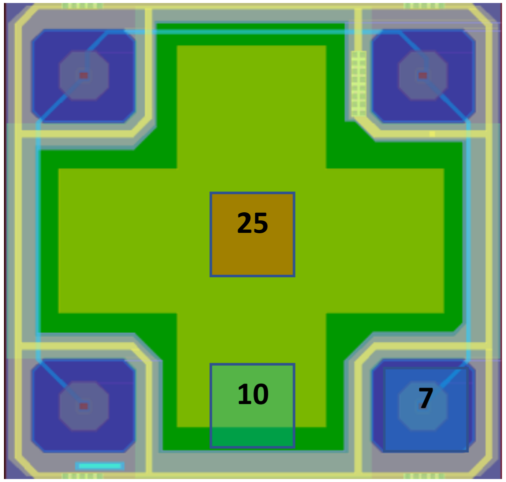


Figure 5.2-3 – STEM, LVP – L/W draw = 0.18/10 um

TCAD simulation

SiO_2: For normal incidence $R = \left|\frac{n_1 - n_2}{n_1 + n_2}\right|^2$

And transmitted: 1- R @ λ = 1064 nm, n_2=1.4469 R = 3.3%, T =96.6%, k = 0
Small attenuation through SiO_2, around 96.6 % of Light transmitted



Attenuation through SiO_2 only in NS regions (7) and through SiO_2-$CoSi_2$ in others (10,25)

TCAD simulation

Physics models: SDEVICE parameters for Optical generation

- OpticalGeneration (QuantumYield (StepFunction (EffectiveBandgap))
- ComplexRefractiveIndex (CarrierDep(Imag) WavelengthDep(Imag)) * extinction coeff. only
- OpticalSolver (OptBeam (LayerStackExtraction (WindowName = "LaserW“ Position = (0, Y_hit, Z_hit) Mode = ElementWise * Laser window of 5 x 5 um2, centre position retrieved from .gds, default NumberOfCellsPerLayer

- Wavelength= 1.064 * Incident light wavelength [um]
- Intensity= @<20000.0*exp(-0.036*@Silicide_Thick@)*0.966>@
- PolarizationAngle= 0 Theta= 90 Phi = 0

Manually estimated charge n ≈ (1-R)(1-exp(-αz_{max})P/hv=416 fC,
for z_{max}= 20 [um], R= 0.966 (SiO_2 attn. only, i.e. hit 7)

TCAD simulation

Physics models: SDEVICE parameters for mobility and recombination

- Temperature = 21°C
- Fermi
- Mobility(PhuMob Enormal (Lombardi PosInterfaceCharge)
- HighFieldSaturation(EParallel)
- RefDens_eEparallel_ElectricField_HFS= 1e17

- Auger
- SRH (DopingDep,TempDep, ElectricField (Lifetime = Hurkx)

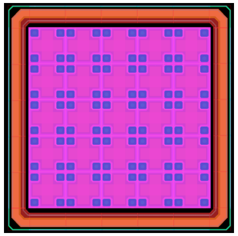
Math models

- ILS
- Geometricdistances
- e/hMobilityAveraging=ElementEdge

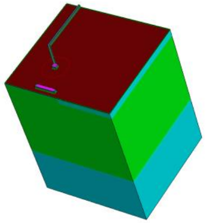
TCAD simulation

Simulations time

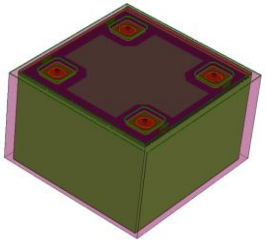
Layout editing

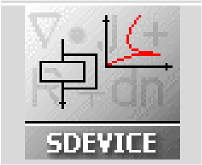


Process simulation ¼ pixel
~5500 secs

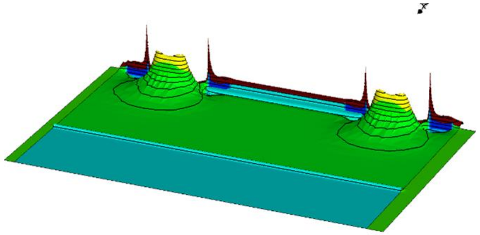


Process simulation – SDEVICE
~4000 secs



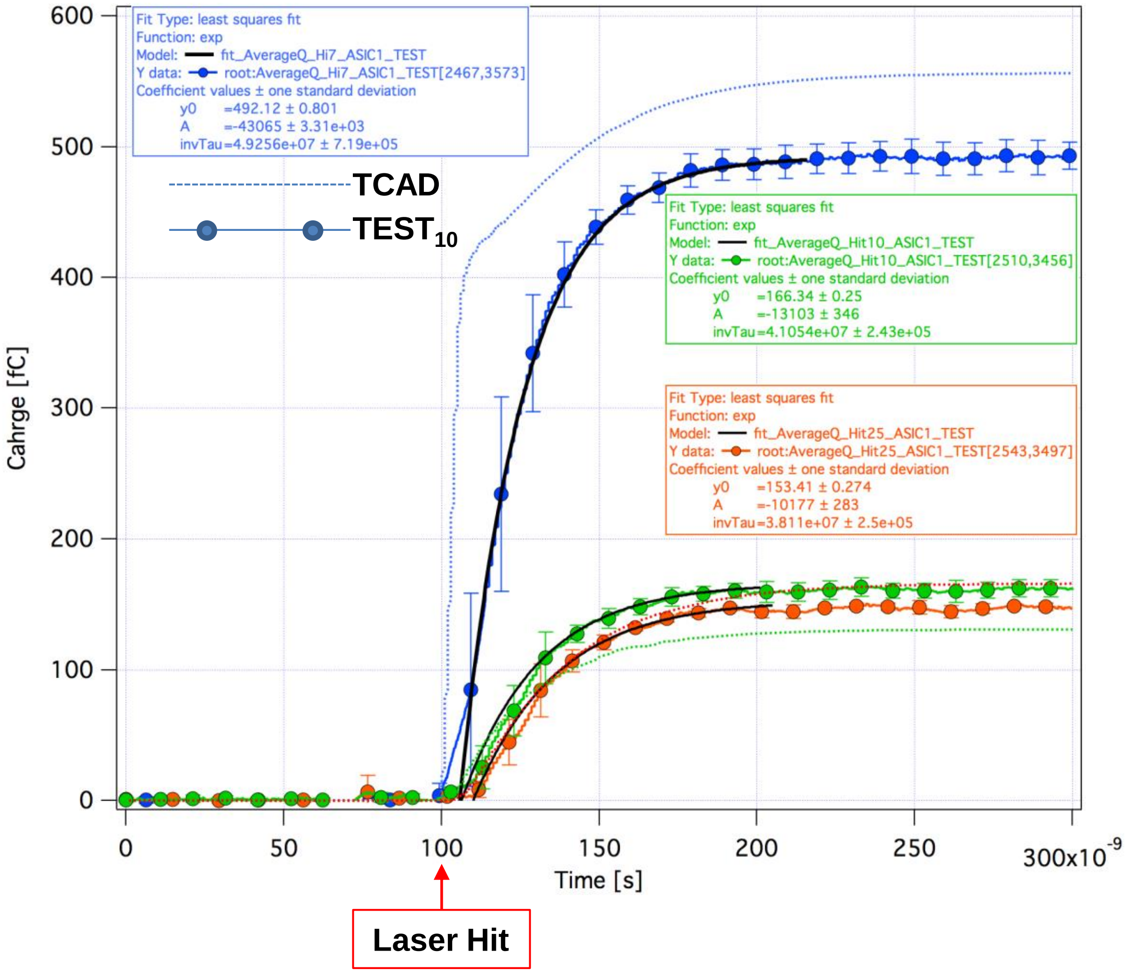


DC/CC simulation
>200k secs



Running on WS Intel Xeon Gold 5122 4 Core Processor, 3.6GHz, 16GB 2.4GHz RAM, 240GB SSD 6Gb/s

TCAD simulation

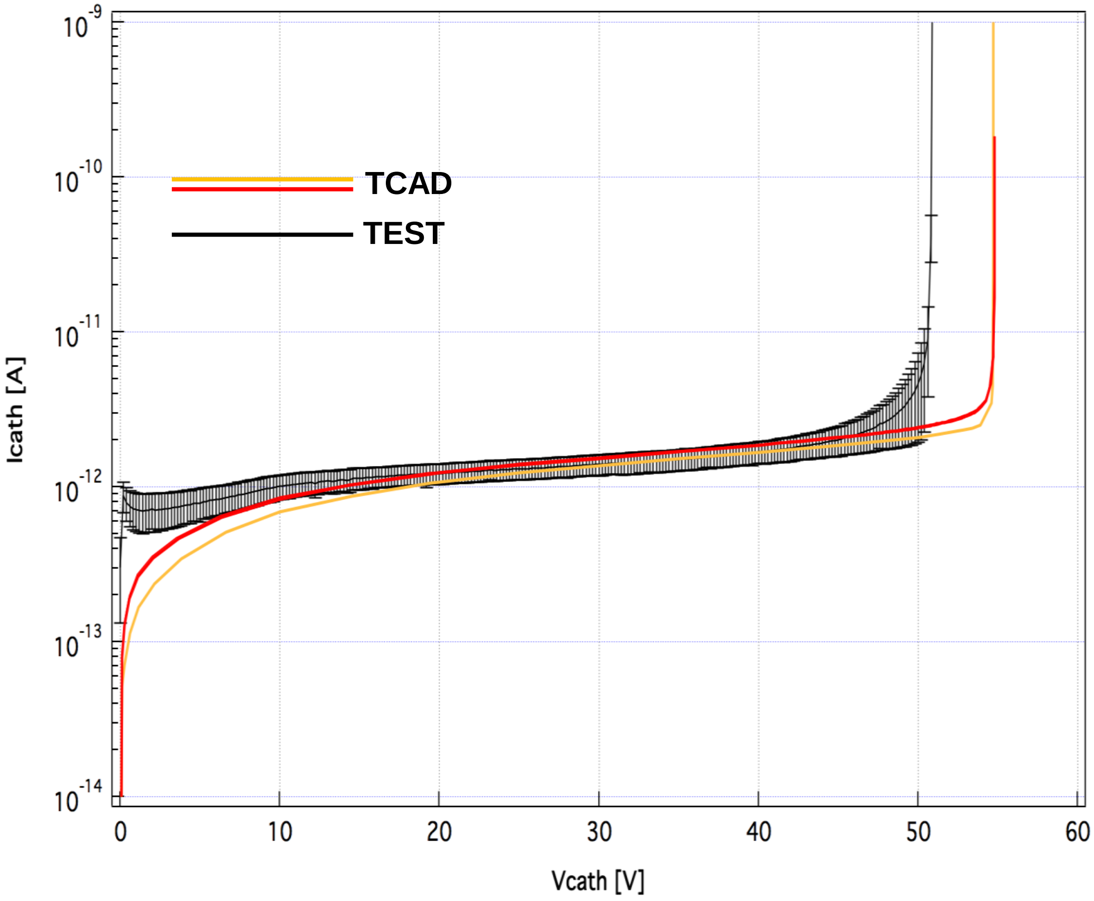


Q_{coll}	Test	TCAD	Δ%
<Qh7>	492	556	**13**
<Qh10>	166	131	**-21**
<Qh25>	153	166	**8.4**

$T_{coll10\text{-}90}$	Test	TCAD	Δ%
$\langle t_{coll}h7 \rangle$	44.6	45.2	**1.3[a]**
$\langle t_{coll}10 \rangle$	53.5	59.9	**12[b]**
$\langle t_{coll}25 \rangle$	57.6	68	**18[c]**

[a]hit7 with CA delay subs: 9.1%
[b]hit10 with CA delay subs: 17.7%
[c]hit25 with CA delay subs: 23.3%

TCAD simulation



DC IV plots up to BV, non irradiated devices.
<IV>[10] measured OVERMOS + σ
IV TCAD Oxch 1.1e11, OxINT 1e11
IV TCAD Oxch 1.2e11, OxINT 1.1e11

I_{leak}	Test	TCAD	Δ%
$<I>_{10V}$	1.01pA	0.85pA	**-14.5**
<BV>	51.66	54.79	**6.1**[a]

[a]BV defined as V: $(\Delta I/\Delta V)_{max}$

Conclusion

- Measured IV characteristics of OVERMOS up to Breakdown
- Measured CC characteristics of OVERMOS using laser injection
- TCAD 3D simulations using a simplified device obtained using SPROCESS. The SPROCESS scripts allow simulation of devices fabricated using TJ 180nm SL (diodes, MOSFETs)
- When properly set up, TCAD simulations seem to reproduce well experimental results, both in DC and in CC, with maximum discrepancy of the order of ~20%
- This completes the studies of non irradiated OVERMOS devices. Next step is the investigation and modelling of irradiated structures

THANK YOU

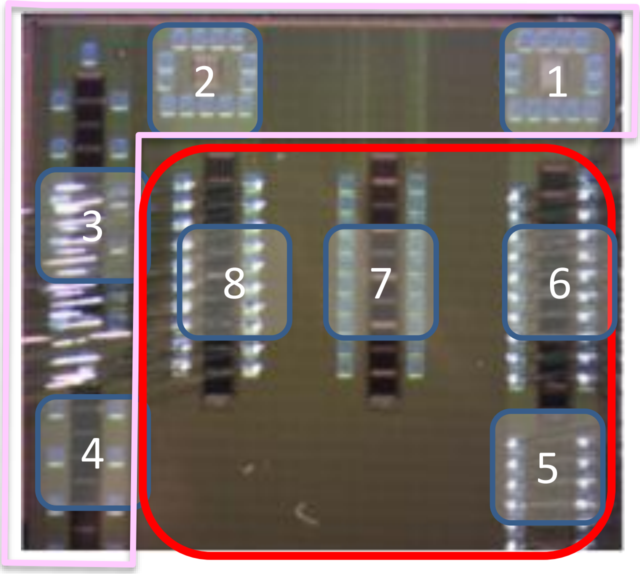
BACKUP

2: Basic Passive: 5x5 of 40 x 40 um

3: Basic Passive Large: 5x5 of 40 x 400 um merged

4: Basic Passive Large: 5x5 of 40 x 400 um

PASSIVE



1: Symmetric Passive: 5x5 of 40 x 40 um

8: Basic Active Large 5x5 of 40 x 400 um

7: Basic Active Large Merged 5x5 of 40 x 400 um

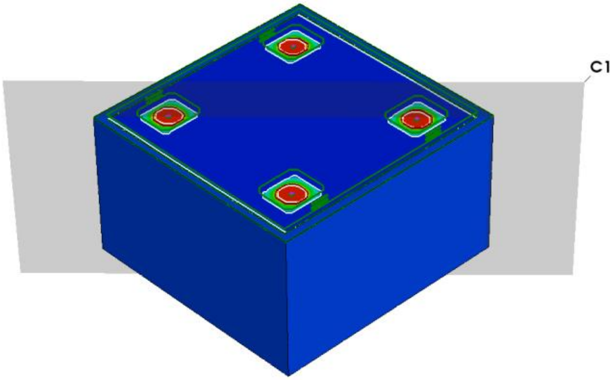
6: Basic Active AC Large 5x5 of 40 x 400 um independent diode biasing AC coupled

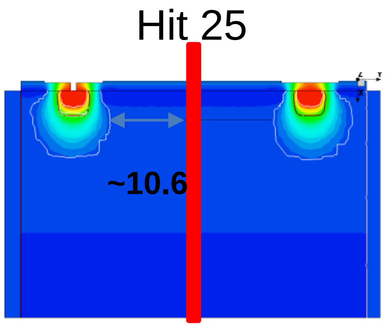
5: Basic Active: 5x5 of 40 x 40 um

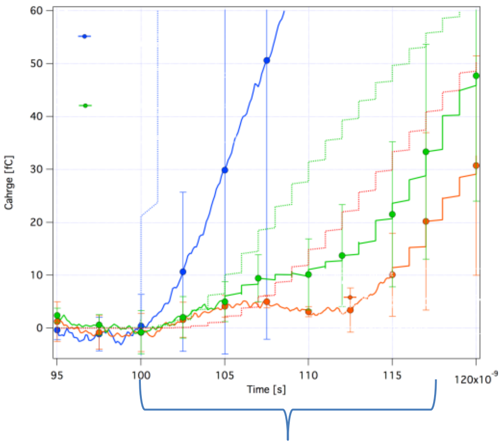
ACTIVE

- The PASSIVE pixels feature different arrangements of the collecting nodes, still of the same size (4 x 4 um2)
- The ACTIVE pixels, i.e. with in-pixel electronics, all allow analogue readout of the pixels

BACKUP







$\Delta t_{1\%}$~16.8 ns

- The maximum delay in signal output is from hit 7
- Assuming diffusion until the edge of DR, ~$z^2/(2D)$=16 ns for hit 25