

Status on TRAMOS (Trapping MOS) and DotPix (Quantum Dot Pixel) ongoing developments

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Charles Renard (C2N) and G. Hallais, Francois Jomard (GEMAC), Francois Olivié and coworkers (LAAS), the EMIR network (Jannus/Saclay)

The purpose of the DotPix project is to design a new kind of pixel for inner vertex detectors arrays with enhanced point-to-point resolution. It is based on a single MOS device, which may allow a resolution below the micron making track reconstruction and vertex determination with an unprecedented accuracy. It comprises a buried gate, which acts as a charge-collecting electrode with memory effect and controls the current of a micron-size n-channel MOS transistor. The design of such a pixel requires the massive use of device simulations. Future e+e- colliders (FCC,ILC) will benefit from this development.

I. Motivations for a new pixel design

II. How a buried gate can act as collecting electrode

III. How it can operate as a memory

IV. Designing and fabricating the buried gate

V. Simulation results

VI. Technological progress

VII. Summary and further work

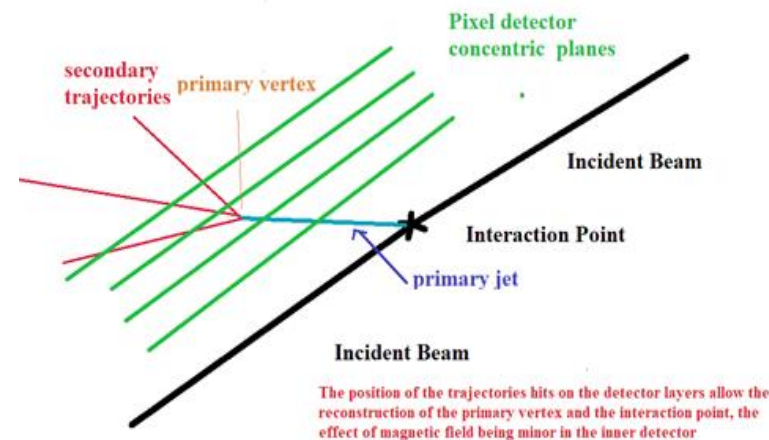
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I. Motivations for a new pixel design

- Future trackers and vertex detectors need accurate track reconstruction and precise vertex determination down to the micrometer
- This is a prerequisite for the $e+e-$ colliders in the future
- Fast response should be also sought for bunch identification, this means accessory detector
- High radiation hardness is still a challenge however less constraining with respect to hadron colliders
- This impose to reduce the area of each pixel , increase the number of pixel per unit area
- Low hit rate per pixel , in favor of reduced data flux by data compression , low multiple hit rate , limited single pixel area
- High p_T events ($-\infty < h < 0$) , $h = -\ln(\tan(\theta/2))$ pseudorapidity, where θ is the angle w.r.t. incident beam



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I. Motivations for a new pixel design

- **Classic and modified CMOS pixels, in many cases too slow, need depleted area to be fast (three transistors at least) NIEL tolerance bad in many case due to diffusion the solution has been DMAPS (with highly resistive substrates)**
- **CCD could be reduced in size but not random addressable.**
- **DEPFET is single device, but should be improved in terms of size**
- **We need a monolithic depleted device with low power consumption, with downscaling possible**
- **Pixel need local readout and memory and a depleted diode, this means many transistors and pixel size > 1 micron squared**
- **We propose to combine every function in a single device pixel : one device + memory in a CMOS compatible process , with a target of 100 nm feature line, and 10 micrometer in depletion layer thickness**
- **Up to now no submicron pixel for charged particle detection has been operating, sizes above 10 x 10 micrometers, this could improve by CMOS downscaling but still need many transistors.**

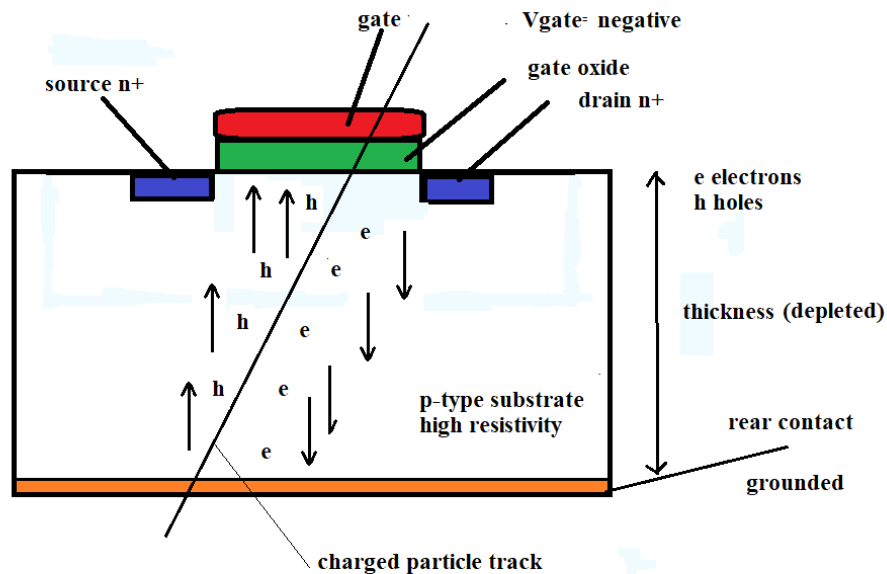
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II. How a buried gate can act as collecting electrode

- A charged particle make a track in the silicon bulk along the vertical or inclined
- We start from a MOS structure, which can be reduced to a MOS capacitor



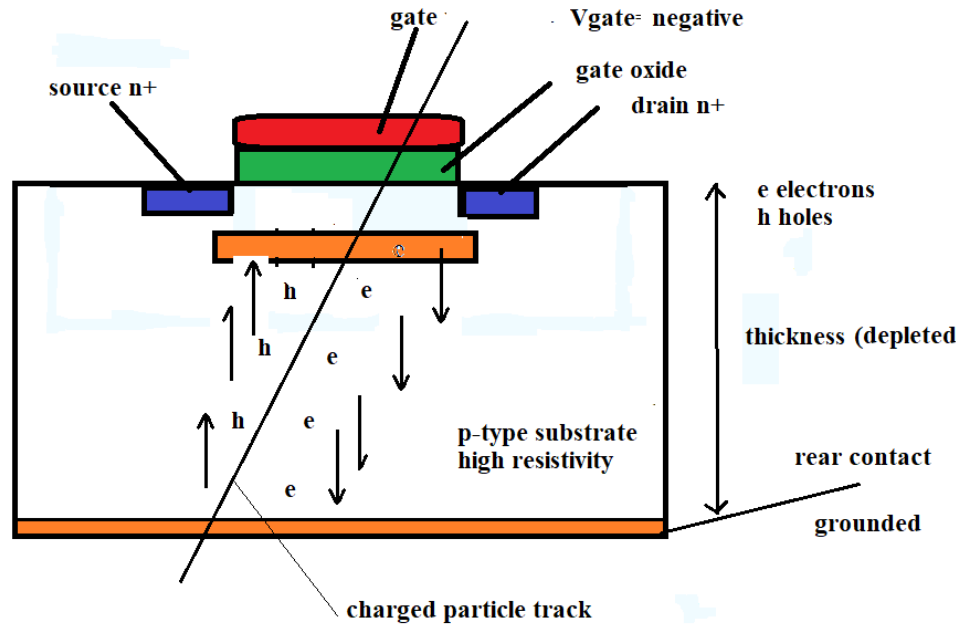
- The thickness of the depleted zone 5 μm to a few tens of μm : need for thinning or implanted zone
- With a negative bias on the gate the holes accumulate under the gate oxide and the electrons are evacuated into ground
- This operation is close to that of a CCD
- Source and drain may be floating during this operation phase
- There is no permanent leakage because of the insulated upper gate only a displacement current during charge migration which should be fast : $v_h = 10^7 \text{ cm s}^{-1}$ for thickness : $thickness = 10^{-3} \text{ cm}$, drift time is $\tau = 0.1 \text{ ns}$
- No use at this stage , but we can introduce a buried control gate.

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II. How a buried gate can act as collecting electrode



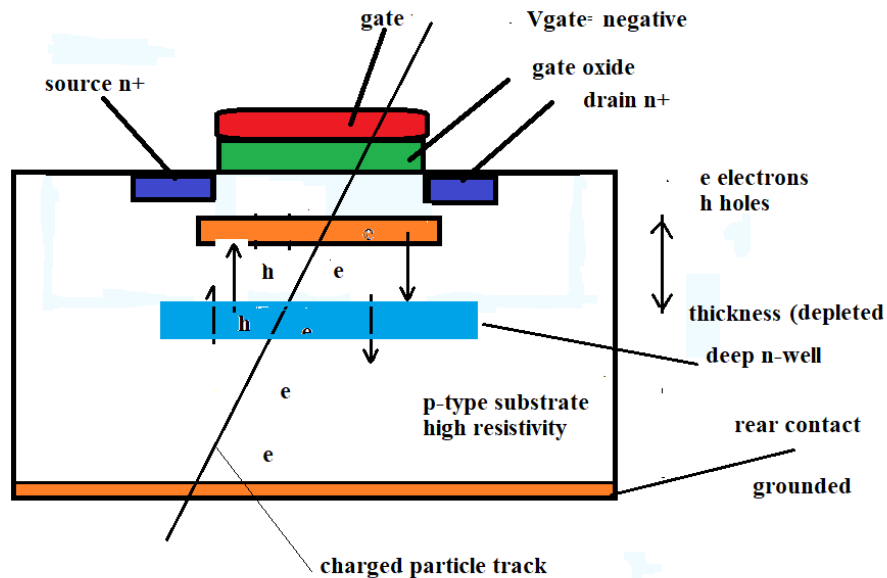
- A buried gate is introduced below the channel
- With a negative bias on the upper gate the holes accumulate in the buried gate, whereas the electrons are evacuated
- The buried gate should act as a potential well for the hole and not for the electrons
- The buried gate should also retain the holes during a long enough time
- The same holds for the collection time and the permanent leakage current
- Source and drain may be floating during this operation phase

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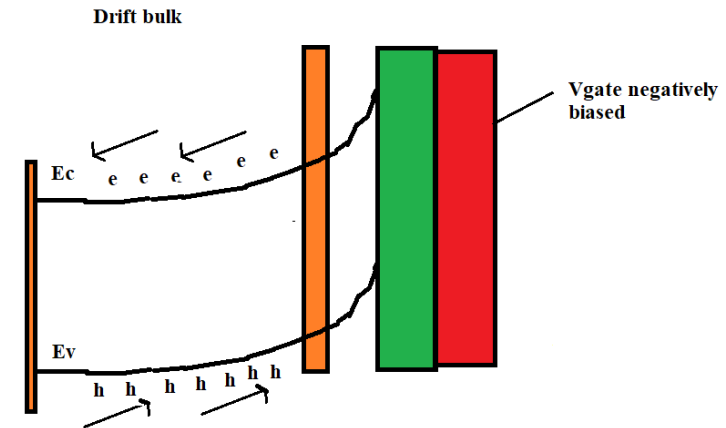
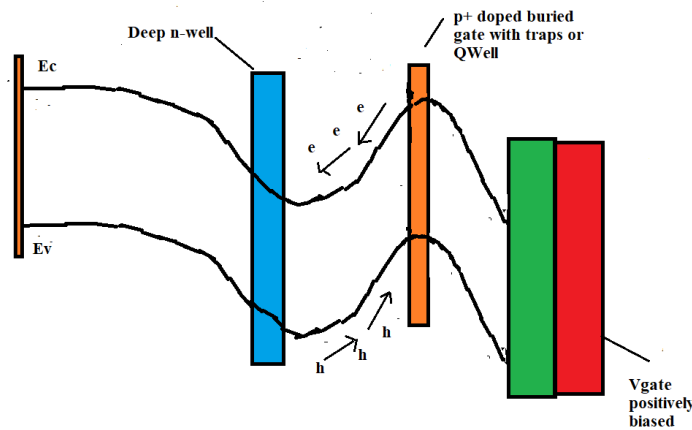
- **Alternative design with a deep-n-well used for electron/hole separation**
- **The MOS structure can be operated with a slightly positive bias on the upper gate**
- **The buried gate is made of a high density of holes traps**
- **A deep impurity can be used for creating the trap zone**
- **The thickness in which the useful electron-hole pairs are created is limited (1micrometer) , transition region of the buried gate/ deep n-well region**
- **Source and drain can be bias during this phase**
- **This is the first version of the TRAMOS (2010)**

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II. How a buried gate can act as collecting electrode



1. The zone between the deep-n-well and the buried gate enable the drift of holes towards the buried gate

2. In the absence of deep n-well the holes drift towards the buried gate. This impose that the upper gate should be negatively biased. High resistivity p-type substrate.

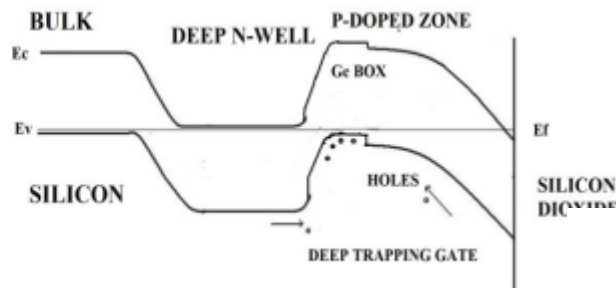
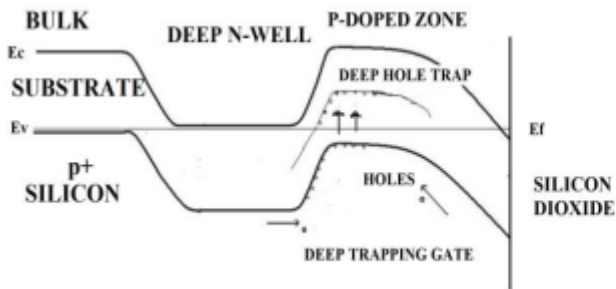
3. We could use the version 2 with a p-channel MOSFET operating permanently with a negative upper gate bias

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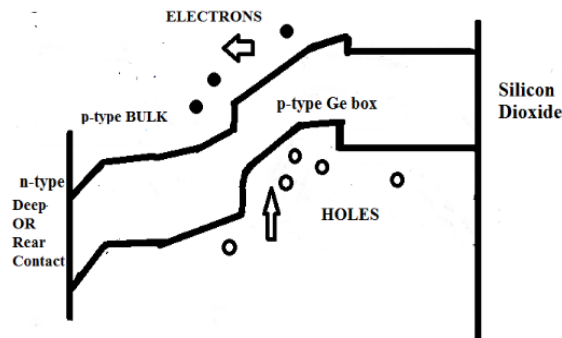
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II. How a buried gate can act as collecting electrode



**TRAMOS + Deep n-well
Use Traps**

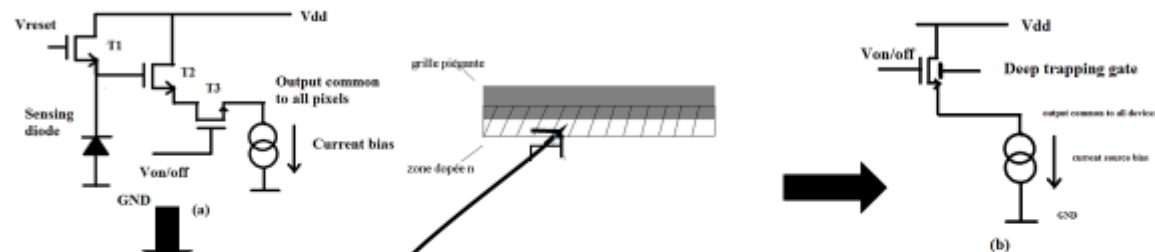
**DOTPIX + Deep n-well
Use VB quantum well**



Upper Gate = negative bias, detection mode

- FET with internal gate : the DEPFET (1987) by MPI Munich

- The CMOS : MAPS by IPHC Strasbourg
- First proposed the TRAMOS (2010)
- Then the Dotpix (2016)



From (a) to (b) the collecting electrode becomes a gate buried under the amplifying device.



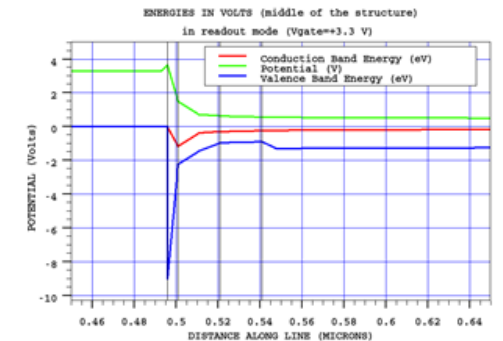
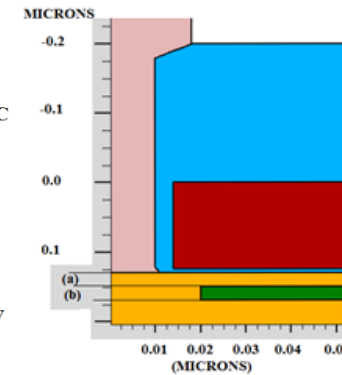
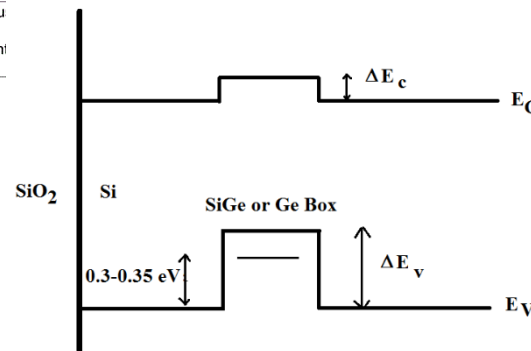
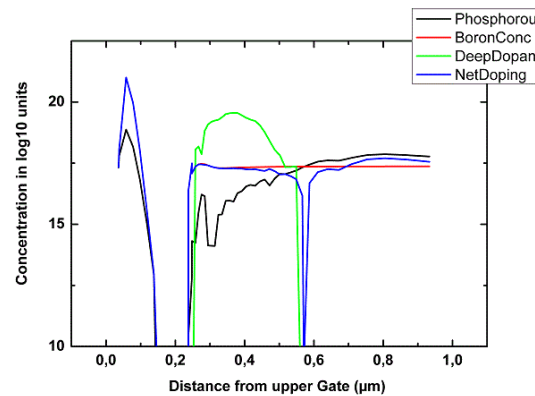
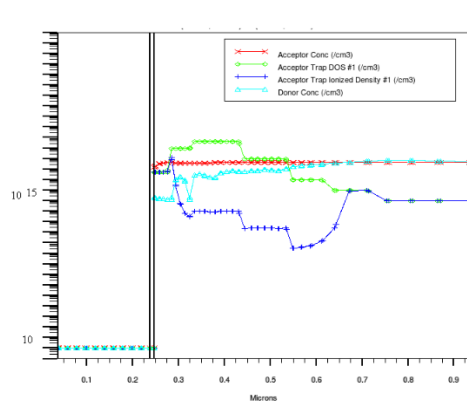
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III. How it can operate as a memory

- We need a buried gate that act as a control gate for the channel current with the ability to retain its hole charge sufficiently long to enable readout. This means the device should act as a memory.
- 1) First use a shallow doped p-type buried with a high concentration of deep impurities (such as Zn) which selectively trap hole and not electrons. Substitutional Zn is double hole trap. Problem how to get a high peak substitutional Zn concentration with no contamination ? Implant +RTP.
- 2) Second use a Quantum Well for holes, not for electrons.
- In the first solution the thermal emission rate for holes trapped on impurity sites determines the **retention time** for holes.
- In the second solution, hole emission to the VB of silicon and other mechanism set the **retention time**.
- In any case **device simulation** is the way to evaluate the functionality of the proposed devices as a way to make a **proof of principle**.



- Impurity profile in the TRAMOS

- Structure of the DotPix (a)=10-20 nm (b)=20 nm

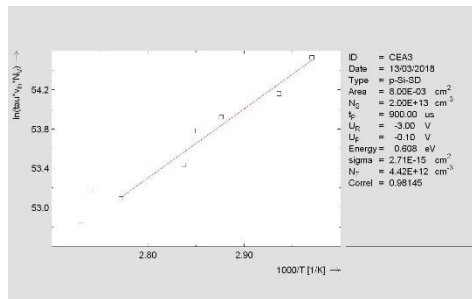
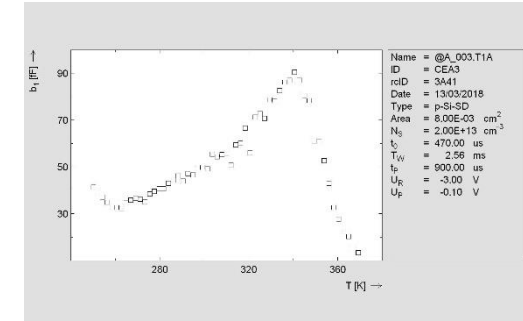
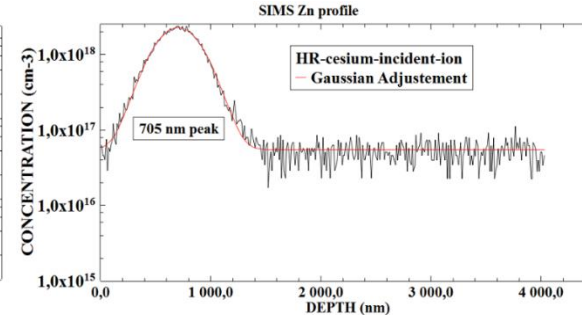
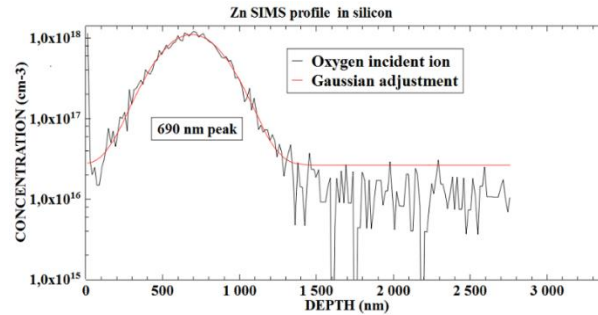
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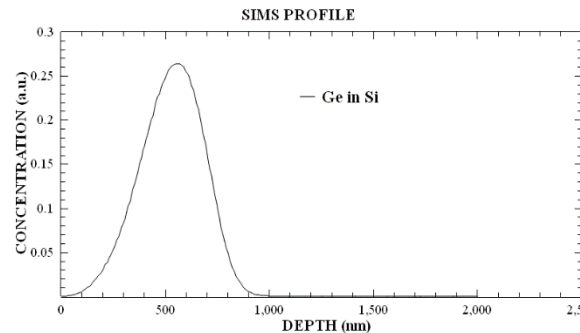
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IV. Designing and fabricating the buried gate

- Zn can be implanted in the bulk silicon during the process of the n-channel MOS transistor
- High energy ion implantation can be used but beware of contamination (1MeV energy)
- But disappointing DLTS results , concentration do not match >> Fermi level pinning
- Substitutional Zn acts as a deep double hole trap
- Needs stabilizing the buried layer (annealing)
- Needs a sharper profile



Very preliminary !!!
Credit F. Olivie

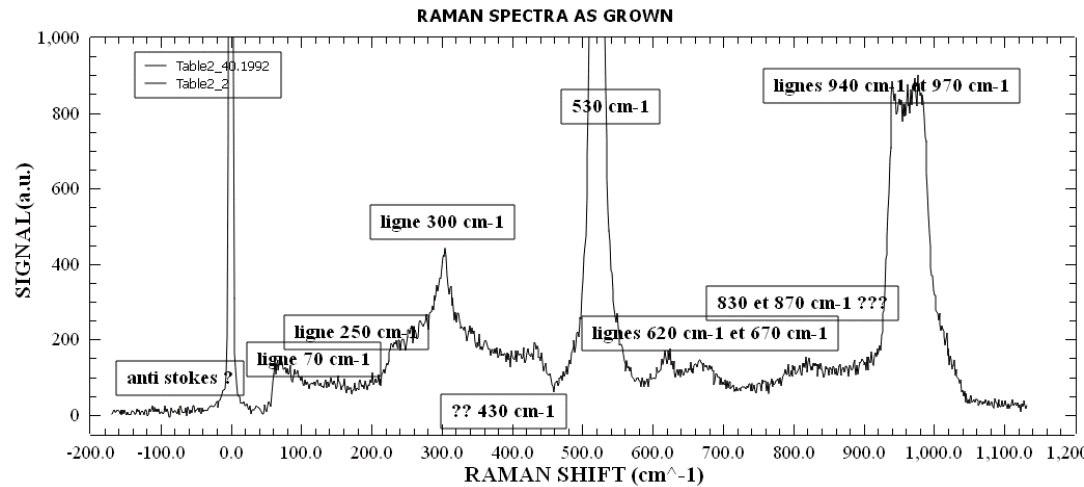
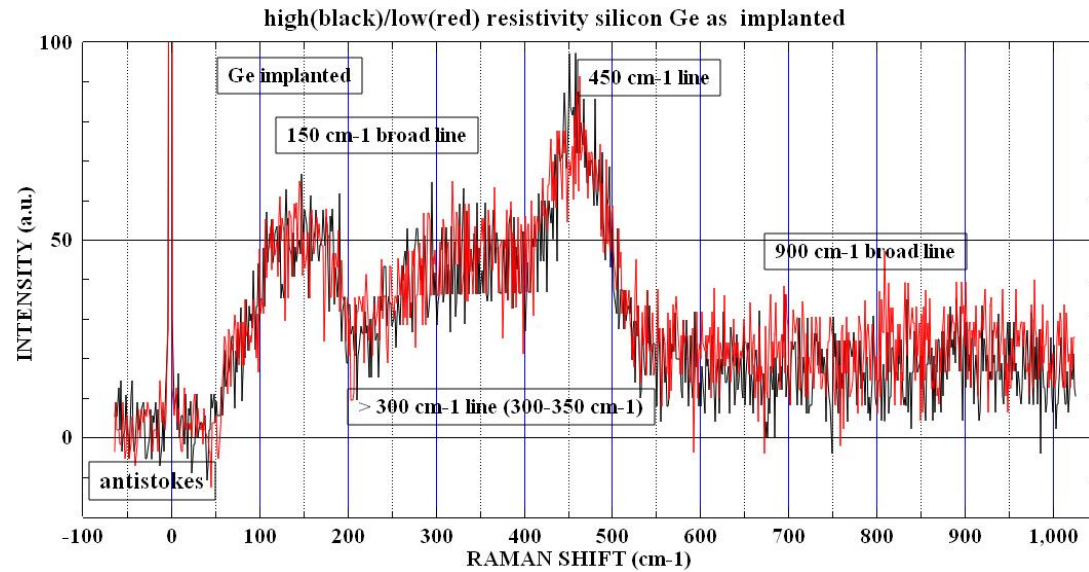
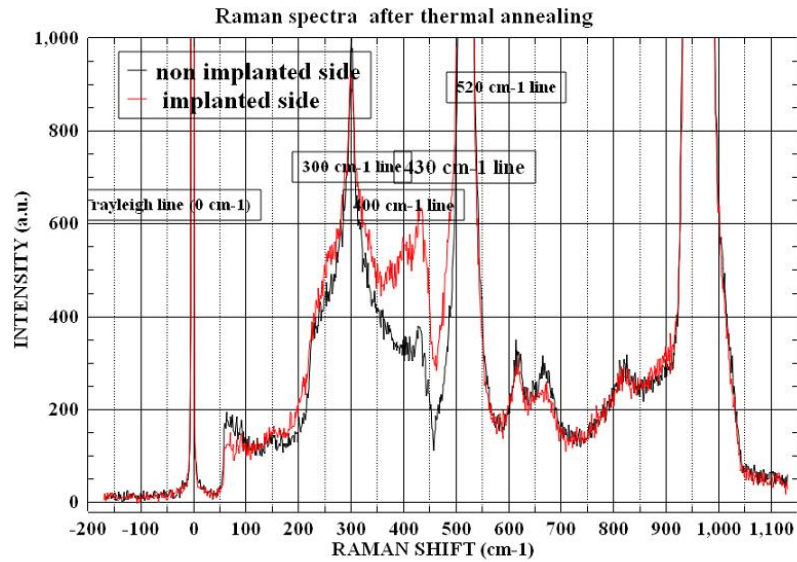


- Ge has been implanted at 1MeV with high doses, the maximum concentration obtained in the samples is 25% with a lot of scatter (down to 6%) , the concentration profile is not sharp but in accord with SRIM simulations
- No thermal anneal, was performed after implantation
- High dose implantations are take to much time !!!
- Could be used however
- This is for high resistivity silicon, similar results are obtained on low resistivity silicon

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- SRIM simulation (Stopping Range Of Ions in Matter, Ziegler et al.), simulation code V.2008 and with Kinchin and Pease displacements calculation method
- The defect concentration is high in the region close to the surface : more displacements than the atomic density (d.p.a > 1)
- Ge ions density : $2 \times 10^{17} \times 20000 = 4 \times 10^{21} \text{ cm}^{-3}$, more than 10% of the silicon atomic density

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Density gradient approximation (Quantum Moments Model) : transport properties for quantum level simulations Density Gradient (Quantum Moments Model) ;

See:

Andreas Wettstein, Andreas Schenk, and Wolfgang Fichtner, Fellow, IEEE, 'Quantum Device-Simulation with the Density-Gradient Model on Unstructured Grids', IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 48, NO. 2, FEBRUARY 2001, 279 and references herein:

Transport equation from reference above
$$\vec{j} = qD_n \nabla n - \mu_n n \nabla (\phi + \Omega) + f(n)$$

With Ω is a quantum correction potential which is a function of n and \hbar and the carrier effective mass and $f(n)$ a vector function of the electron density

What we must take into consideration by TCAD :

- Quantum channel confinement simulation
- Thin gate oxide MOS capacitors and transistors
- Small geometry heterojunction diodes (QW are this case)
- Confinement of carriers / electron wave functions extension
- This model is based on the moments of the Wigner function equations-of motion (perturbation approximation, in a way semi-classical) which consists of quantum correction to an hydrodynamic model
- No need to determine stationary solution to Schrödinger equation as with Poisson-Schrödinger method, hence better for transient behavior.
- Both holes and electrons are considered in the transport process : very important with the DotPix !!!
- Purely classical simulations were made showing that quantum simulations introduce only limited corrections

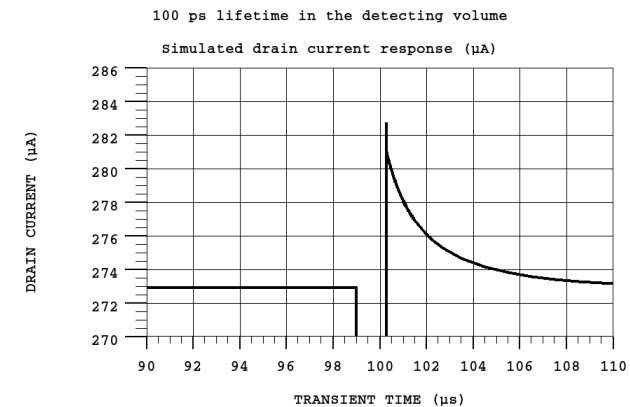
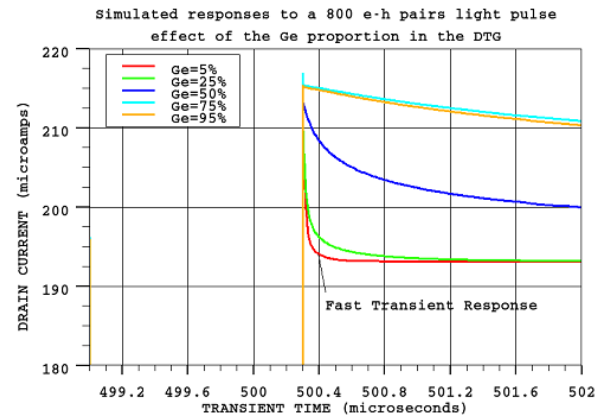
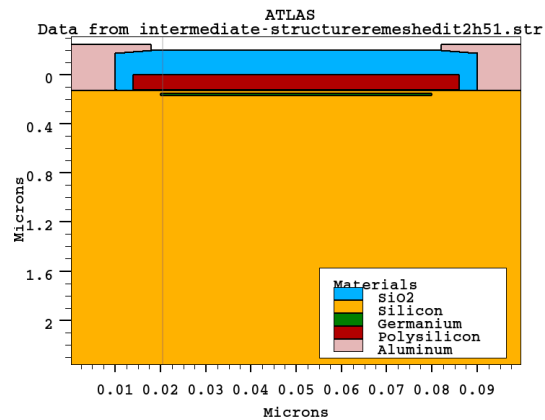
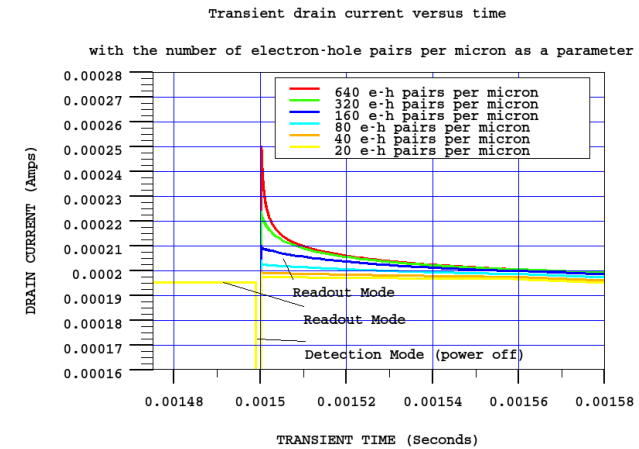
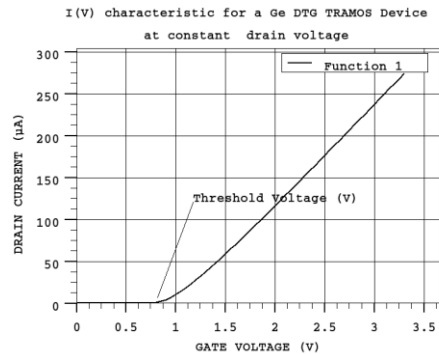
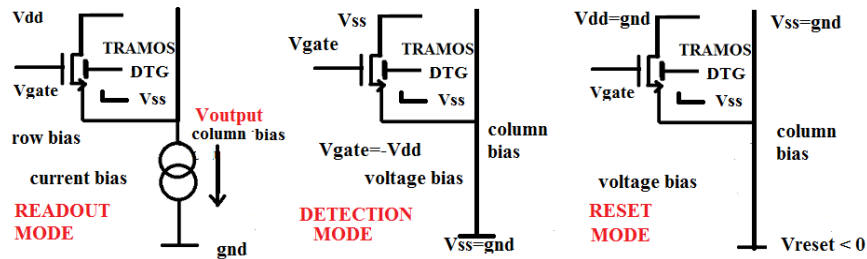
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V. Simulation results

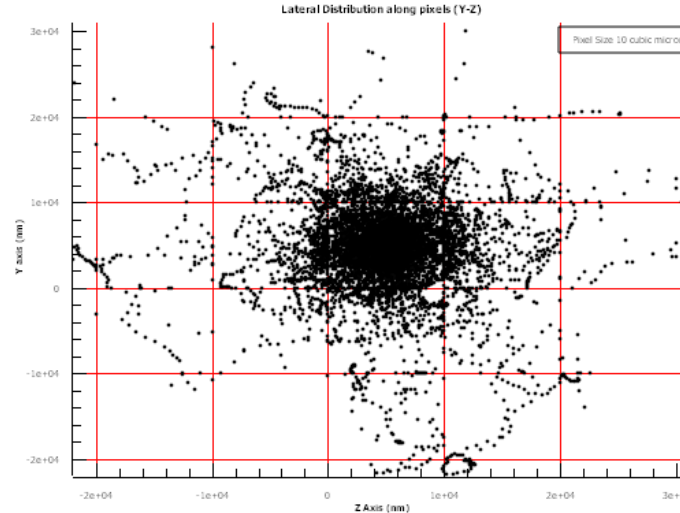
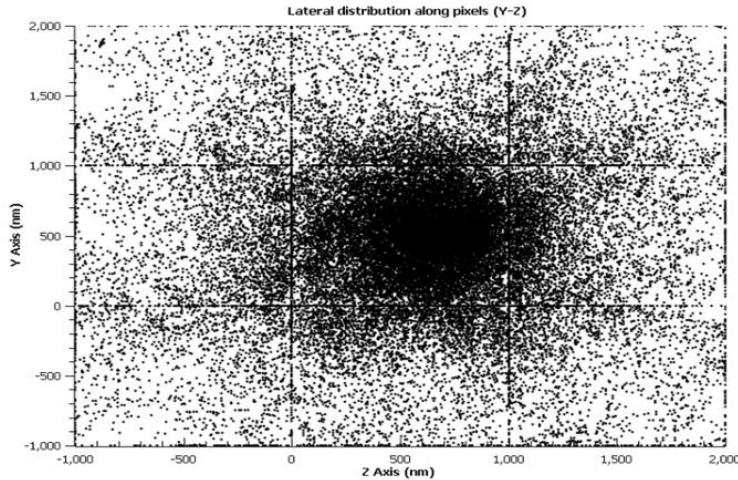
Focus on the Quantum Well design (results have been published) Germanium layer in the first figure, the thickness of the structure is set to 10 nm in the simulation file. Quantum density gradient simulations



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V. Simulation results



Pixel Size (μm^2) Thickness (μm)	E_{avg} (keV)	E_{MPV} (keV)	Ratio avg (%) (E_N/E_p) [*]	Efficiency ($E_{\text{Th}}=500\text{eV}$)
1 * 1 * 10	3.28	2.17	4.74	99.3
1 * 1 * 20	6.76	4.89	4.9	99.82
1 * 1 * 30	10.86	7.84	-	>99
1 * 1 * 40	14.36	9.68	-	>99
1 * 1 * 50	17.98	13.21	-	>99
10 * 10 * 10	3.26	2.15	0.994 1	99.9
10 * 10 * 50	16.68	13.17	2.08	>99
10 * 10 * 100	34.76	24.3	2.35	>99

**GEANT4 on a $1\mu\text{m} \times 1\mu\text{m} \times 10\mu\text{m}$ structure,
 Scattered Hits on the Silicon Layer : 130 GeV
 pions (credit to V. Kumar, Saclay, 2016 , M2
 report)**

**The same on Pixel Size $10\mu\text{m} * 10\mu\text{m}$,
 Thickness $10\mu\text{m}$:**

Wafer Thinning is necessary , detection efficiency remains good enough for thicknesses of 10 micrometers

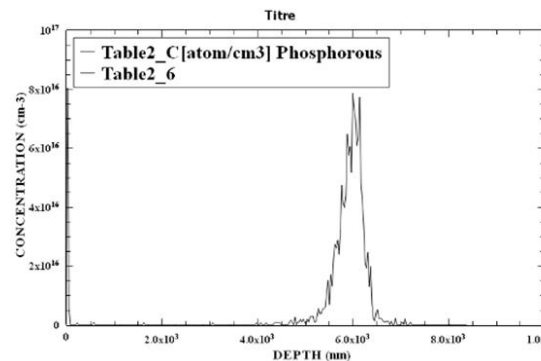
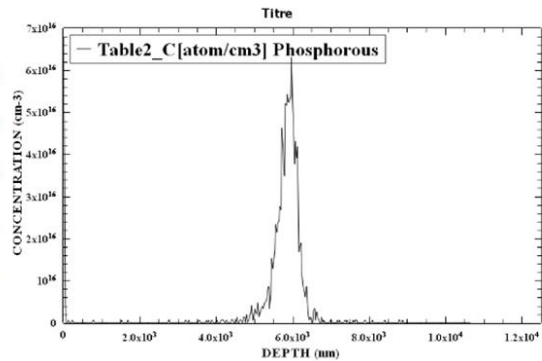
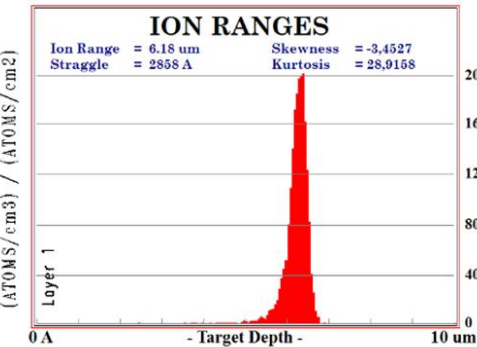
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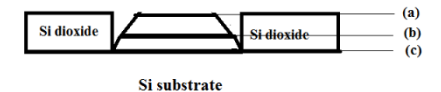
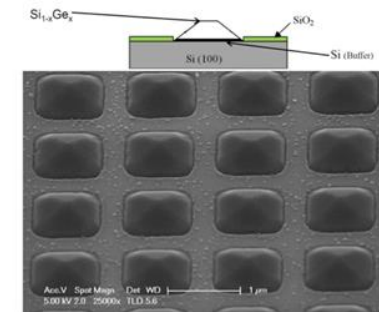
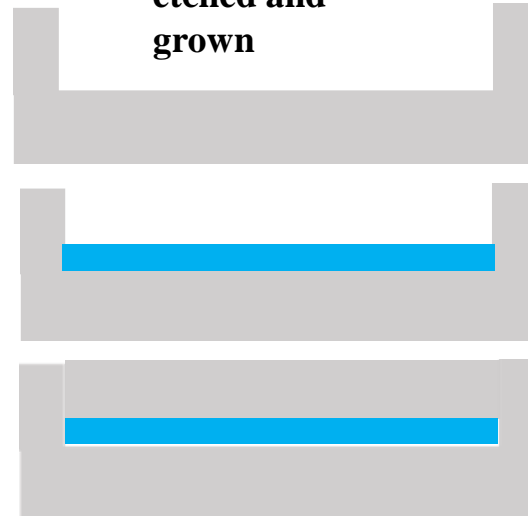
VI. Technological progress

SRIM (Stopping and Range of Ions In Matter) simulations and SIMS (Secondary Ion Mass Spectroscopy, GEMAC equipment) for Phosphorous implanted at high energy (14 MeV in silicon) for Deep-well, at 5 μm below the surface, no need for high doses.



- Alternative to ion-implantation
- UHV/CVD of SiGe on a silicon substrate grown on the whole wafer surface
- Si/ grey and Ge/blue
- Pseudomorphic layer (4%, lattice mismatch between Ge and Si)
- Ge lattice constant : 0.565 nm and Si : 0.5431 nm
- Normally Ge/Si compressively strained
- Ge >> 20 nm metastable or relaxed
- C2N equipment

Selectively etched and grown



(a)-(b) : Ge (% ?) épaisseur ??
(b)-(c) : Si buffer layer épaisseur ??

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VII. Summary and further work

- Device simulations have been extended to the case of p-channel device and are encouraging
- Characterisation of Si/Ge/Si epi layers are under way. These were made at C2N by Charles Renard and coworkers
- Work is under way to make a MOS process with reduced thermal budget, to limit inter diffusion
- Participating institutes are welcome, and people too, for simulation, modelling , characterisation and technology
- The project is open, some collaboration with DEPFET or CMOS researchers would be particularly appreciated
- ILC and FCC would benefit from this R&D , joint R&D ?
- Work with facilities or laboratories with material characterisation competences is sought: ion implantation, SIMS, RBS, electrical measurements such DLTS, epitaxial growth and CMOS processing , this would contribute to accelerate the developments along with irradiation facilities

Contributions from : Charles Renard (C2N) and G. Hallais, Francois Jomard (GEMAC), Francois Olivie and coworkers (LAAS), the EMIR network (Jannus/Saclay) with G.Gutierrez

**Jannus: Joint Accelerators for Nano and Nuclear Science); C2N Centre de Nano Science et de Nanotechnologies
Laboratoire d'Analyse et d'Architecture des Systèmes; GEMAC (Groupe d'Etude de la Matière Condensée)**

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• Work published up to now:

- N. Fourches, Y. Degerli, M. Besançon, A. Besson, G. Claus, G. Deptuch, W. Dulinski, M. Goffe, A. Himmi, Y. Li, P. Lutz, F. Orsini, M. Szelezniak.. (2005, October). “Performance of a fast programmable active pixel sensor chip designed for charged particle detection”. In *IEEE Nuclear Science Symposium Conference Record, 2005* (Vol. 1, pp. 93-97). IEEE. <http://dx.doi.org/10.1109/NSSMIC.2005.1596214>
- N.T. Fourches, “Device simulation of Monolithic Active Pixel Sensors: Radiation damage effects”, *Nuclear Science Symposium Record* , Pages 2523-2529 , *IEEE Transactions On Nuclear Science*, Vol. 56, No.6, December 2009, Pages 3743-3751, <http://doi.org/10.1109/TNS.2009.2031540>
- Nicolas T. Fourches, “Ultimate Pixel Based on a Single Transistor With Deep Trapping Gate”, *IEEE Transactions On Electron Devices*”, Volume 64, Issue 4, (2017) 1619-1623 <http://doi.org/10.1109/TED.2017.2670681>
- N. Fourches, E. Orsier , J du Port de Pontcharra, R. Truche , “Design and test of elementary digital circuits based on monolithic SOI JFETs”, *IEEE Transactions on Nuclear Science* Vol 45 N° 1 February 1998, <http://dx.doi.org/10.1109/23.659553>
- Nicolas T. Fourches, “A novel CMOS detector based on a deep trapping gate”, *Nuclear Science Symposium Conference Record (NSS/MIC, 2010)*, p 655-658, 2010, Knoxville, Tennessee: <http://dx.doi.org/10.1109/NSSMIC.2010.5873840>, Nicolas Fourches, "Semiconductor device ", U.S. Patent No. 7,936,018. 3 May 2011
- Vishant Kumar, Master II, Thesis, Ecole des Mines de Nantes, defended September 2016, available on request at IRFU
- N. T. Fourches, & W. Vervisch, (2016). “Simulations of a silicon pixel based on MOS Deep Trapping Gate Principle, arXiv preprint arXiv: 1602.00263. <http://arxiv.org/abs/1602.00263>

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EXTRA SLIDES

$$e\vec{j} = -\mu k_B T \nabla n - \mu n \nabla(\Phi + \Lambda)$$

$$\Lambda = \frac{\hbar^2 \beta}{12m} \left[\nabla^2 \Phi - \frac{\beta}{2} (\nabla \Phi)^2 \right]$$

$$e\vec{j} = -\mu k_B T \nabla n - \mu n \nabla \Phi - \mu \left(\nabla \frac{\hbar^2 n}{4mk_B T} \cdot \nabla \right) \nabla \Phi_q, \quad (1)$$

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Status on TRAMOS (Trapping MOS) and DotPix (Quantum Dot Pixel) ongoing developments

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EXTRA SLIDES

Pixel Size 10 μm * 10 μm , Thickness 10 μm :

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The Electrical Properties of Zinc in Silicon

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Abstract. Electrically active deep levels related to zinc in silicon are investigated in n- and p-type silicon using Deep-Level Transient Fourier Spectroscopy (DLTFS) measurements.

While in n-type silicon a level at $E_c - 0.49$ eV is observed, the main zinc-related levels in p-type silicon are determined to be $E_v + 0.27$ eV and $E_v + 0.60$ eV. The latter are associated with zinc situated on regular silicon lattice sites. The emission rate of these centers exhibits a field dependence which cannot be quantitatively explained with the Poole-Frenkel model.

On the other hand, a shallow level at $E_v + 0.09$ eV is observed only in boron-doped silicon which may be related to a zinc-boron complex. Other zinc-related levels are found at $E_v + 0.23$ eV and $E_v + 0.33$ eV, their concentration depending on that of zinc on substitutional sites. In addition, the evaluation of depth profiles and the analysis of the field dependence of the emission rate based on the DLTFS method is presented

