Contribution ID: **4**   Type: **not specified**

Status on TRAMOS (Trapping MOS) and DotPix (QuantumDot Pixel) ongoing developments

Tuesday 27 November 2018 14:30 (20 minutes)

Abstract: The DotPix project is the result of several attempts to design a new kind of pixel for inner vertex detectors arrays with enhanced point-to-point resolution. As experiments include the DEPleted FET (DEPFET) based detector or monolithic pixels, it is now important to design a pixel based on a single device, which can reach a resolution below the micron with reduced thicknesses allowing track reconstruction and vertex determination with unprecedented accuracy. This is necessary for the future e+e- colliders (FCC,ILC).The proposed pixel structure, based on MOS technology will be described with its different possible implementations. It comprises a buried gate, which acts as a charge-collecting electrode with memory effect and controls the current of a micron-size n-channel MOS transistor. The device may be downscaled. The design of an architecture compatible with a process flow close to standard CMOS has required the massive use of device simulations. We have identified the bottlenecks and we will describe the way we can overcome them in a near future.
Short Bibliography:

Nicolas T. Fourches, IEEE Transactions On Electron Devices, Volume 64, Issue 4, (2017) 1619-1623. http://doi.org/10.1109/TED.2017.267068
France

Primary author: Dr FOURCHES, Nicolas (IRFU/DEDIP/DePhyS CEA Saclay)

Presenter: Dr FOURCHES, Nicolas (IRFU/DEDIP/DePhyS CEA Saclay)

Session Classification: Device Simulation