Overview of design and evaluation of depleted CMOS sensors within RD50

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**RD50-MPW1 – Overview**

**General details**
- MPW in the 150 nm HV-CMOS process from LFoundry
- To test the technology aspects of this process and novel designs
- Submitted in November 2017, received in April 2018
- Fabricated on wafers with 2 different substrate resistivities
  - $500 \, \Omega \cdot \text{cm} \ (40 \, \text{samples})$ and $1.9 \, \text{k} \, \Omega \cdot \text{cm} \ (80 \, \text{samples})$

**MPW contents**
1) Tests structures for e-TCT and sensor capacitance measurements
2) Matrix of depleted CMOS pixels with 16-bit counter
   - $26 \times 52 \, \text{pixels}$
   - $75 \, \mu\text{m} \times 75 \, \mu\text{m} \, \text{pixel area}$
3) Matrix of depleted CMOS pixels with FE-I3 style readout
   - $40 \times 78 \, \text{pixels}$
   - $50 \, \mu\text{m} \times 50 \, \mu\text{m} \, \text{pixel area}$
   - Analog and digital readout embedded in the sensing area
   - Completely independent matrices
   - Careful design with LF15A V1.2.0, the first design kit to include
     - Models to simulate the sensing diodes
     - Proper verification
- Pixel size is 50 μm x 50 μm
- No readout electronics
- I-V of **central pixel** of test structure for e-TCT
- Measurement done using a probe station with sensor in complete darkness
- $V_{BD}$~55-60 V as expected from design, but $I_{LEAK}$ is too high
- Doing TCAD simulations and getting support from the foundry to understand this problem
- The sensors are fully functional *(see presentation by I. Mandic in this RD50 WS)*
2 sets of DAQs

- 1 developed by IFAE (available from a previous design), for more details see presentation by S. Terzo in TWEPP 2018
- 1 developed by IFIC/HEPHY (developed within the CERN-RD50 collaboration, in progress)
- For more details about the IFIC/HEPHY DAQ, see presentation by R. Marco-Hernandez in 32nd RD50 WS
Fairly good agreement between measured and simulated results

Larger mismatch in those DACs that carry smaller currents (probe with 1M Ω input resistance takes current away and modifies the measurement)

Measurements done with IFAE DAQ

With IFAE DAQ, $I_{\text{LEAK}}$ of matrix is also large at very small voltages ($I_{\text{LEAK}} = 25$ mA @ HV = 2 V)
Aims

- Replicate the breakdown voltage and leakage current measured with RD50-MPW1
- Understand what is causing the large leakage current

**We are doing TCAD simulations to**

- Study the effect of increasing the spacing between PWELL (cathode @ HV) and NWELL (anode)
  - Simulation of a range of PWELL/NWELL spacings
  - Effect on the electric field
- Study the effect of pixel corners (90 degrees, 45 degrees and rounded) on electric field strength
- Study the effect of chip guard ring configuration on breakdown voltage and leakage current
Simulation of a range of PWELL/NWELL spacings

- Increasing the spacing between the PWELL (cathode @ HV) and NWELL (anode @ $V_{DN}$)
  - Magnitude of electric field decreases
  - Breakdown voltage increases as expected
- We also think there is some lateral diffusion
TCAD simulations

3D simulation of electric field at pixel corners

- **Left**: Top-down and front views of the electric field of a pixel with square corners
- **Right**: Simulation area (~ 1/4 of the pixel) chosen to minimize simulation time (> 1 week)
- Red lines are junction interfaces; white lines are depletion region limits

\[ V_{DN} = 1.8 \, V \]
\[ HV = -70 \, V \]
TCAD simulations

3D simulation of electric field at pixel corners

- **Left:** Top-down view of the electric field of a pixel with square corners
  - Pink dashed lines represent cut lines for front-views
- **Right:** Front-views of non-corner and square corner slices of the pixel
  - High electric field at square corners, which generates premature breakdown voltage
3D simulation of electric field at pixel corners

- **Left**: Pixel with **square corners**
- **Right**: Pixel with **rounded corners**
  - Running simulation of electric field of a pixel with rounded corners at the moment
  - Colour of the simulations represents the doping concentration
Simulation of guard rings

- **Top**: Chip edge of RD50-MPW1 contains a large bias ring
- **Bottom**: Chip edge of a future RD50-MPW2 with a possible improved guard ring
  - Guard rings typically stop the pixel depletion region from coming into contact with the chip edge
- Colour of the simulations represents the doping concentration
Simulation of guard rings with edge defects

- Edge defects introduced during dicing
- **Noschis model** (4 trapping levels): edge defects form a depletion region that can contribute to the leakage current
- **Top**: Simulation of guard rings with edge defects at -50 V
  - Pixel/edge depletion regions do not merge
- **Centre**: Simulation of guard rings with edge defects at -70 V
  - Pixel and edge depletion regions merge
  - Pixel depletion region touches the edge of the chip and can increase the leakage current
- **Bottom**: Same simulation as in centre, but plotting the electron current density instead of the doping concentration
  - NWring ‘collects’ leakage current when the pixel/edge depletion regions merge
Comparison of TCAD simulated values with measured leakage current

- In RD50-MPW1, we have:
  1) Pixels with PWELL (cathode @ HV) and NWELL (anode @ $V_{DN}$) spacing of 3 μm
  2) Pixels with 90 degrees corners
  3) A large PWELL bias ring around the sensors instead of multiple NWELL and PWELL guard rings, as typically done in planar silicon sensors

- 1), 2) and 3) contribute to the leakage current, but do not explain the large measured values

- The foundry is aware of this situation. We are getting support from them.

- We suspect the biggest contribution to the large leakage current comes from filling layers added during the post-processing stage

- The filling layers generate conductive paths with a significant electron current density that contributes to the sensor leakage current. We are running TCAD simulations to fully understand this problem.

- The filling layers can be prevented at the design stage with blocking layers

Need to submit a test MPW

- We think it is too risky to submit the planned, large and expensive RD50-ENGRUN1 as our next step

- We think it is a lot safer to submit a small and cheap test MPW (RD50-MPW2) before submitting RD50-ENGRUN1

- TCAD simulations and chip design for RD50-MPW2 are quite advanced
Pricing condition:

a) MPW pricing condition
   - Charged area: 6 mm$^2$ (minimum area)
   - Price: 900 €/mm$^2$

b) Pricing for 2 customer specific substrates
   - 1000 € (80 dies in total)

TOTAL PRICE for a) and b) is 6,400 € (before VAT)
Pricing condition:

a) MPW pricing condition
   - Charged area: 9.31 mm²
   - Price: 900 €/mm²

b) Pricing for 2 customer specific substrates
   - 1000 € (80 dies in total)

TOTAL PRICE for a) and b) is 9,400 € (before VAT)

We are looking for funding.
If institutes are interested in participating, please contact me asap.
We need to book the area with the foundry before Christmas.
**MPW contents**

1. Tests structures for e-TCT
2. Matrix of depleted CMOS pixels with analog readout
   - 15 x 15 pixels
   - 60 μm x 60 μm pixel area
   - 2 different flavours of fast pixels
3. Matrix of depleted CMOS pixels with FE-I3 style readout
   - Same as 2), but with digital readout
   - Analog and digital readout embedded in the sensing area
   - Completely independent matrices
   - For more details about the pixels, see presentation by C. Zhang in 32nd RD50 WS

**Motivation**

- Fabricate each step of the detector separately (sensors, analog readout and digital readout) to measure and study each part independently.
Aims

- Improve the current time resolution of depleted CMOS sensors by a factor 10 with dedicated RO circuits
- Implement new sensor cross-sections
- Study pre-stitching options to increase the device area beyond the reticle size limitation
- Improve the current radiation tolerance with careful sensor design and backside processing

**All the work we are doing with RD50-MPW2 is a preparation for submitting RD50-ENGRUN1**
The design of the sampling pixel is quite advanced
The design of a new control unit is also progressing well
We can achieve timing resolutions of around 2 ns (simulated)
For more details about the sampling matrix, see presentation by O. Alonso in LCWS2018
We have started a project to develop depleted CMOS sensors within CERN-RD50

We have designed and fabricated a first test MPW (RD50-MPW1):
- RD50-MPW1 is under test at the moment
- I-V measurements show a $V_{BD}$ around 55-60 V as expected from design, but $I_{LEAK}$ is too high
- We are doing TCAD simulations to understand this problem and study how we can improve the design of the sensor

We stress the need to submit a small and cheap test MPW (RD50-MPW2) before submitting the planned, large and expensive RD50-ENGRUN1:
- Design and TCAD simulations for RD50-MPW2 are quite advanced
- RD50-MPW2 will contain passive diodes and 1 or 2 small matrices with analog or analog and digital readout electronics
- Before submitting RD50-MPW2, we need to find the funding to cover the prototyping costs

The design of the large RD50-ENGRUN1 is running in parallel

Thank you for your attention!