

Irradiation study of CMOS pixel detector structures on RD50-MPW1 chips from LFoundry

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RD50 submitted a pixel detector prototype ASIC in the 150 nm CMOS technology at LFoundry. It contains two matrices of MAPS pixels and few test structures. The test structures include passive pixel arrays near the edge of the chip suitable for E-TCT measurements. The chips were manufactured on p-type silicon with two different initial resistivities around 500 Ohm-cm and 2000 Ohm-cm. Chips were irradiated with neutrons in Ljubljana up to maximal fluence of 2×10^{15} n/cm². Edge-TCT measurements were made with passive devices and evolution of effective space charge concentration on neutron fluence was measured for the two different initial resistivities. Results of this study will be presented in this contribution.

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