

Options and constraints for passive sensor fabrication at CMOS foundries

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Motivation

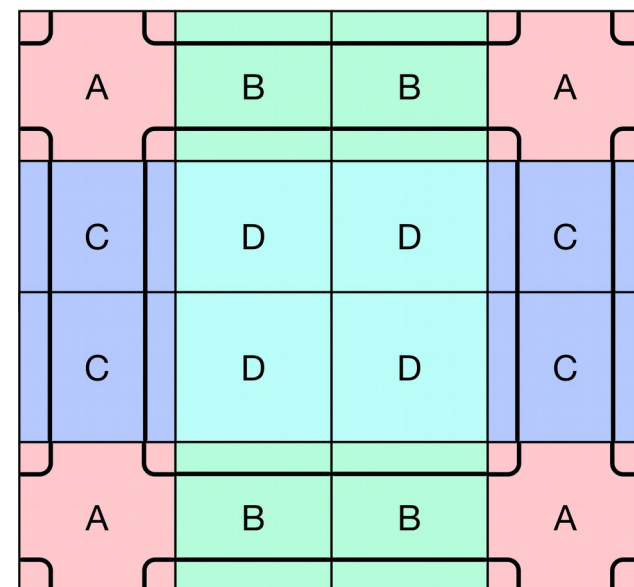
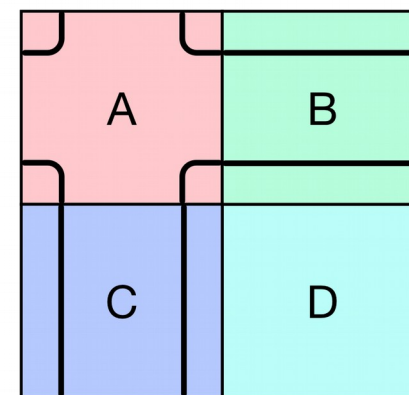
- Radiation-hard silicon sensors are used in larger and larger areas
 - Full tracker replacements for HL-LHC, FCC trackers...
 - Calorimetry – see e.g. HGAL and as high-granularity direct sensors
 - Timing detectors (e.g. HGTD)
- ▶ cost-efficiency of increasing importance
 - visible in efforts to establish production on 8” wafers

- Why produce something in CMOS fabs?
 - Large throughput (typical fab capacity: some 10.000 wafers/month)
 - typical detector size: Pixel – o(1.000) wafers, Strips – o(10.000) wafers
 - Established and **very** thorough QA/QC protocols
 - Usage of 8” or even 12” wafers
 - Has the potential to be significantly (a factor) cheaper than established sensor vendors for large volumes
 - large wafers
 - very few mask steps compared to a standard CMOS process
 - “huge” feature sizes, i.e. cheap/coarse masks and visible light lithography possible

Drawbacks/challenges

- Reticule-based lithography
 - typical reticule sizes are ~20mm by 20mm (some larger)
 - if you really need a larger sensor, you need to compose it, i.e. “stitch”
 - not all fabs offer stitching – actually probably very few (examples: TowerJazz, LFoundry)
 - classically: large pixel matrix (D), edges (B, C), corners (A)
 - however, apparently equal size sub-reticules are preferred for alignment precision
 - the more/the smaller sub-reticules you have, the more “shots” the stepper will need – the longer the lithography will take and the more costly it will get
 - ideally (cost-wise) create a detector from single-chip modules
 - will always fit on a reticule
 - makes (module) testing easier
 - more items to handle, but identical type and comparatively small size might enable the use of industrial pick+place machines

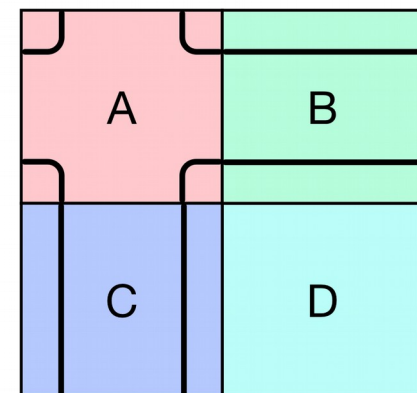
Reticule



on wafer

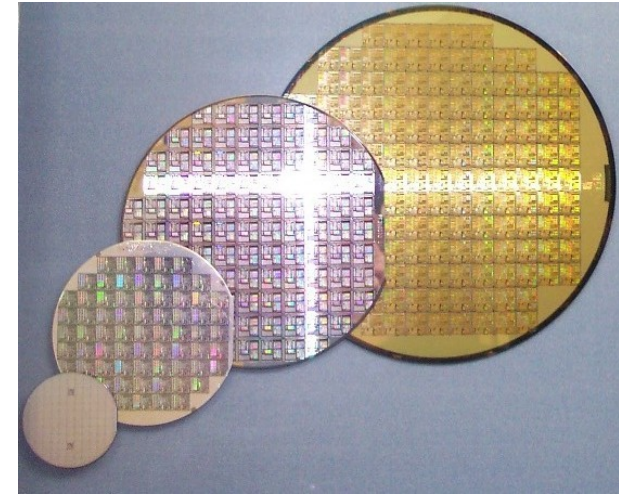
Drawbacks/challenges

- More reticule-based issues
 - usually, reticules cannot be rotated – sometimes wafers can, but maybe just by 180 degrees
 - usual “matrix reticules” (A) only contain identical pixels - what about “special” pixels, e.g. long/ganged pixels?
 - have more than one mask set
 - have more than one metal mask
 - use UBM metal (full-size contact mask!) to connect pixels
 - fabs are used to placing their own test/monitoring structures into the dicing streets, i.e. at the edge of the reticule
 - doesn't work like this for stitched sensors, be sure to discuss options with foundry
 - your own test structures have to fit in B, C or D – much less options than for a “usual” contact-lithography wafer, where one has ample space around the main sensor tiles



Drawbacks/Challenges

- Substrates
 - Default is (M)Cz wafers, mostly p-type, with 10-20 Ohm*cm for HV-CMOS – too low for passive sensors
 - In CIS (CMOS Imaging Sensors) processes, often higher resistive substrates are offered – or epi/SOI
 - Usually too low for passive sensors anyway, and epi not useful – high-resistive (kOhm*cm) substrates are necessary
 - Some fabs unwilling to produce on high-resistive substrates
 - Procurement usually done by the fab – wafer suppliers seem to be a highly regarded trade secret
 - define requirements, fab will look for suitable wafers
 - high-res default seems to be MCz, but there are some afterthoughts in RD50 about p-type MCz...
 - 8” FZ wafers exist and can be procured (lead time o(10 weeks)) – large quantities would have to be clarified in advance
 - while thinning down to 50µm is standard and “for free”, backside implant and metallisation are not
 - post-processing? special process step?

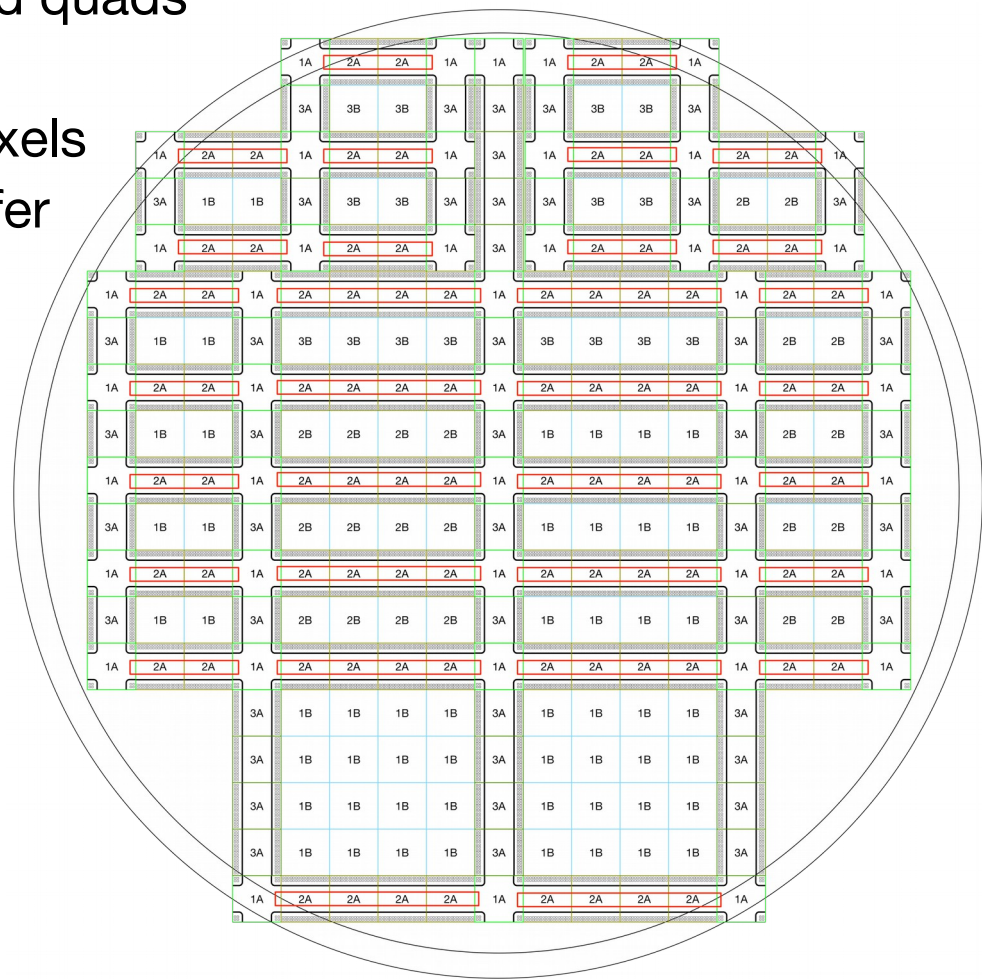


Advantages/Features

- Turnaround times: typically 3 months after submission
 - might be slower if processes are heavily modified or very customer-specific
 - the more standard you can go, the faster
- QA/QC
 - CMOS plants are probably the best controlled/supervised/QCed production sites anywhere
 - ideal if underlying process is intended for automotive/aerospace (i.e. not consumer)
 - stay as close to standard process as possible
- Wafer size
 - 8" or 12"
- Substrate thickness
 - thinning down to 50 μ m standard and without charge (caveat backside!)
- Features: MIM capacitors (AC coupled pixels), MOhm resistors
- Price for large volumes
 - Classical 8" CMOS wafers with are few 1000 EUR/wafer, with reduced number of processing steps o(several 100 EUR) could be reachable
 - With stitching probably a bit more expensive, but still much cheaper per area than classical sensor vendors producing on 4" and 6" wafers

Ongoing activities

- Several monolithic CMOS sensor productions on high-resistive substrates with various foundries ongoing
- Beyond that, ATLAS and CMS are pursuing a joint submission to assess the feasibility of passive planar pixel sensor production on 8" wafers at a CMOS foundry
 - RD53A compatible singles, doubles and quads
 - DC and AC coupling
 - 50 μm by 50 μm and 25 μm by 100 μm pixels
 - will also have stitched strips on the wafer
- Timeline: submission hopefully in December, wafers back in early April
- Once we know if/how well (yield) that worked, we should probably follow up also within RD50...



Next RD50 workshop at Lancaster University

Some organisational points

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Next RD50 workshop

- During the last CB, it was decided to have the spring RD50 workshop 2019 at Lancaster University, United Kingdom
- Some facts about Lancaster University:
 - has been a founding member of RD50 and has re-acquired full member status in 2015
 - is among the Top-10 universities in the UK
 - is a campus university
 - founded in 1964
 - > 15.000 students



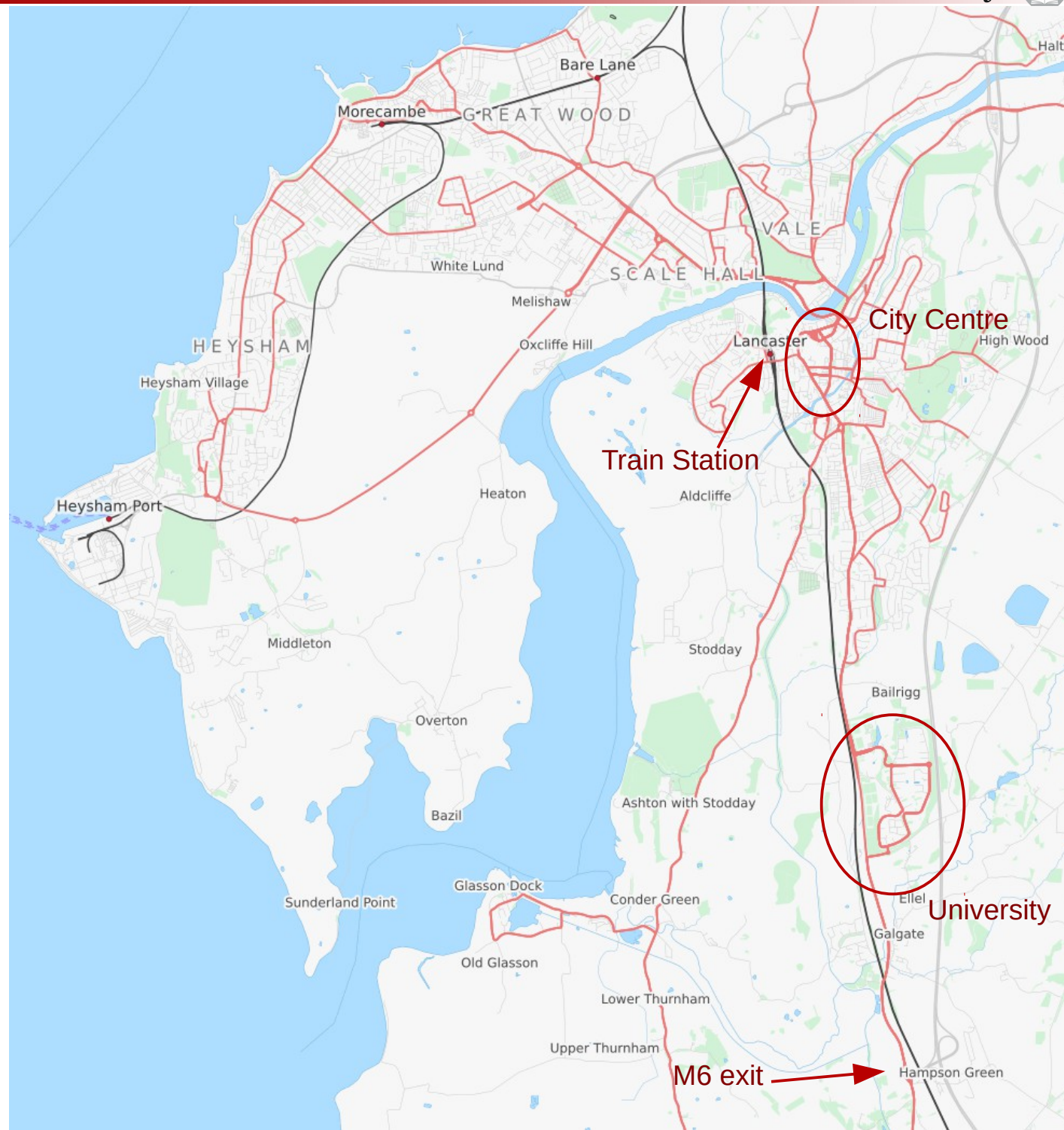
Getting to Lancaster

- North of Manchester/Liverpool
- Airport access to
 - Manchester (direct train connection from the airport, about 1 hour)
 - Liverpool
 - Glasgow (2 hours by train)
 - Edinburgh (2 hours by train)
 - Birmingham (2 hours by train, direct train connection from the airport)
 - (London – 2.5 hours by train, but you need to get from the airport to London Euston station first...)
- For groups of participants, we can organise airport transfers from/to Manchester and Liverpool at reasonable cost (~60 GBP per car)



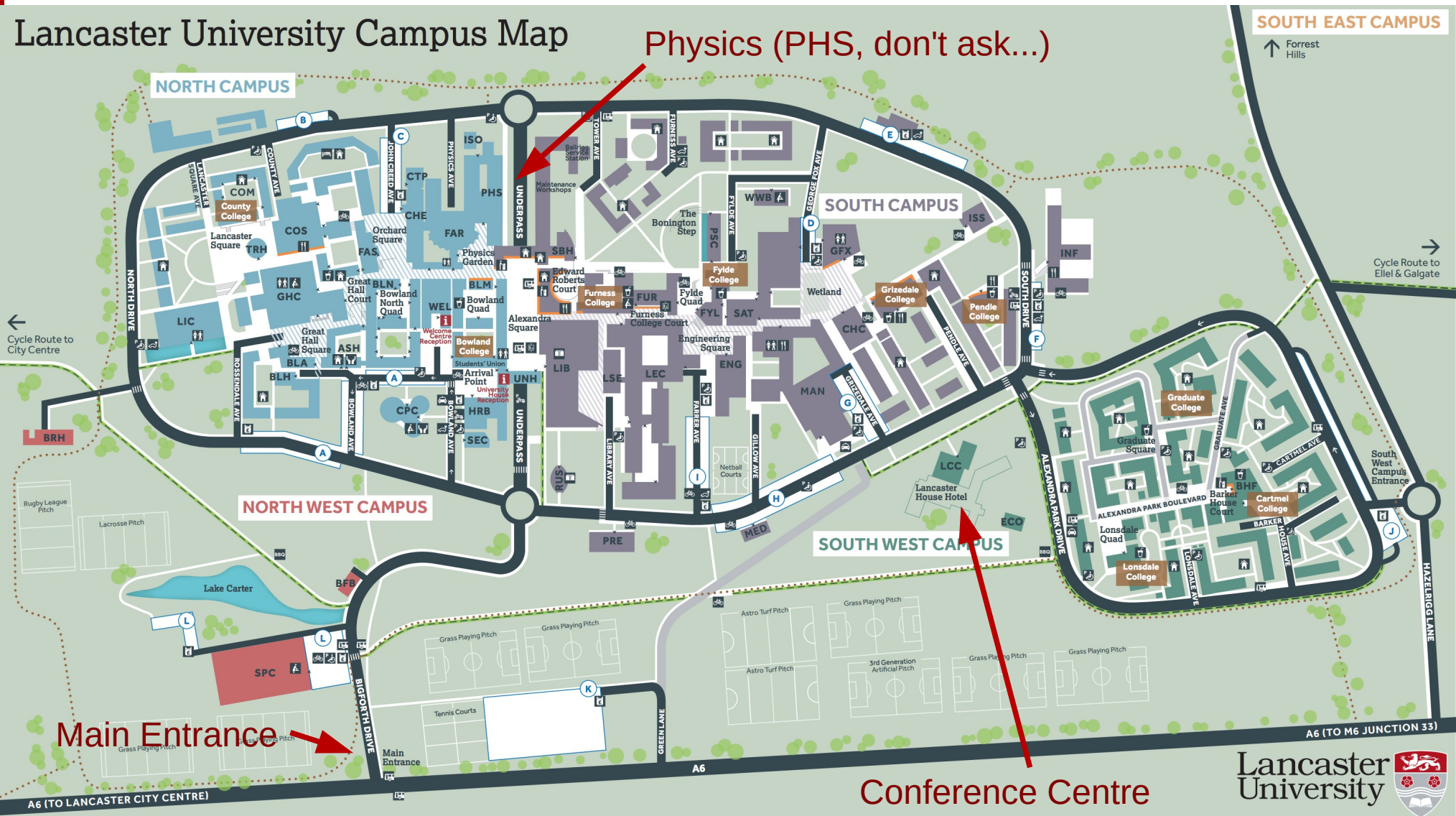
Local map

- University Campus located south of Lancaster
- Train station just west of city centre
 - there are direct busses, but more frequent busses from the central bus terminal (north end of city centre)
 - you can also take a taxi (~10 GBP)
- Motorway (M6) exit south of campus (“Lancaster south”)



Campus Map

- <https://www.lancaster.ac.uk/media/lancaster-university/content-assets/documents/maps/campus-map.pdf>



The Physics Building (PHS on the map)

- Freshly refurbished
- Access both from the ring road and from “the spine” - the central walkway connecting all buildings for pedestrians
- Park in visitor car park B if arriving by car, and get a scratchcard from me (beware of fines!)
- Bus stop under Alexandra square (central square)



Room options

- June is still term time, but rooms are available near the Physics building or a little separate but still on campus
 - or we could opt for a retreat in “Forrest Hills”, featuring even a Golf Course...
- B&B accommodations available on campus (35-52 GBP/night singles, 62 GBP/night double)
- Rather cheap AirBnB options close to the university
- Lancaster House Hotel also on campus
 - ~90 GBP/night, but a real hotel...
- Will need to charge a conference fee for room hire (!) and catering (coffee breaks, catered lunch)
 - but the “customary” 150 EUR should be sufficient
 - can include the workshop dinner



Leisure...

- Lake District and Yorkshire Dales close by
- Might be an incentive for additional time before/after the meeting...



When?

- Traditionally, RD50 meets in early June, but there have been exceptions
- Early June clashes with school holidays (June 3) and Pentecoste (June 8-10)
- Possible dates (some caveats, let's get a preference picture and then sort out the details):
 - June 5-7 (Wed-Fri), “the classical date”
 - June 11-13 (Tue-Thu)
 - June 12-14 (Wed-Fri)
 - June 17-19 (Mon-Wed)
 - June 18-20 (Tue-Thu)
 - June 19-21 (Wed-Fri)
 - June 24-26 (Mon-Wed)
 - June 25-27 (Tue-Thu)
 - July 1-3 (Mon-Wed)
 - July 2-4 (Tue-Thu)
 - July 3-5 (Wed-Fri)
- Agreement via doodle within the next days (email to follow):
<https://doodle.com/poll/87m3h56dypabathh>

Schedule details/travel

- RD50 workshops most often started on Monday mornings and ended early on Wednesday afternoon
 - forces travel on Sunday
 - not optimal for people with family commitments (like me)
- Proposal for both the next workshop at Lanaster and the future in general:
 - start after lunch on Monday to allow travel in the morning, and in turn finish late on Wednesday afternoon
 - same number of nights required, but Mon-Thu instead of Sun-Wed
 - alternatively, start on Wednesday morning, then travel can be on Tuesday afternoon and Friday afternoon
 - or start Wednesday at noon (i.e. travel on Wednesday morning) and then travel back on Saturday morning (usually much cheaper)

Summary

- We are looking forward to hosting you in June 2019!
- Date to be fixed very soon with your input (so let us know!)
- Travel reasonably easy via Manchester Airport (largest UK airport outside London) with lots of direct connections

AND

- Please fill in the doodle poll to give your availability, use the comments to give us additional input!

<https://doodle.com/poll/87m3h56dypabathh>