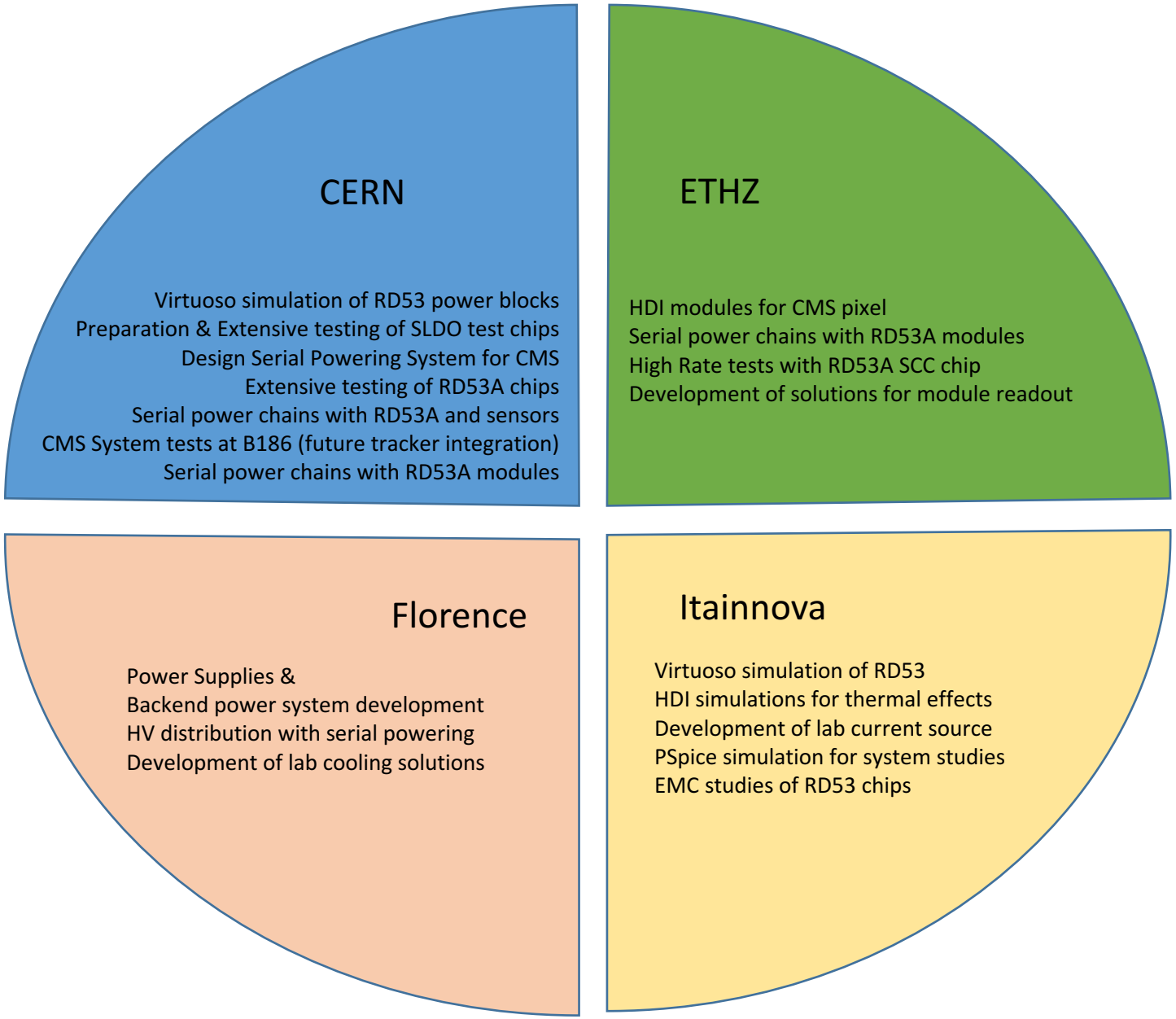
SP testing and plans for CMS

SP for ATLAS and CMS pixel detectors

https://indico.cern.ch/event/755140/

CMS Serial Powering activities



Measurements done at CERN

Extensive measurements with 2.0 SLDO test chip **(Nov 2017-Feb 2018)**

Line/Load regulations
- Slope & Offset discrepancy

Current sharing and power up
- With current source prototype from ITATINNOVA

Exploring the limits Vin>2V & Iin>2A

RD53A Bare Chip Measurements **(Feb 2018 - July 2018)**

Line/Load regulations
- Slope & Offset discrepancy
- Start-up behavior of bandgaps

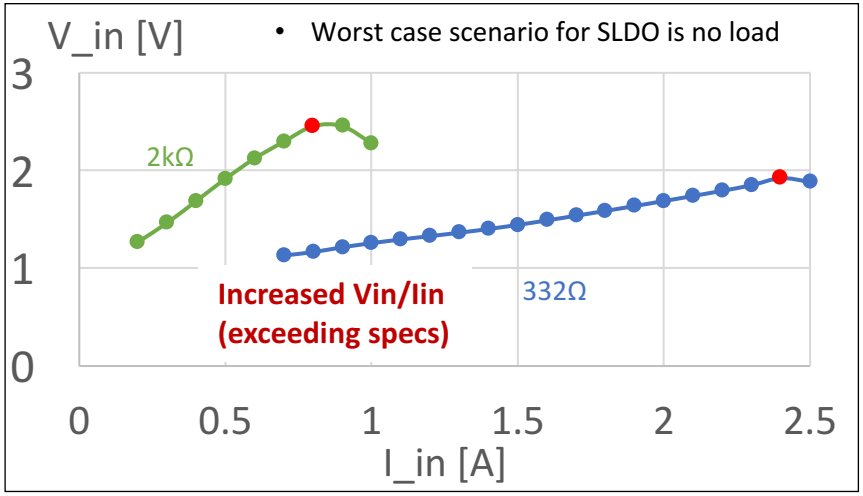
Tests in climatic chamber
- Variation of reference & bandgap output voltages across temperature
- Line regulations at different temperatures -> Different bandgap “start up”-behaviour

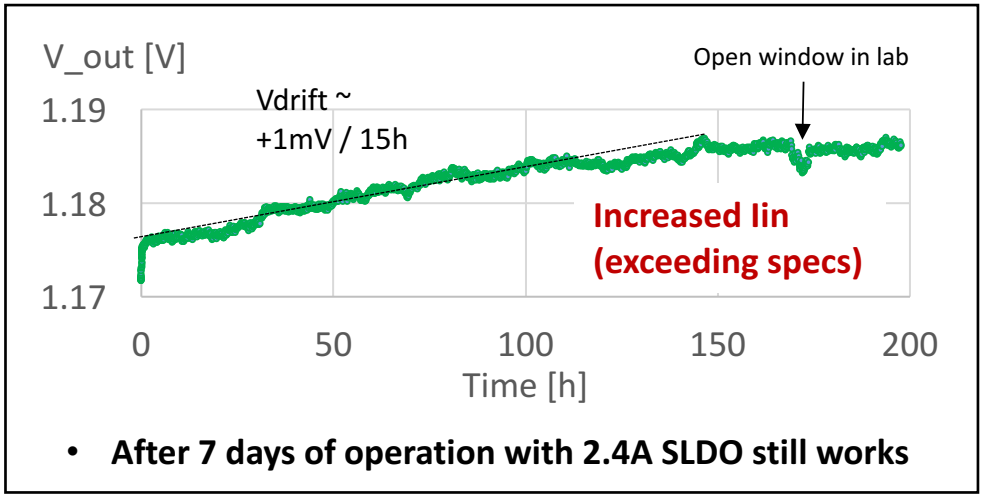
On-chip load tests by creating transients in both domains:
- Activating/Deactivating clk for digital
- Enabling/Disabling analog

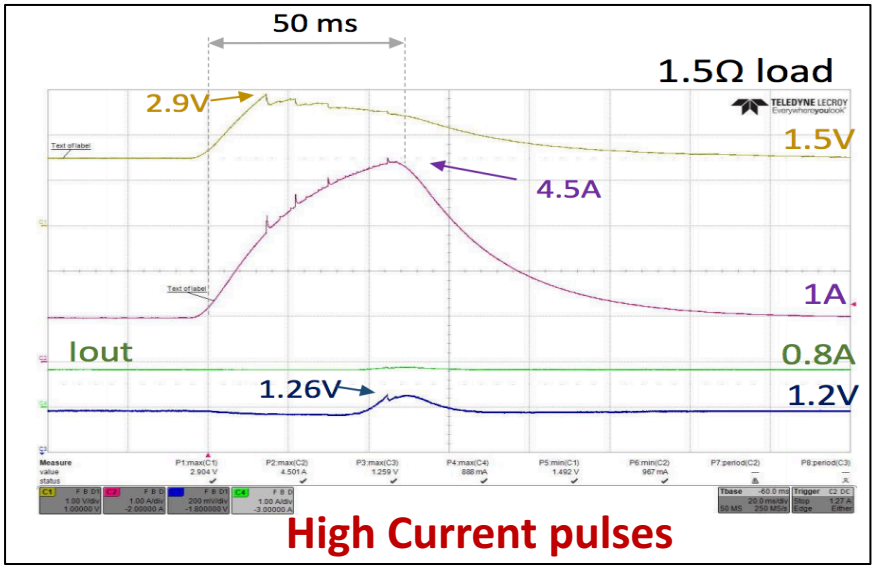
RD53A with Sensor Measurements **(Aug 2018 - now)**

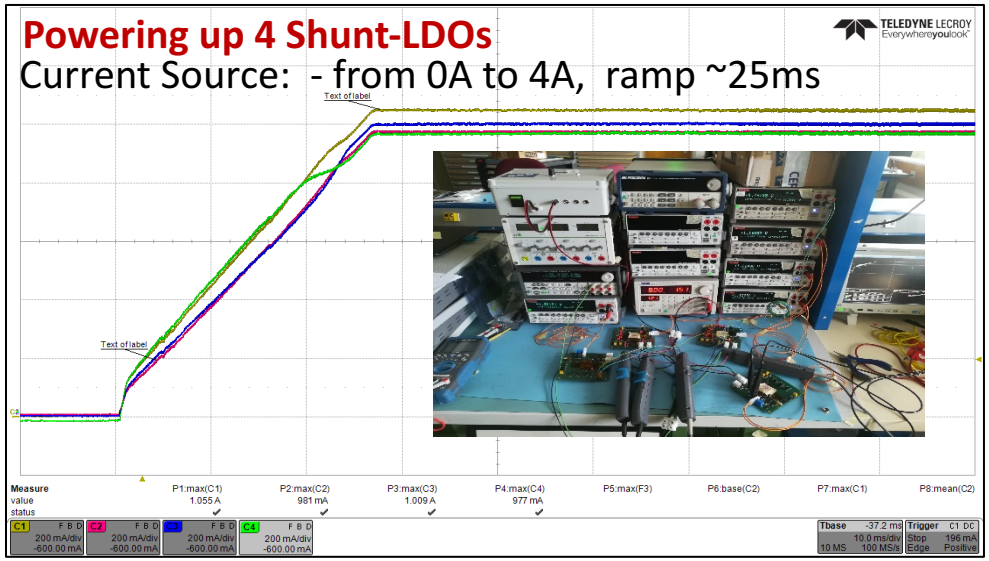
Serial power chain of 4 RD53A modules in test beam
- In serial chain (1x4, 4x1)
- Different HV schemes
- Successful data taking

2.0A test-chip: Reliability & Current Sharing tests







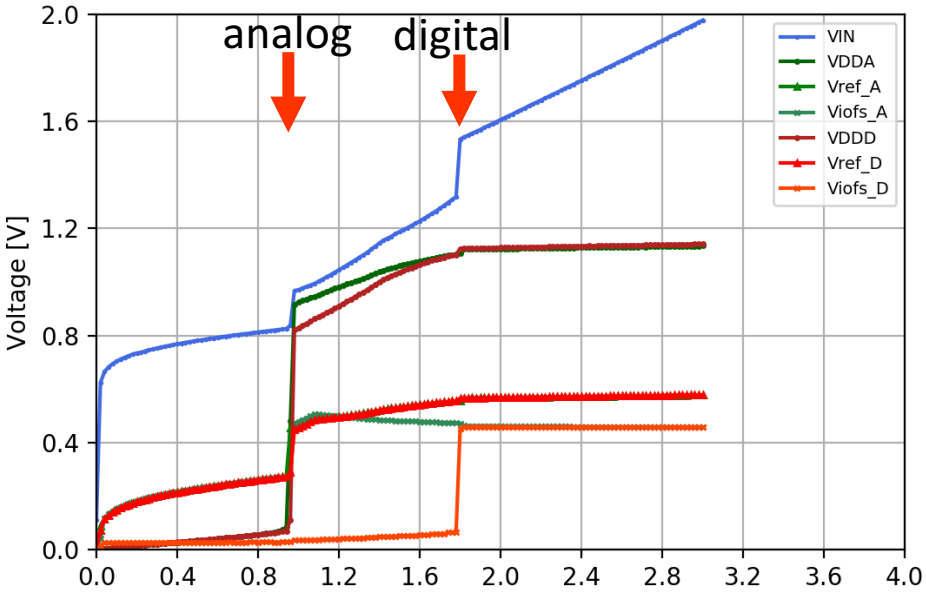


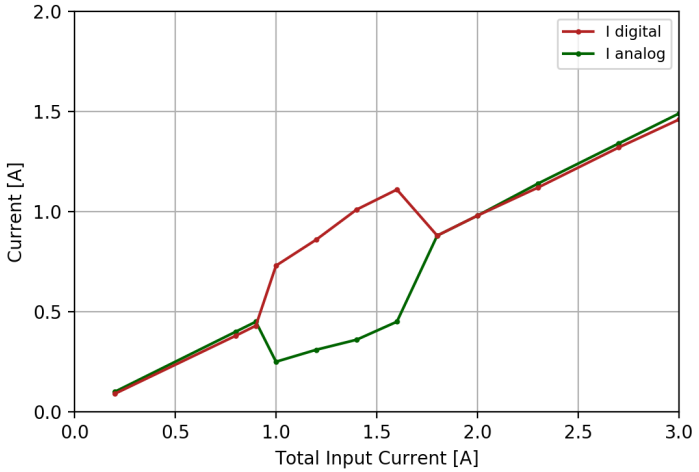
Line regulation - bandgap startup voltage

- Some bandgaps need higher V(I) to start up
- Seen with **different** bandgap voltages (VrefA, ViofsD, ViofsA)

  => Example of late digital Vofs shown here
- After bandgaps "started" dynamic range is good
- Unequal current sharing "*Eye*" possible:
  - When Vofs starts, SLDO gets into higher ohmic state

  => Jumps in current sharing





Line Regulation at different temperatures

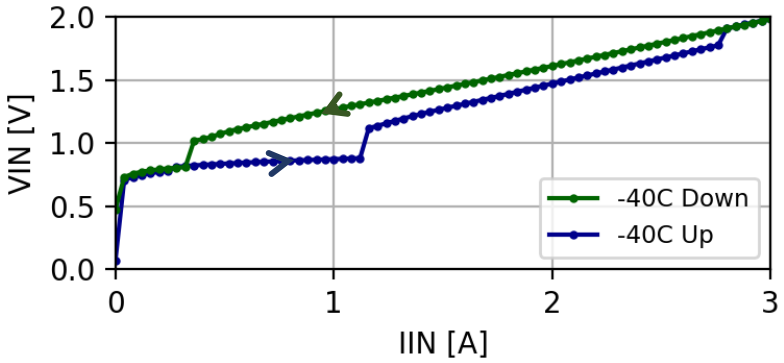
- Seen with **different** bandgap voltages (VrefA, ViofsD, ViofsA)

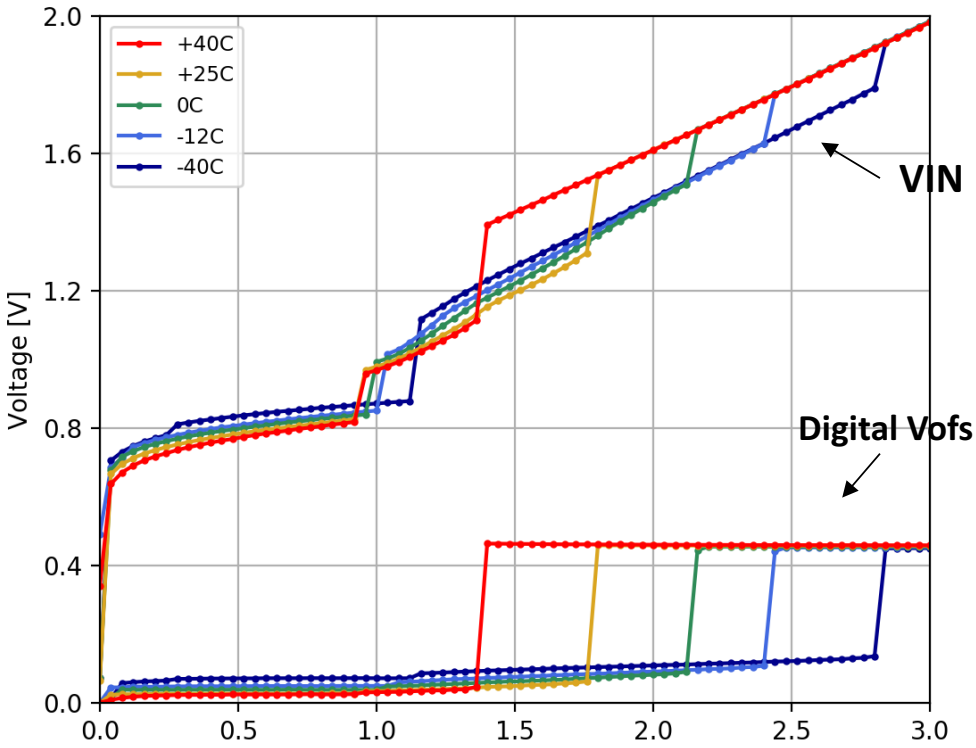
  => Example of late digital Vofs shown here

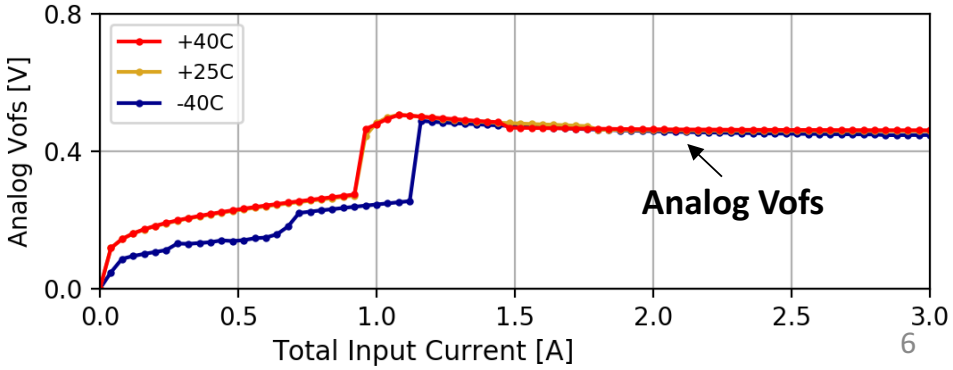
- Higher voltage/current needed with lower temperature

- Only “start up” problem

=> Once start up dynamic range is very good:







Power Consumption & Load Regulation

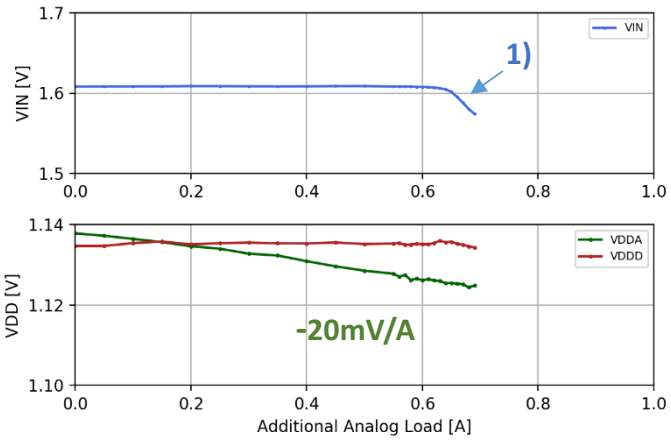
Load current measurement for ShuntLDO-mode not implemented in RD53A

=> Load regulation by draining additional Load

- Consumption of RD53A after power up without clock (DP not connected):

	Analog	Digital
After power up, without clock	~400mA	~50mA

a) Additional analog load:

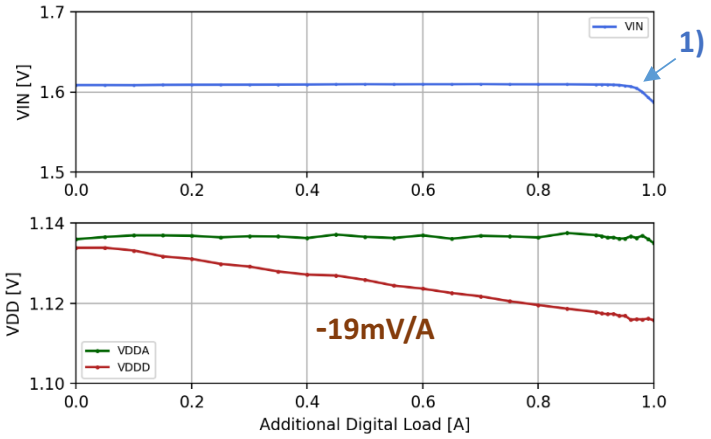


Results

- No differences between analog and digital regulator
- Voltage with load decreases by ~20mV/1A load
  => Other voltage stays stable O(1mV)

1) When total load current reaches supply current (1A per SLDO)
   => ShuntLDO regulator cannot regulate properly
   => VIN starts to decrease

b) Additional digital load:



Next serial power studies planned at CERN:

8 SCC modules for SP testing

- 1 (+1) KC705, 1 CERN FMC, 1 DP-to-SMA, 2 Ohio FMC for clk/cmd fanout

Shunt headroom studies

- Define average power & Tests with different configuration for analog and digital SLDO

Chain transient, Failure modes

- Transients through operation -> Overload situations and load fluctuations
- Force voltage transients & Emulate shorts / opens

DAQ

- Use chip ID to independently configure chips with 1 board

HV studies

- Test with CAEN HV supply: Floating channels, Off-mode
- More studies?? Noise??
- ~Destructive tests: Forward biasing of sensor ?

Power up & Long cables

- Current source from ITAINNOVA & prototype service cables

AC coupling

- Investigate potential voltage spikes due to AC capacitor charging

Temperature studies

- Active cooling with Peltier element for 1 chip available
- Slope, Offset vs T

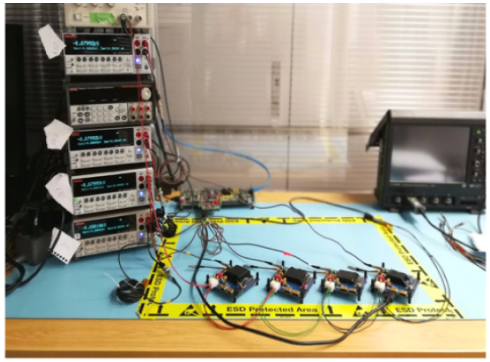
New SLDO prototype testing

- Typical characterization measurements

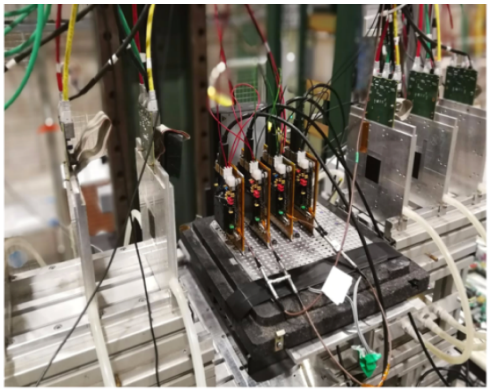
Ongoing System tests for CMS

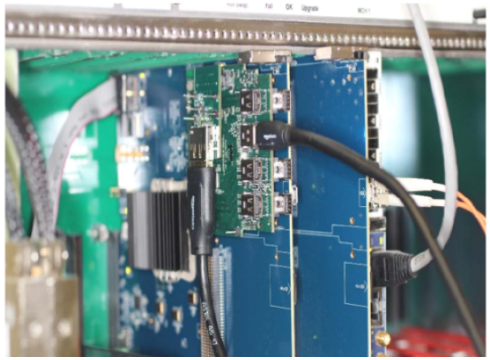
- Ongoing activities (Q4 2018):
  - Serial power validation with single RD53A modules in lab and testbeams
    - ~10 modules on bench with realistic cables, power supplies
    - Addressing HV distribution
    - Failure modes with chains of chips
  - Extensive RD53A tests for feedback for final ASIC design
  - First e-links tests with RD53A chip
  - Development of DAQ hardware for multiple chip readout
  - Preparing services for larger volume tests
  - High rate tests with RD53A
- Next steps (2019):
  - First chains of multichip modules (HDI)
  - Readout chain validation with LpGBT
  - First integration tests on realistic structures

Serial power chain of 4 single chip modules

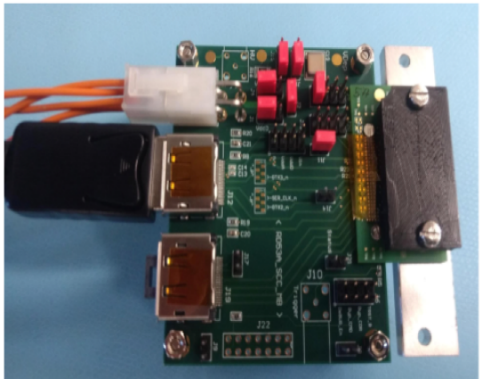


Serial power chain in a test beam





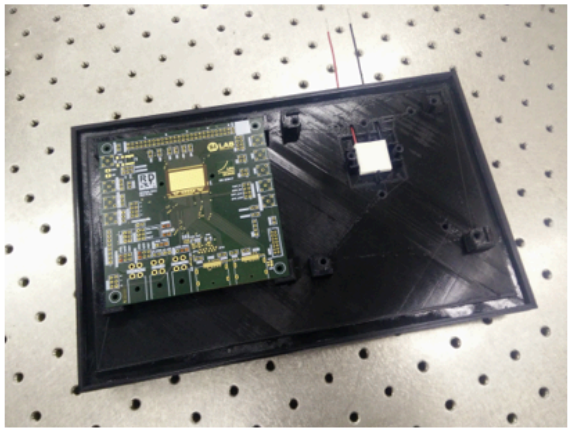
New Readout Interface Card
for Multiple Chip Readout & FC7



Tests of Light Irradiation SCC card

Serial Powering / System Test activities in Firenze: medium term planning

- People: Antonio Cassese (postdoc), Rudy Ceccarelli (PhD), Marco Meschini, Simone Paoletti, Giacomo Sguazzoni
- The group is restructuring: activities are being reorganized
- Items on which the group could contribute in the next months:
  - commissioning of Peltier-based temperature controlled system for SCC cards; useful for quantitative measurements in the context of different powering and HV distribution schemes
  - study of HV distribution schemes with planar and 3D sensors with CAEN A1515 (16x 1kV floating channels)
  - system tests with SP chains, (long) prototype cables and suitable sources



ETH zürich

Serial powering activities and plans at ETH

Malte Backhaus, Vasilije Perovic, Branislav Ristic, Daniele Ruini, Gianluca Vagli

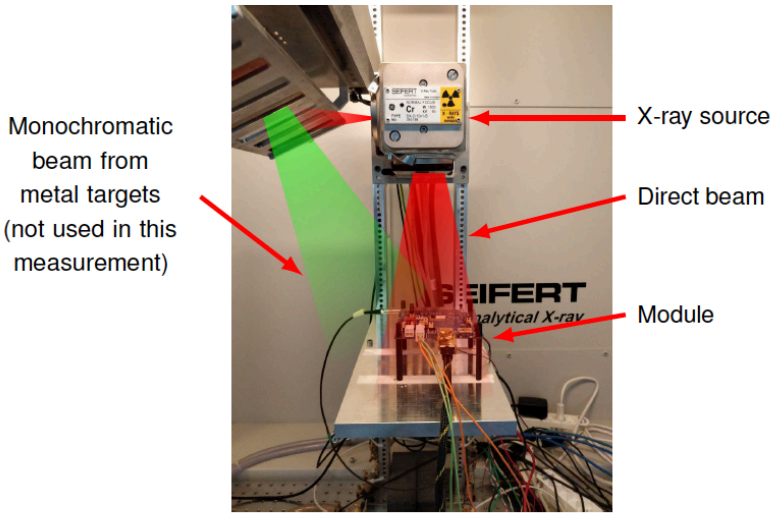
IPA

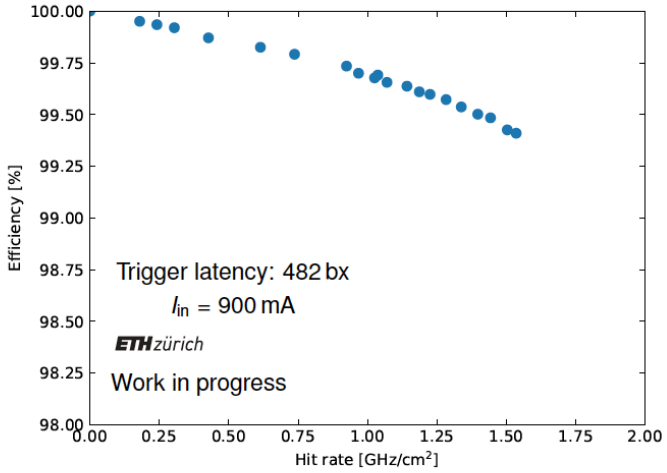
Serial powering staff

- 2 postdocs: Malte, Bane.
- 2 PhD students: Vasilije, Daniele (will soon leave SP).
- 1 master studend: Gianluca.

Current activities: SP chain of RD53A

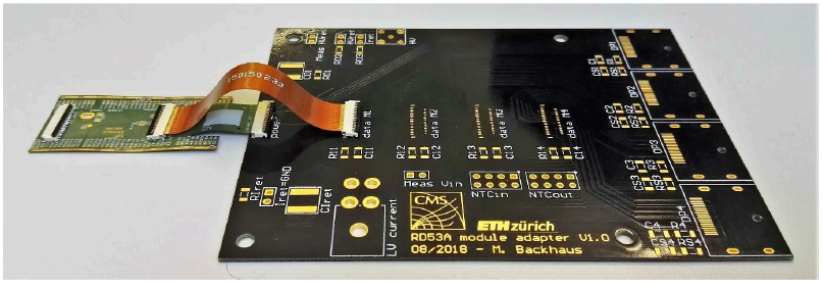
- We currently have five RD53A SCCs: four with bare chips, one with sensor.
- Plans:
  - operate them in a chain, see also tests done last week at CERN;
  - measure efficiency in high hit rate environment with X-rays.





Current activities: RD53A modules

- HDI (and adapter PCB) designed and in hand.
  - HV and thermal stress tests ongoing.

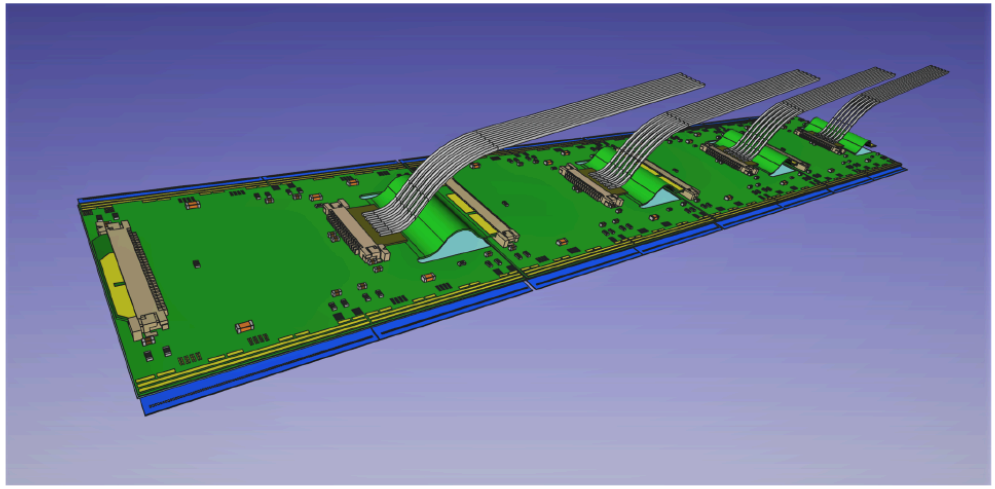


- Preparing for construction of “digital” modules (w/o sensor) to test HDI functionalities, wirebonding, ecc.
  - First module ready this week.

- Once we have enough modules: operate them in a SP chain.

Future plans: detector mechanics

- Detector mechanics with CO_2 cooling being designed.
- Plan to build one structure with four ladders:
  - Two equipped with heaters ($\sim$ April 2019).
  - Two equipped with modules: RD53A first (2019), then real modules when these are available (2020–21).



1. Introduction

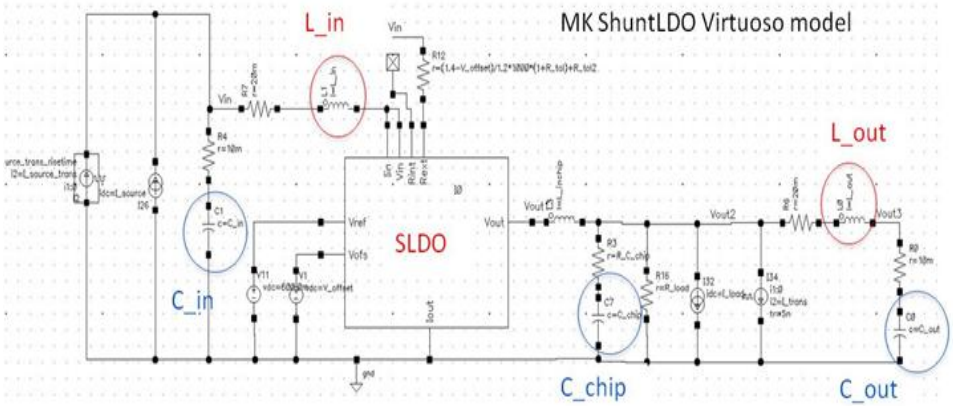
- ITAINNOVA contribution to CMS Pixel Phase II is focused on system aspects of power supply distribution.
  - Simulations
  - Components and system prototypes development
- These activities may be grouped in three areas:
  - RD53 ROC (power stage)
    - SLDO Simulations (Virtuoso & Pspice Mod) & measurements
  - HDI design and development (HDI-BPIX)
    - SiWave simulations and prototype development (2x1 HDI BPIX)
  - EMC (grounding and transients) studies
    - Prototype development (PS, SP chain for EMC purposes)
    - EMC tests

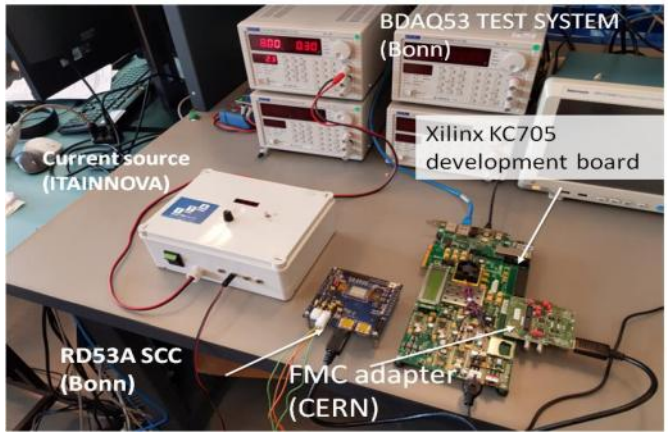
2. RD53 activities

- Main goal of this part of the project is to develop a simulation models to understand the performance of the power stage of the RD53A & B chip.
- For that purpose several simulations have been carried out to find any failure scenario of Shunt-LDO before the chip submission, and to analyze system level behavior:
  - Component level:
    - Stability issues
    - Effects of parasitic inductances (PCB and system level) & internal chip C
    - Start-up behavior
  - System level :
    - Decoupling capacitors optimization
    - Full system level model (Source + wiring + PCB parasitics + shuntLDO)
    - “Real” current source model validation & Power dissipation aspects

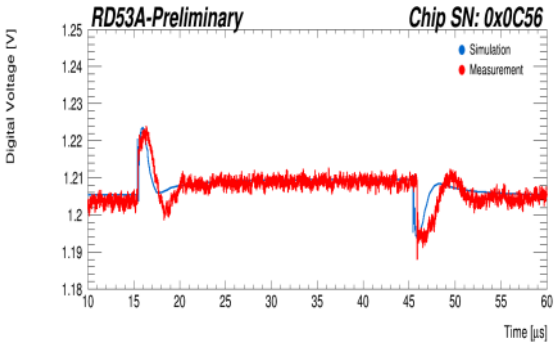
2. RD53 activities

- These activities have been performed in collaboration with Stella and Dominik within RD53 Network and coordinated by Jorgen.
- These activities have included simulation models and real test on RD53A ROC.
  - Dynamic response of the SLDO
  - SLDO configuration (Voffset, Rin)
  - Start-up behavior
    - (BG, Current source, ..)
  - ROC power dissipation

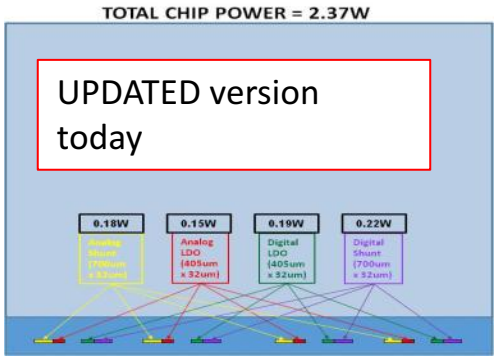




Dynamic response of SLDO



Power Model of Final chip

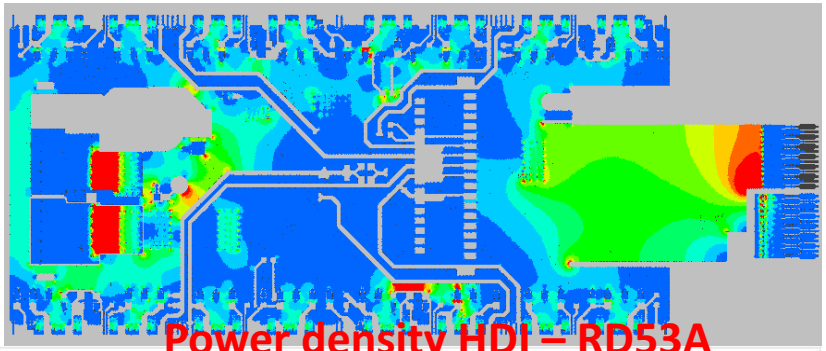


3. HDI design and development

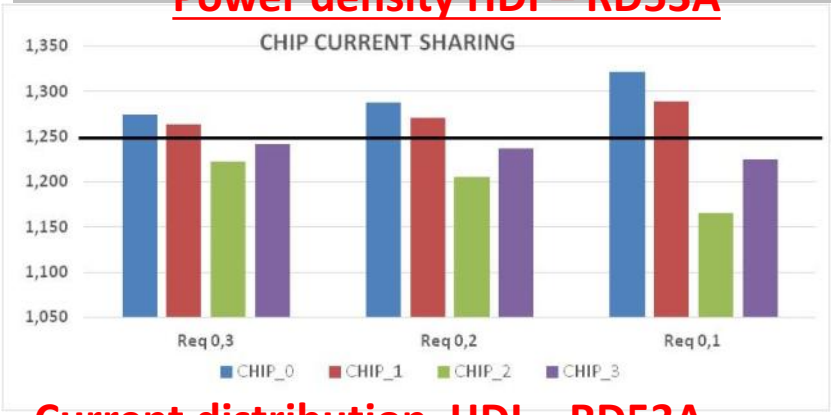
- ITAINNOVA is involved in the BPX-HDI design (2x2 and 2x1)
- The activity is divided in two parts :
  - Perform several simulations of the HDI in order to verify the performance of the HDI
    - It helps a lot to evaluate designs
  - Design the HDI 2x1 BPIX design
- This activity is coordinated with ETHZ (Malte) and within HDI working group.
- Actual status
  - Simulations models of the HDI2x2 RD53A
  - Design and Simulations of HDI2x1 RD53A

3. HDI design and development

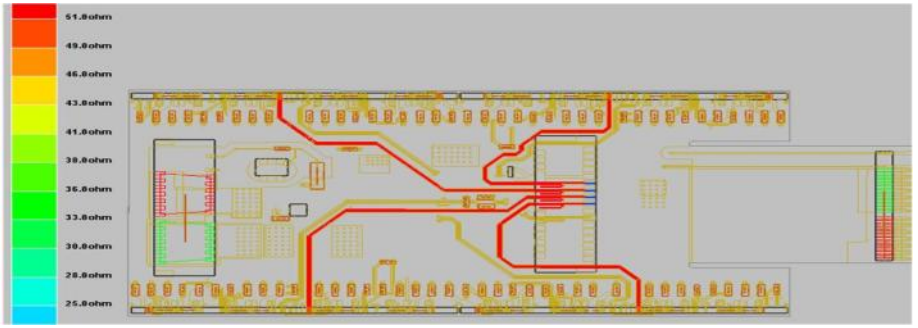
- A first estimation of the power dissipation of the HDI 2x2 RD53A has been performed (~ 500 mW)
  - Chip current sharing due to SLDO configuration (mismatching)
- Signal lines impedances has been verified too.
- Model validation will be perform with the HDI – 2x2 RD53A



Power density HDI – RD53A



Current distribution HDI – RD53A



Signal line Impedance (CM &DM) HDI

Net Name	Z of Longest Violation/Warning (Ohms)
DO0_N	52.1
DO0_P	52.1
DO1_N	52.1
DO1_P	52.1
DO2_N	52.1
DO2_P	52.1
DO3_N	52.2
DO3_P	52.2

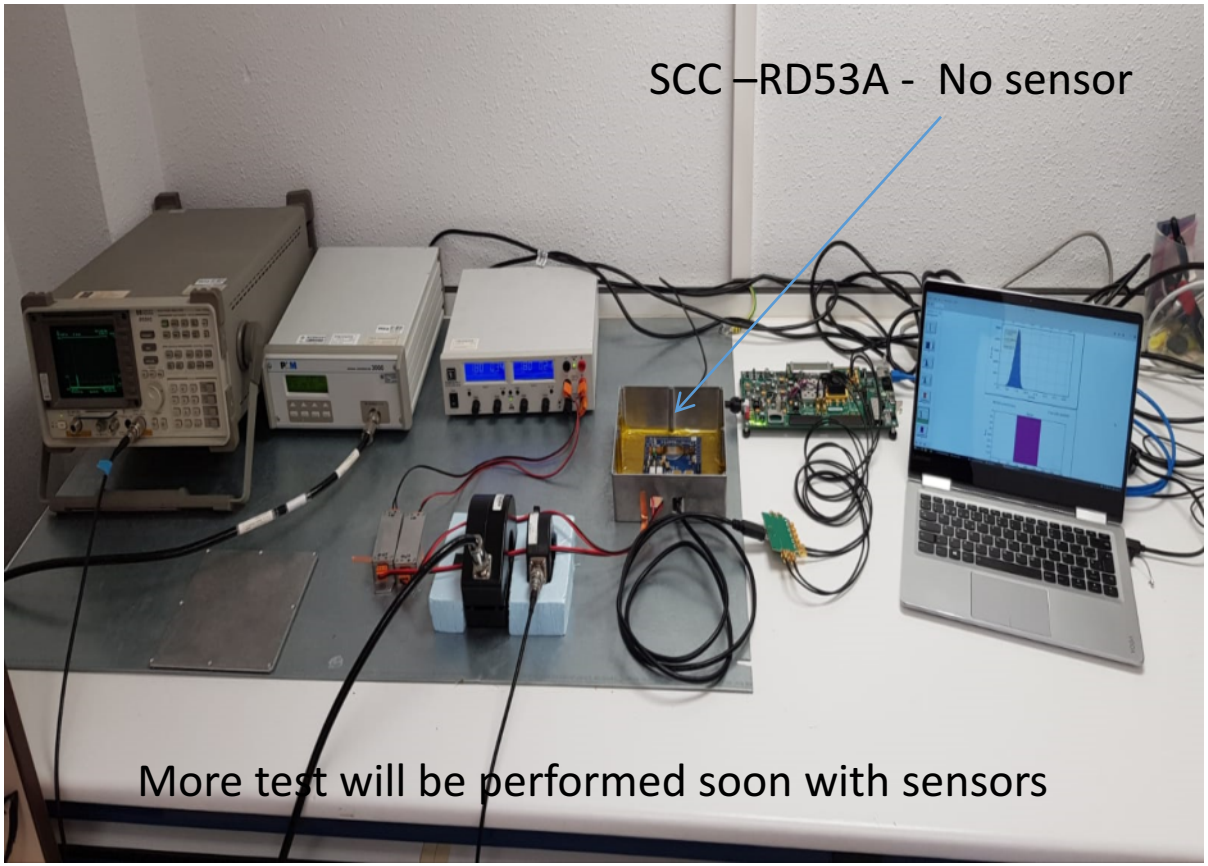
Net Name	Z of Longest Violation/Warning (Ohms)
DO0	92.9
DO1	92.8
DO2	92.9
DO3	93.0

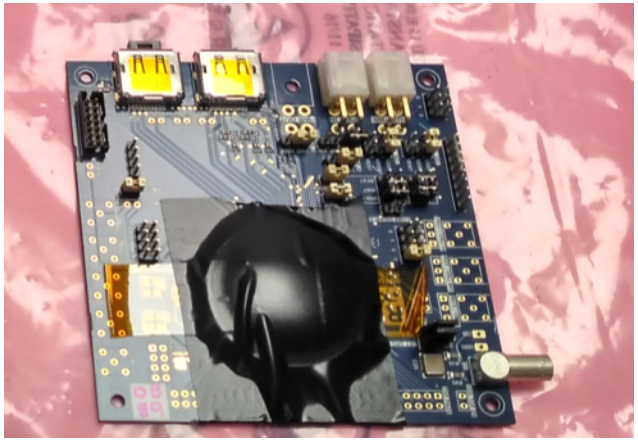
4. EMC studies

- The main goal of these activities is to perform EMC studies that will be used to evaluate grounding topology and transients present in SP power distribution system
  - The idea is to perform several EMC test that allow to gain insight in the noise issues of SP topology.
- For that purpose several activities are planned
  - SCC with & without sensor susceptibility
  - Small serial power chain with 4 SCC (3 no sensor as a dummies & 1 with sensor) – Grounding configuration.
  - Serial power chain susceptibility with HDI 2x2 (TBD with Malte)
  - Transient & failure tests with dummy boards

4. EMC test studies

- First EMC test has already perform (with standard PS unit) with SCC without sensors
  - Much more immune to the one tested as a reference with FEI4.





5. Summary

- ITAINNOVA activities on CMS pixel phase II are focused on serial powering aspects.
  - RD53 design – Power stage
  - HDI design
  - EMC test – Prototype development
- All activities are complementary
  - Example: HDI current distribution based on SLDO mismatch (Voff – Rin Configuration) & SLDO simulation of parasitic components.
  - Example: EMC test on SCC will be performed with SCC with the Cin similar to simulation models of RD53A.
- ITAINNOVA plan to continue this activity (Future plans)
  - RD53: LPM, SLDO verification, Failure scenarios, BG effects.
  - HDI: Design and Simulations of HDI2x1 RD53A & HDI 2x2 Support
  - EMC test: EMC test on SCC (1 & serial power chain 4 SCC)