Fachhochschule
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Shunt-LDO Regulator

New Features

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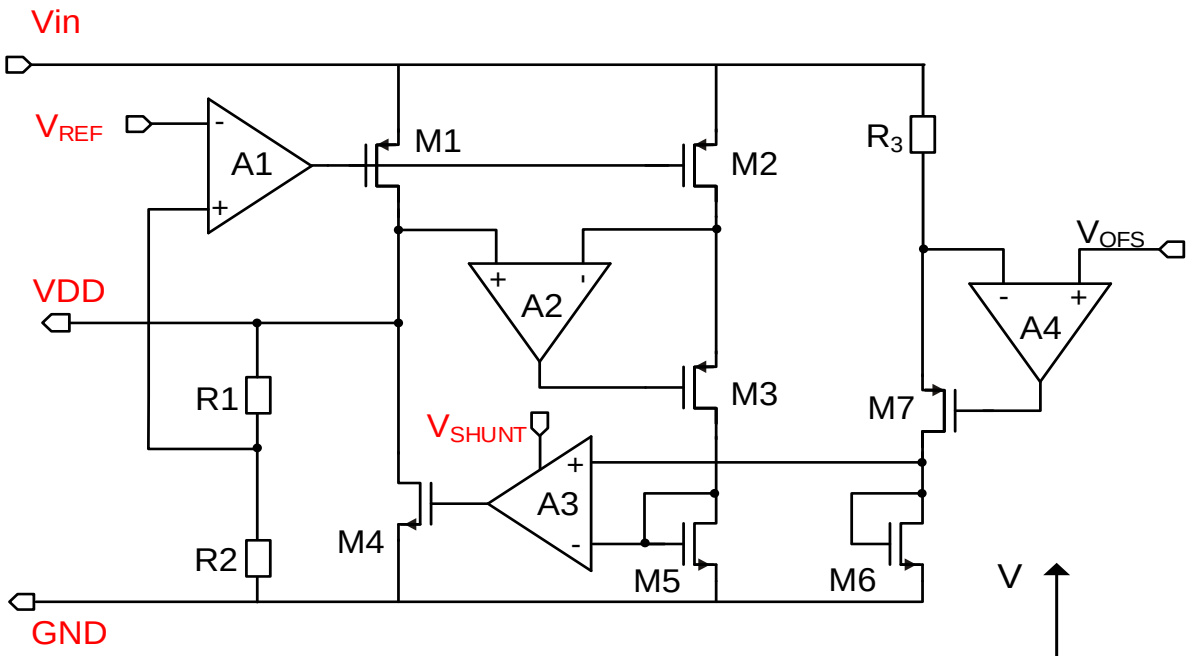
Serial powering for ATLAS and CMS pixel detectors

Shunt-LDO Regulator

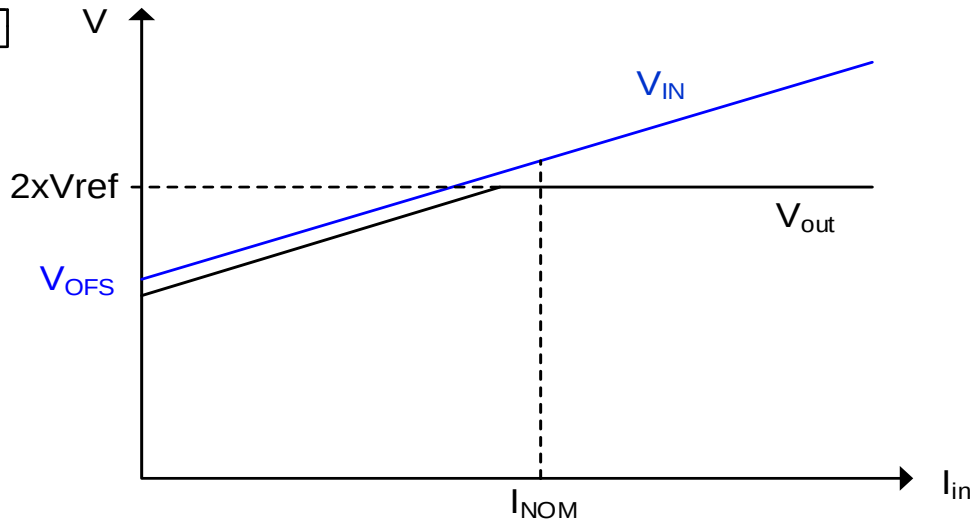


SLDO regulator:

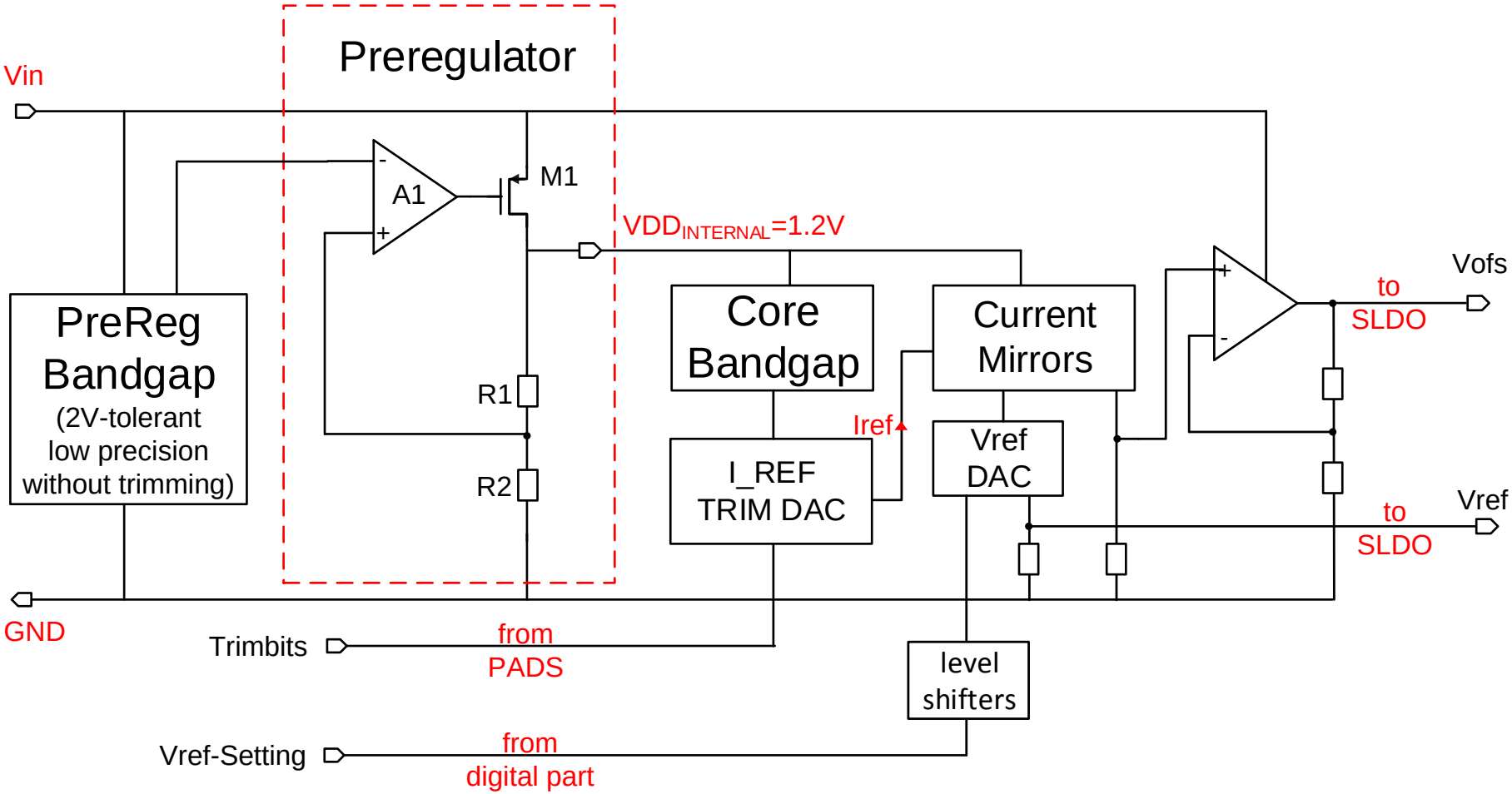
- combination of LDO & shunt regulator
- current not dissipated is shunted
- regulator input impedance defined by R3 and Vofs
- output voltage defined by Vref

SLDO input impedance characterstic reminds

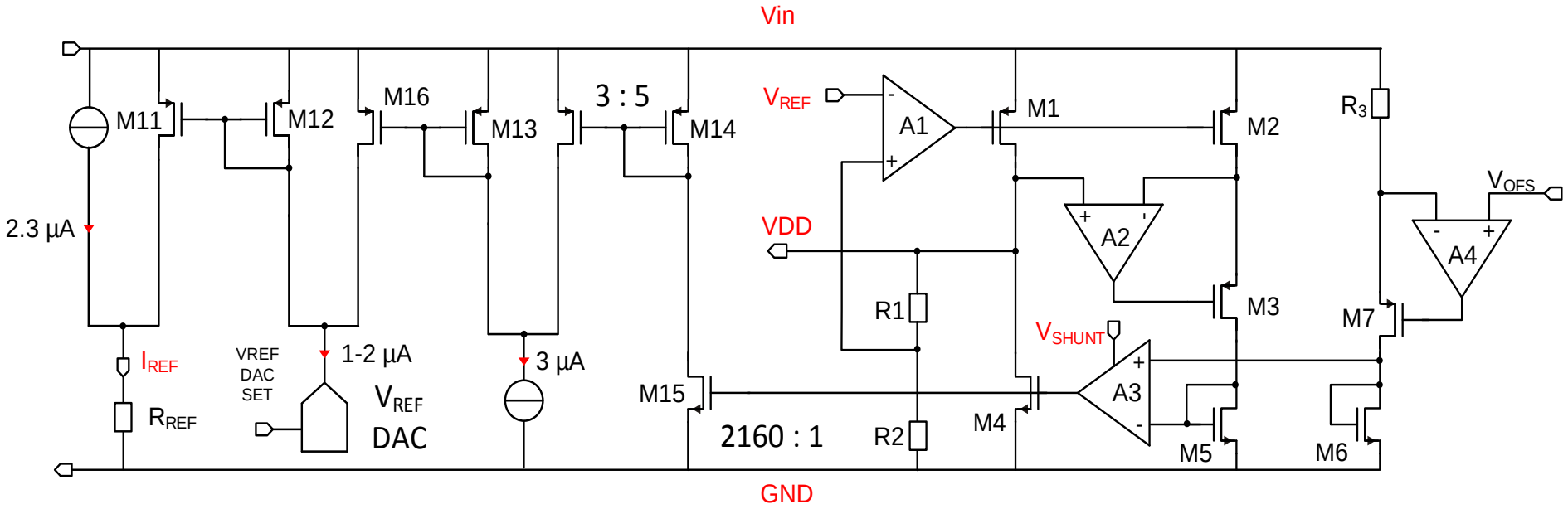
- voltage source with series resistance
- Zenzer diode with series resistance



New SLDO Biasing Scheme



Under Shunt Protection

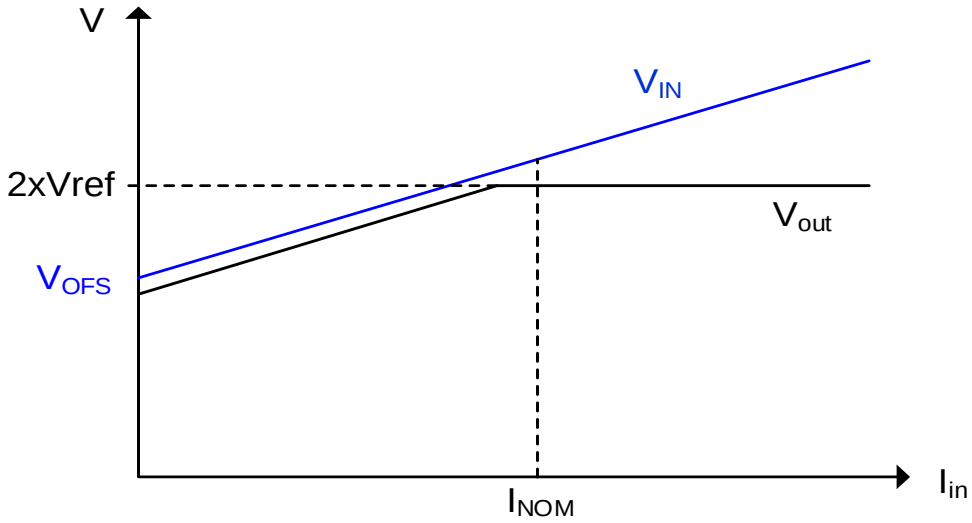


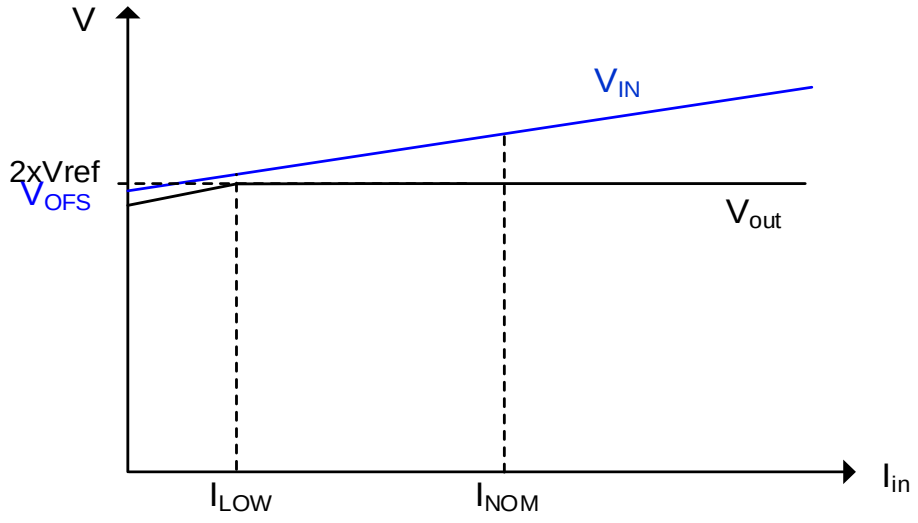
- overload current situation is considered as undershunt current scenario
  - high load current reduces shunt current
- In undershunt current case Vref is reduced
- minimum voltage defined by current source
  - Vmin=2.3µA x 150kOhm=350mV
- additional injected current (1-2µA) can be configured by DAC setting
- At shunt current lower < 11 mA addition current is disabled

Low Power Mode

- During detector assembly tests will be performed without active cooling
- Three approaches are studied
  - high Vofs voltage & low slope
    - Startup circuit for Vofs generator required
  - Power-On Mode detector (Alvaro Pradas)
    - Monitors the input current during power-up and switches to respective power mode
  - AC coupled control signal (Hans Krüger)
    - AC signal applied before power-on
    - rectifier generates supply voltage for a small digital configuration circuit

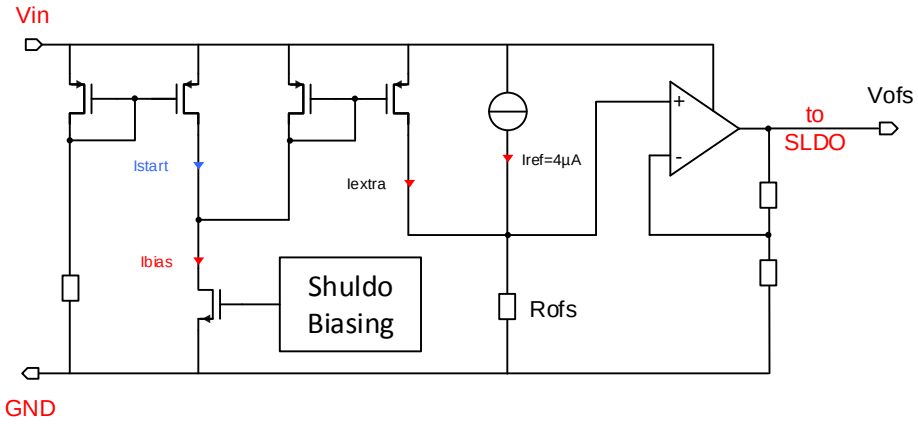
High Vofs & Low Slope Approach

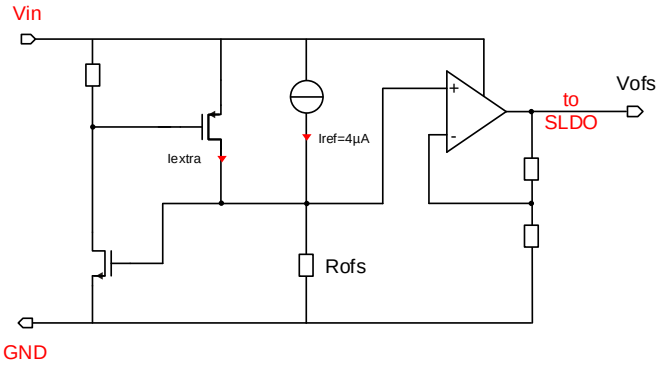


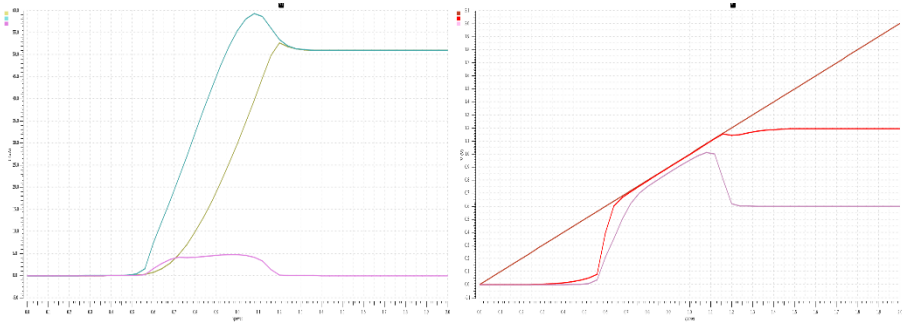


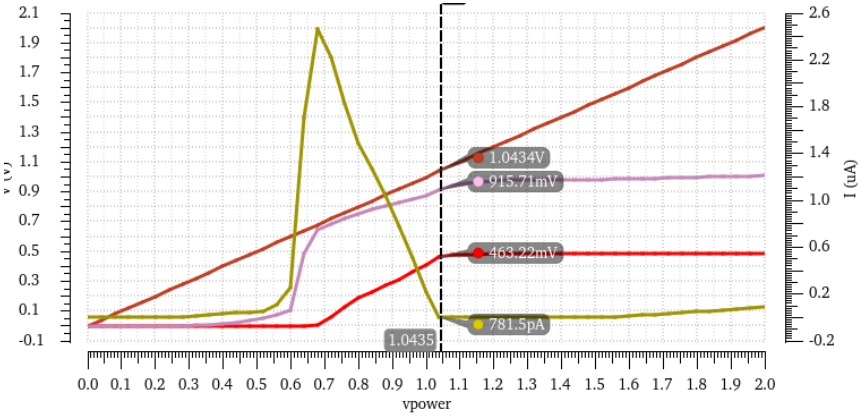
- Vofs is shifted closer to the reference output voltage
  - With smaller amount of input current a sufficient input voltage level is reached
  - Increasing the input current the nominal operating point is reached at higher voltage drop

Vofs Startup Circuit









TO DO LIST

- finalize startup-circuit for high-Vofs & low slope approach
- implement Power-On detector
- study potential AC coupling implementation
- Verfication tasks
  - monte-carlo start-up circuit of parallel chips
  - introduction of Radiation Models into Verification Plan
  - 100mA simulation for low power mode drop-out requirement
- Implementation Tasks
  - Vin Monitoring Resisors Change Ratio 1:4
  - shunt load current monitoring circuit
- Voltage-clamp