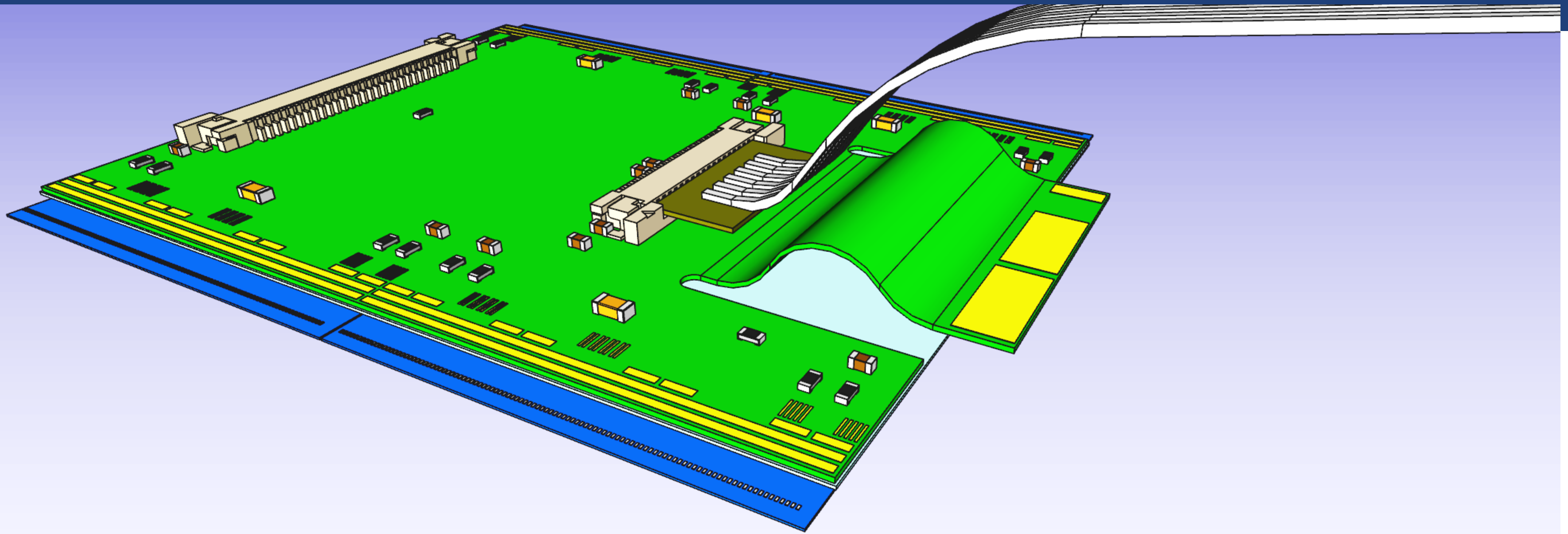
ETH zürich



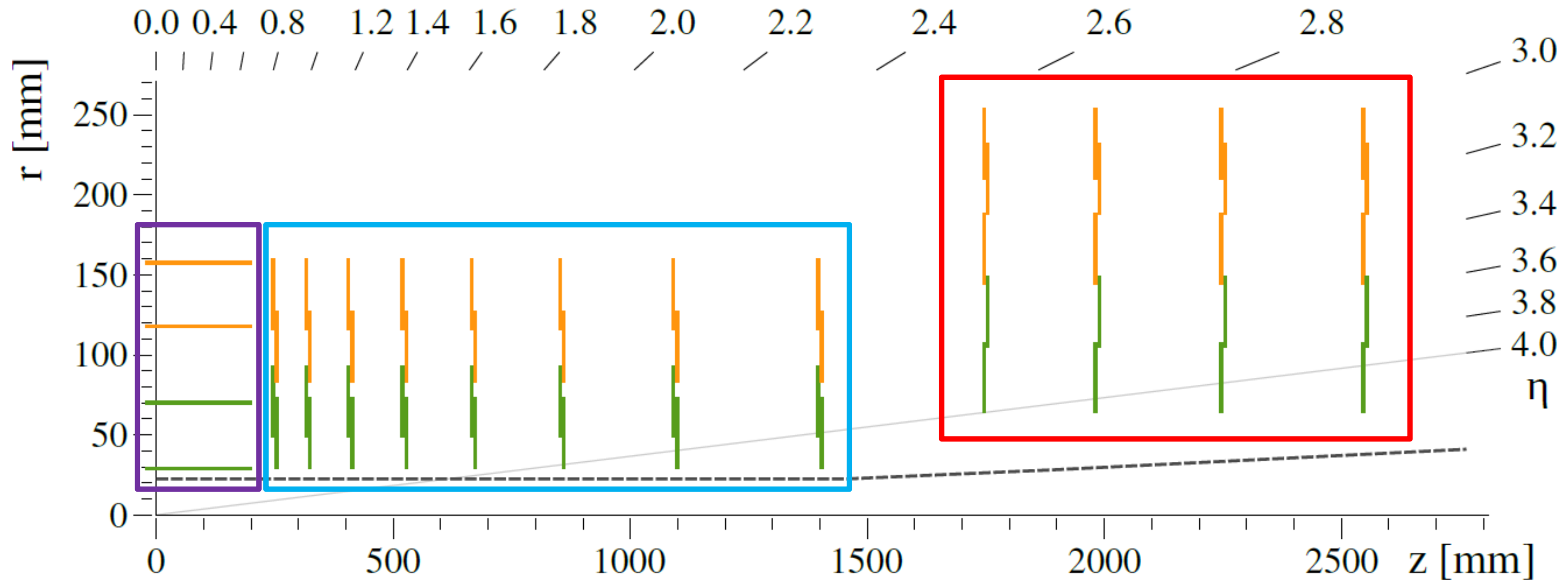
Module issues related to SP: CMS

Malte Backhaus, CMS phase 2 IT module WG

IPA

Outline

- CMS pixel detector parts
  → and consequences for module SP
  → Module HDI design
- Simulations of HDI
- Barrel HDI prototype
  - Results
  - Further plans
- Barrel thermal simulations
- Summary



TBPX – central barrel → 1x2 and 2x2 chip modules
TFPX – forward discs → 1x2 and 2x2 chip modules
TEPX – very forward discs → only 2x2 chip modules

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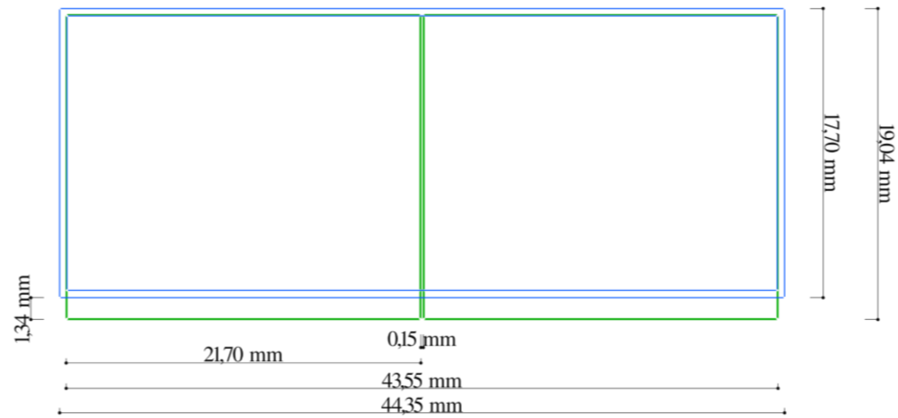
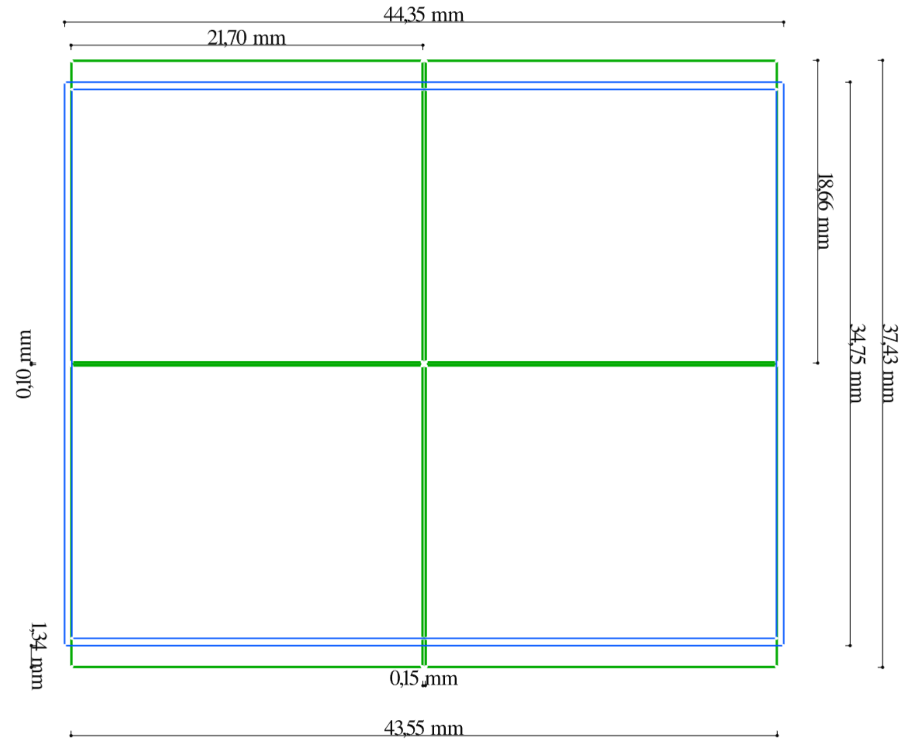
Module dimensions

1x2 module

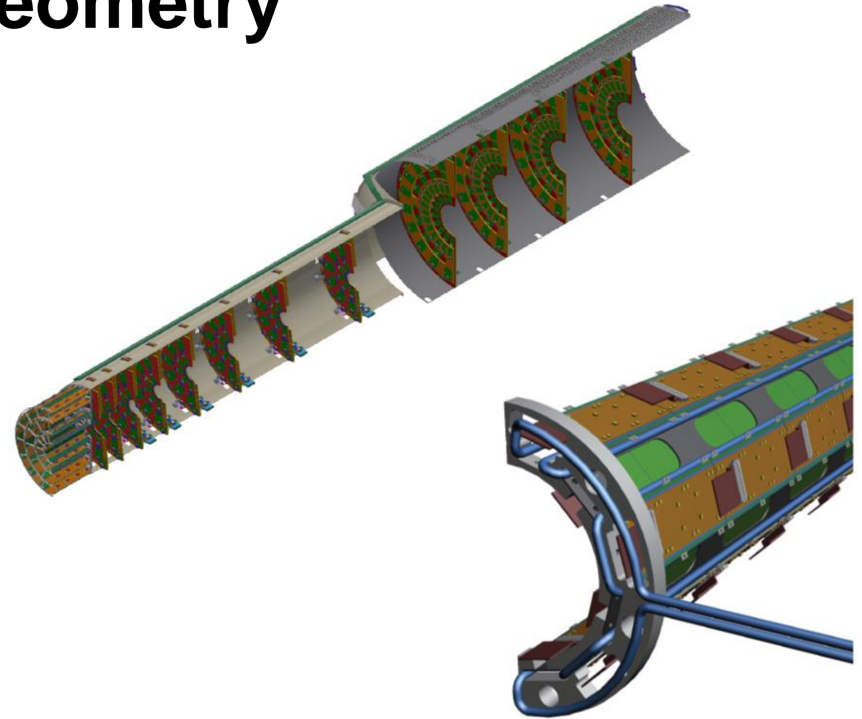


2x2 module

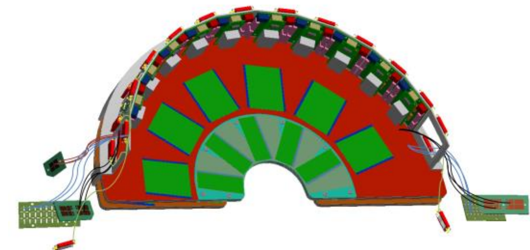


IPA

Installation and overall geometry



- Installation from both detector sides
  → merging region in center of detector
- TBPX and TFPX services integrated on TFPX tube (baseline)
  → One structure for installation
- TEPX independent of TBPX/TFPX
- Module constraints from geometry:
  - Ladders in TBPX vs. dees in TFPX and TEPX
  - Both faces of TBPX ladders loaded with modules
    → no possibilities for service routing on back-side / access to module
    → Supply current needs to be routed directly from module to module
        → In on one side, out on the other side
    → Current needs to return also from module to module on the module
        → In on one side, out on the other side
  - TFPX and TEPX: current entries and exits module at the same side



Module design in TFPX and TEPX

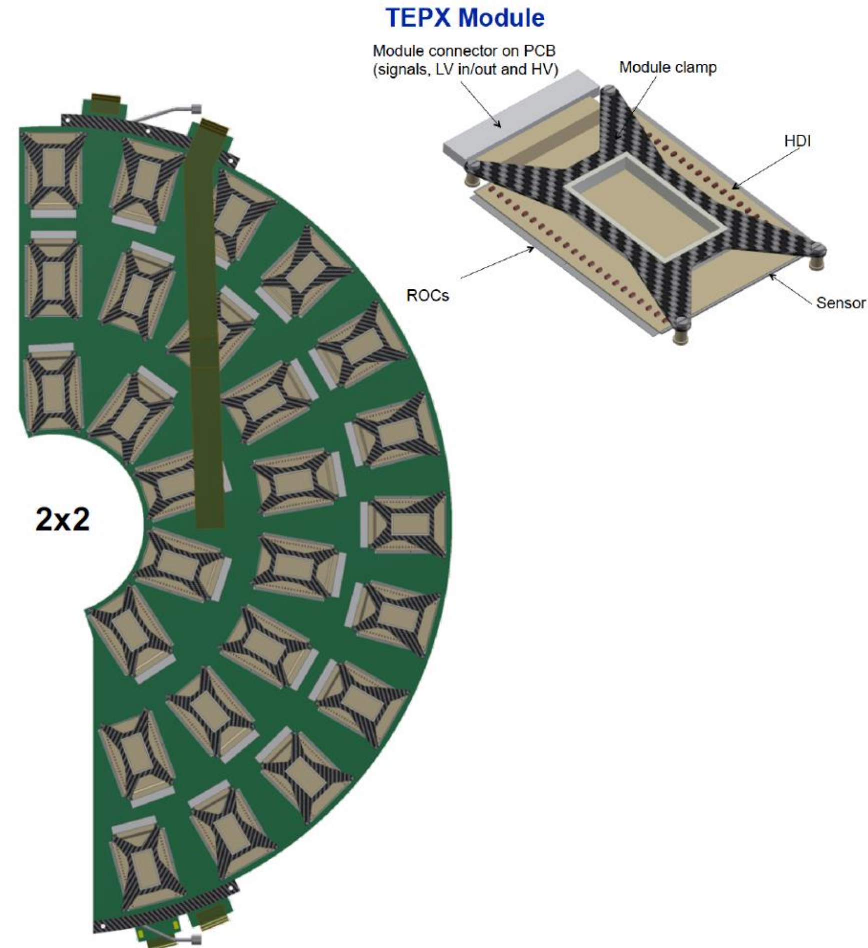
TFPX

- Current routing from module to module under study
  - Aluminium pigtail soldering under investigation
  - Working on definition of a base-line idea

TEPX

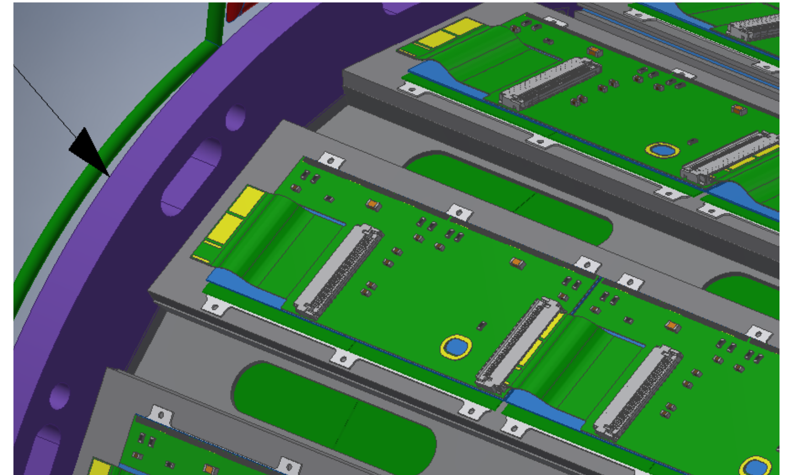
- Investigating large flex-print (or PCB) for supply current routing, HV distribution, and signal routing
- All connections to services via "pigtail" on module HDI which plugs into a connector on the large flex-print

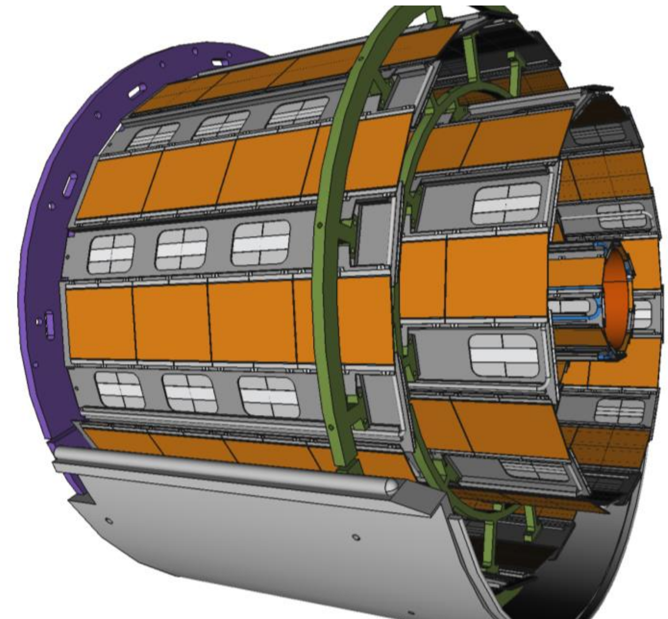
→ HDI prototype to be designed soon (PSI/UZH)



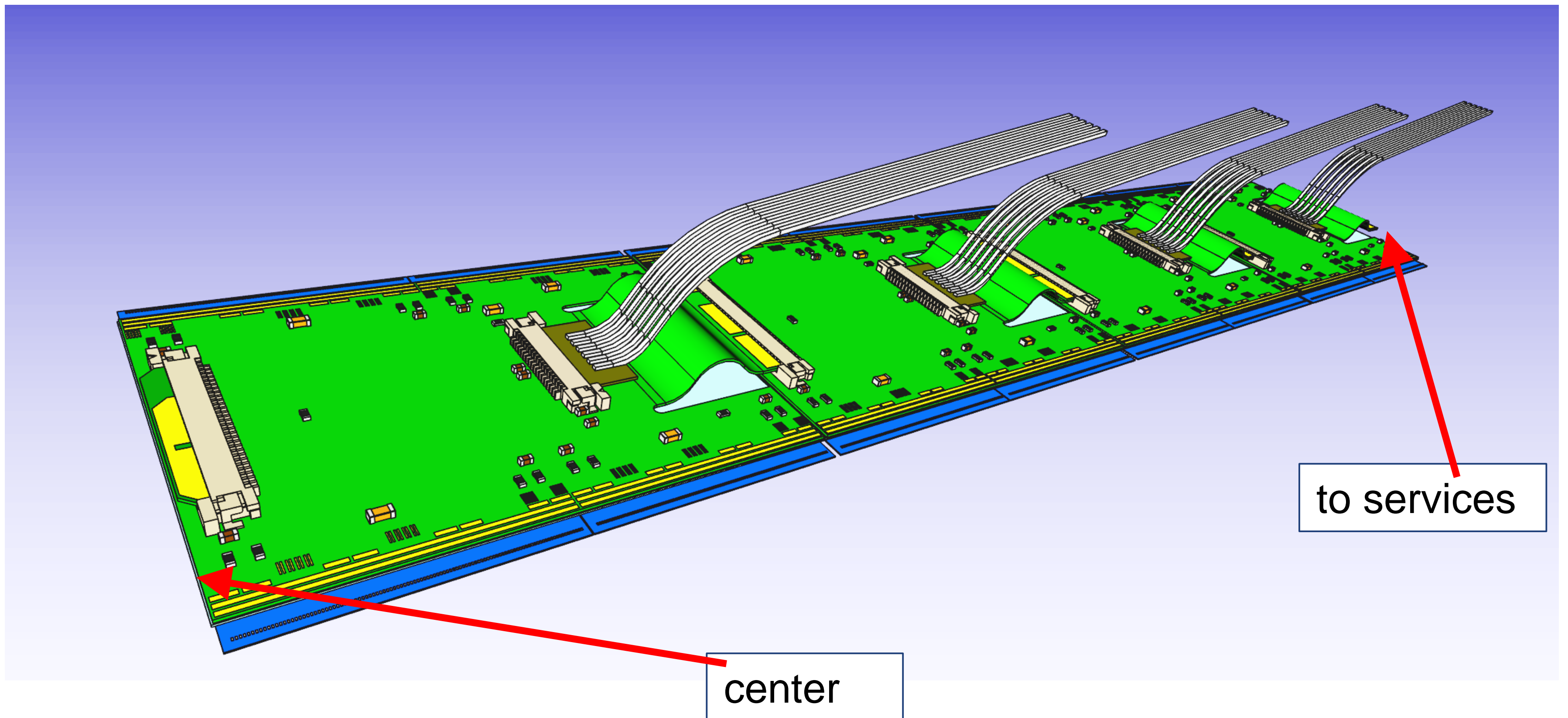
Module design in TBPX

- Both faces loaded with modules
  → no possibilities for service routing on back-side / access to module
- Need to route supply current and return rurent on ladder front-side from module to module
  → challenging connection
  → high current density
  → need one “power-in” and one “power-out” connection on each side of the module
  → signal cable connection independent from power connection
- Keep quick replace/repair option
  → Replacement without damage to structure or neighbouring modules
  → Avoid permanent glueing of modules to support if possible

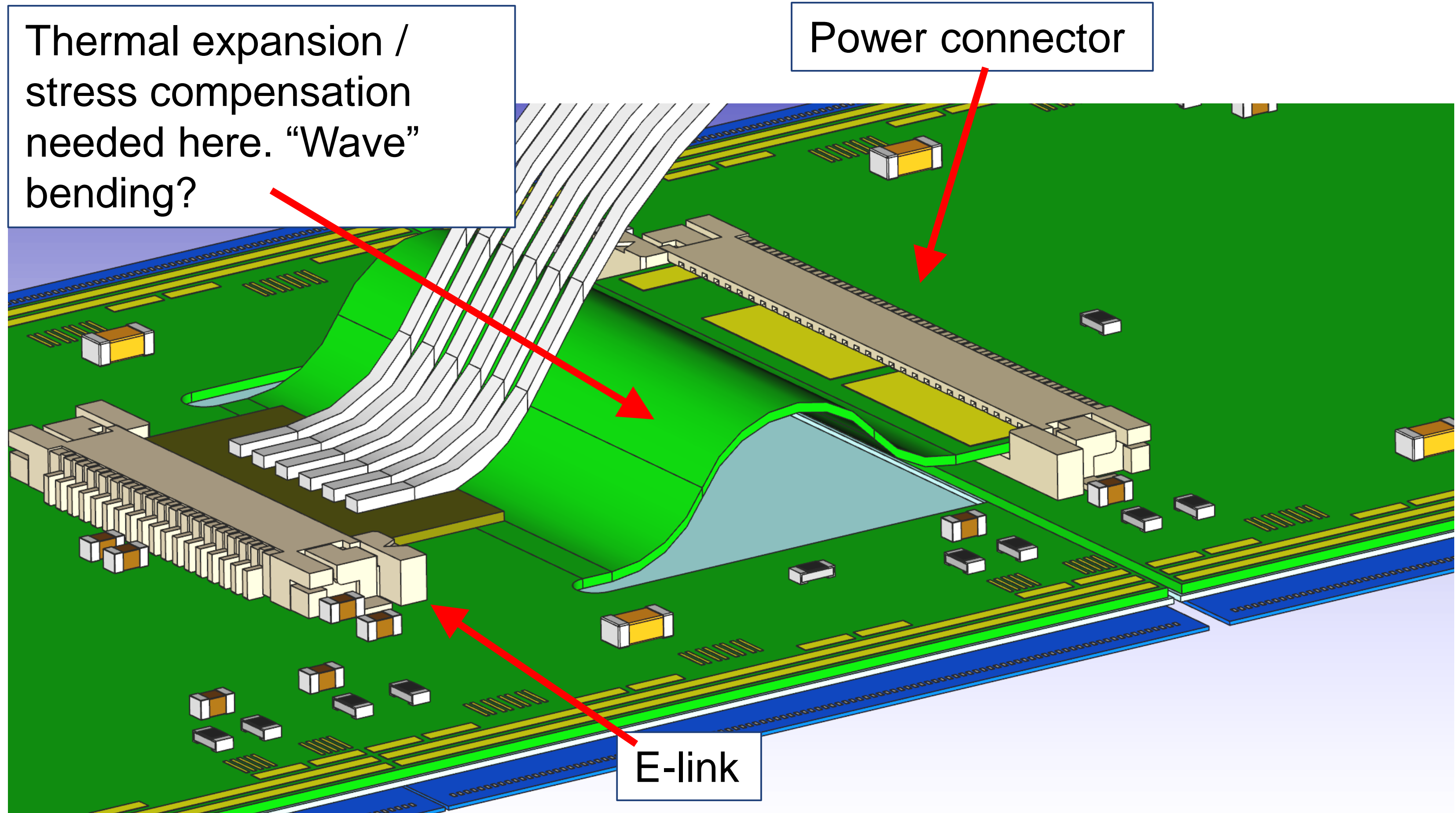




Connection to chains in barrel



Connection to chains in barrel

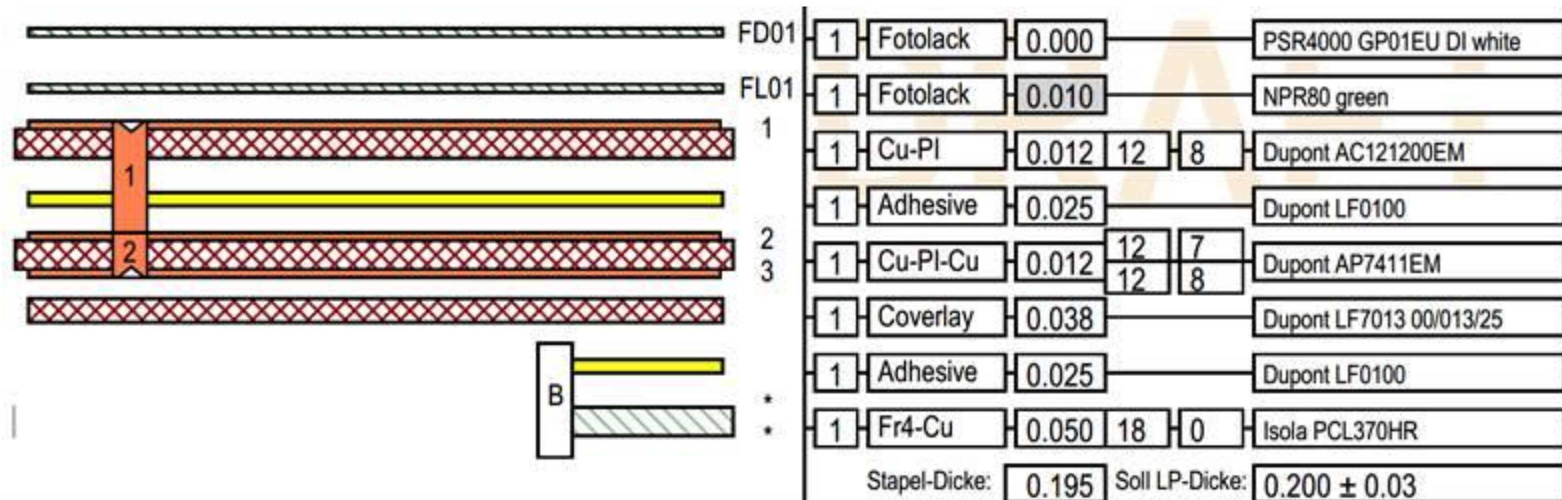


HDI Requirements

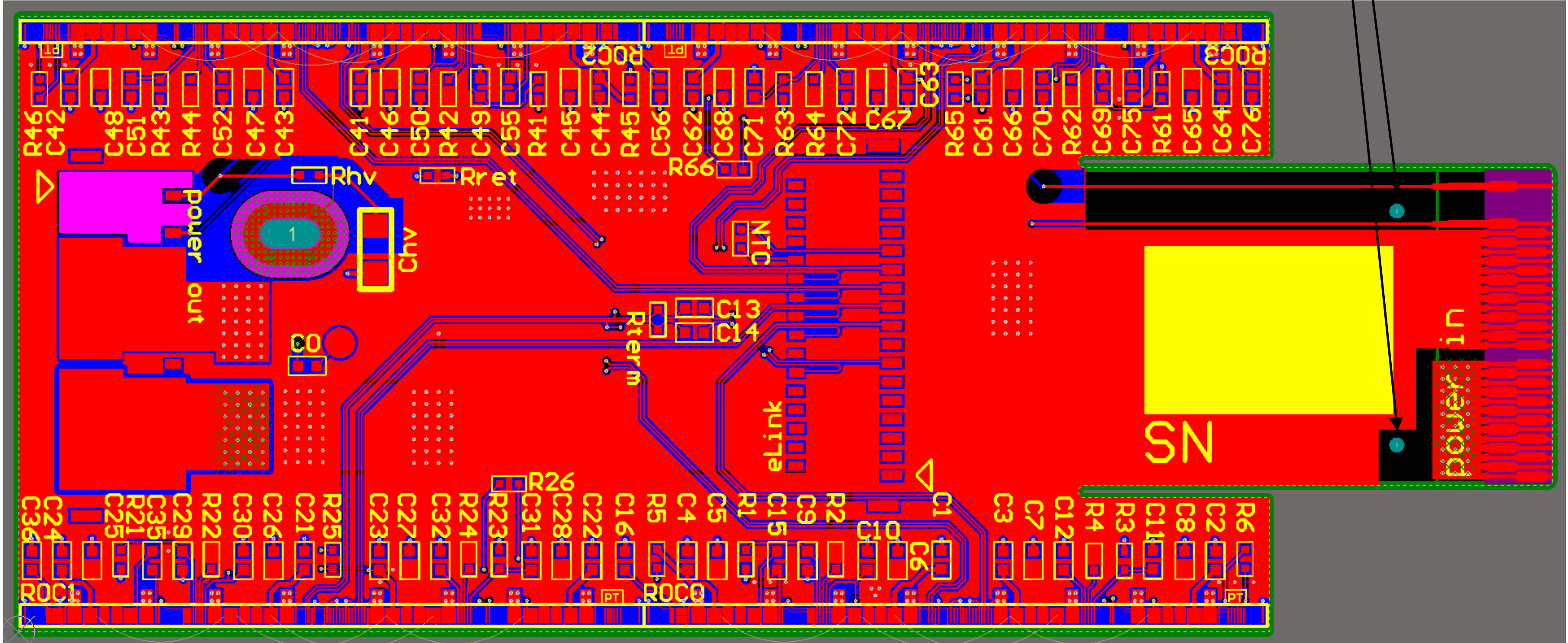
- Clearance driven by wire-bond pad frame
  - Single row, no fanout, >50um wide pads
  - ROC: 100um pitch
  - → Chose 60um wide pads with 40um clearance
    → 10um copper thickness and ENIG/ENEPIG gold-plating possible with larger clearance
- High voltage design
  - More challenging due to distribution from module to module
    → Lines with large clearances etc.
- Supply current distribution
  - Up to 8A in I_{in} and also I_{ret} on final modules, ~1/2 on RD53 modules (on ~1/2 area)
  - Low as possible resistance difference between chips in parallel
  - Need a plane on stable potential for shielding + return current routing on the module (TBPX)
  - → Use Bottom Layer as “local module GND” plane
  - → Use Top Layer as I_{in} plane
  - → Use middle plane for return current routing
- Radiation tolerance
  - Activation
  - Glue delamination
    → To be validated

TBPX HDI layer stack

- Two major challenges:
  - Impedance and DC-resistance of eLink routing
  - Power dissipation in supply current and return current routing (of serial powering chain)
- Use a solid copper plane for return current routing
  → „closest possibility to a GND plane“
  → improved power dissipation of return current
  → crossing of signal lines (down-link) on bottom plane, still solid copper plane shielding the eLinks
- Input current to chips on top layer plane
- Output current (input to next module) on bottom plane

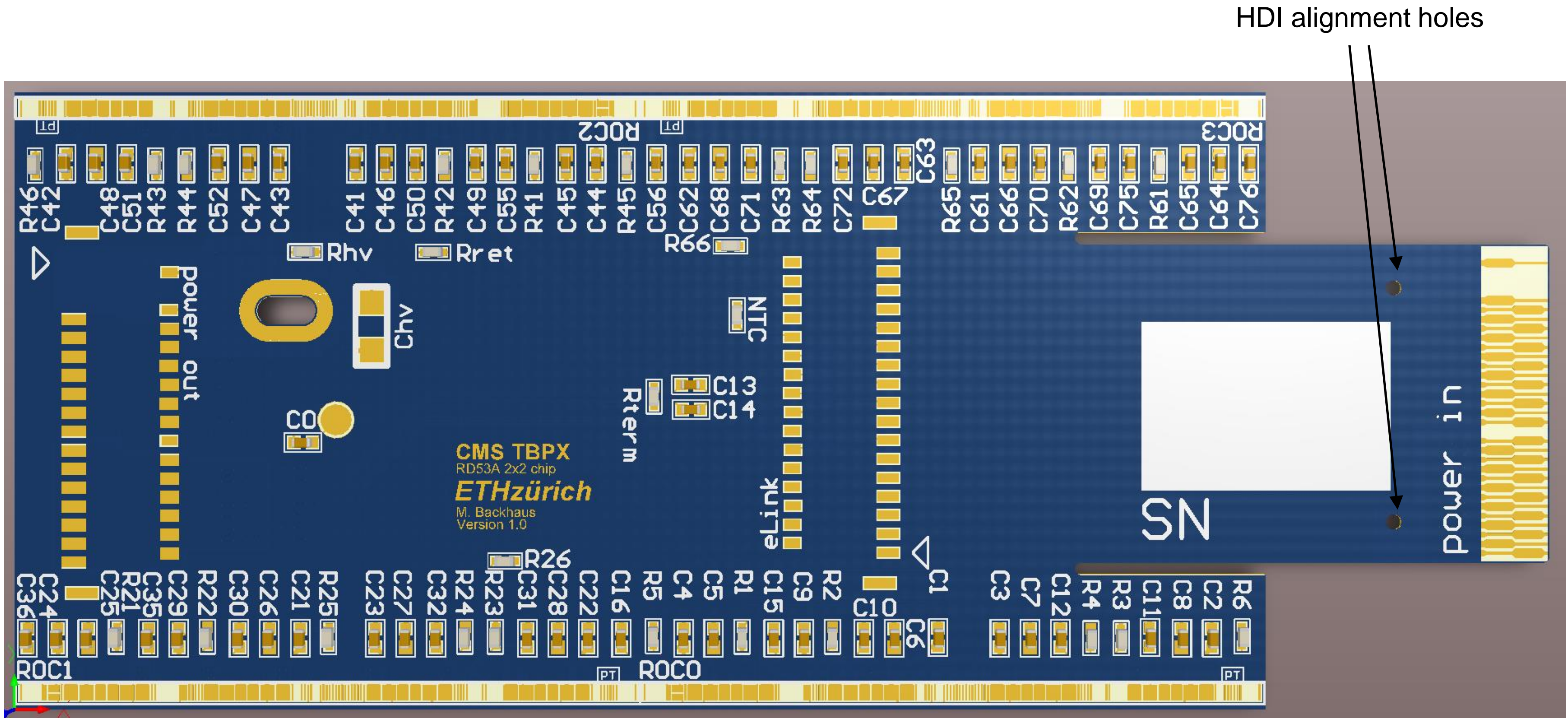


RD53A TBPX HDI design

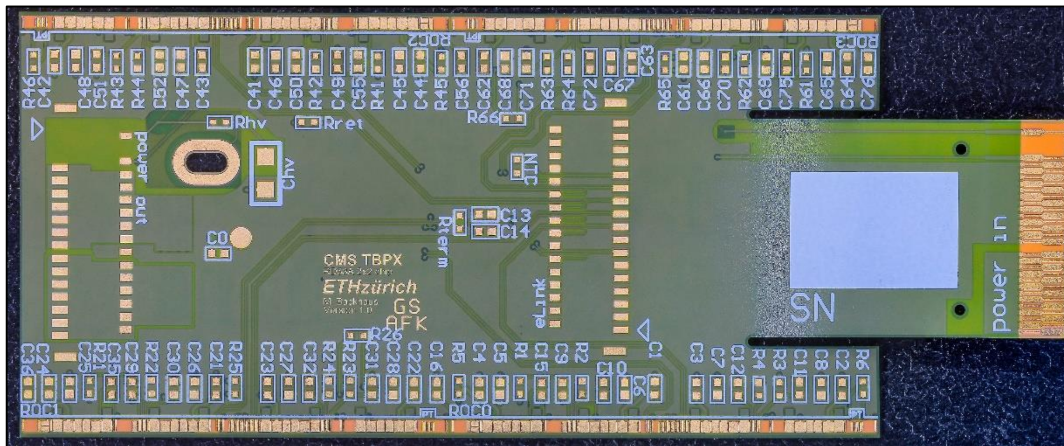


IPA

HDI design



TBPX 2x2 RD52A HDI



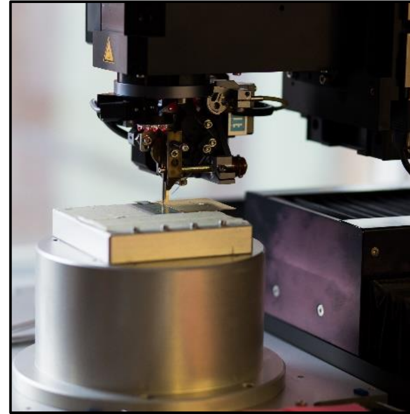
- Received 100 HDI prototypes
- Did optical inspection, good first impression
- Started syst. measurements

Test of HDI before module construction

Tests to be done immediately:
- High voltage - done
- Supply current - now
- Wire bond stregths – this week
- SMD component loading - done
- Accelerated ageing / stress test
- Design validation with Chips
  → digital modules

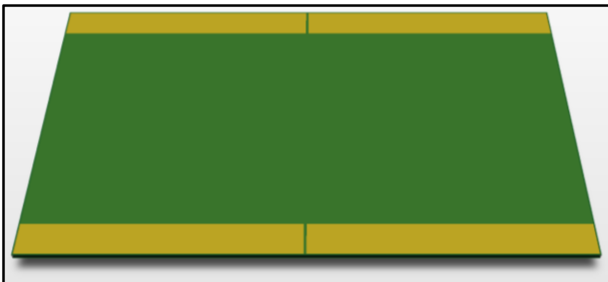
After:
- Wire bond encapsulation
- Flex irradiation → delamination
- SMD component irradiation
- Spark protectionn

HDI wire bond test

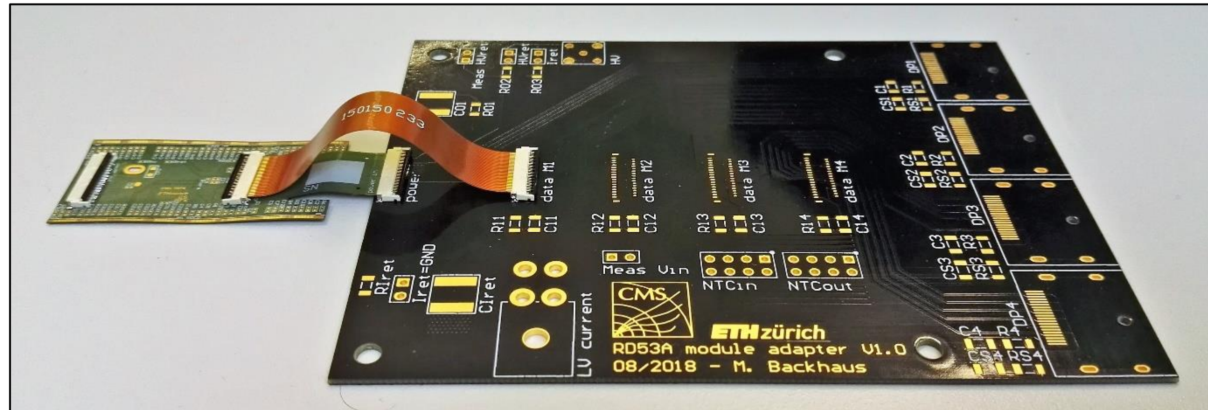


HDI high voltage test

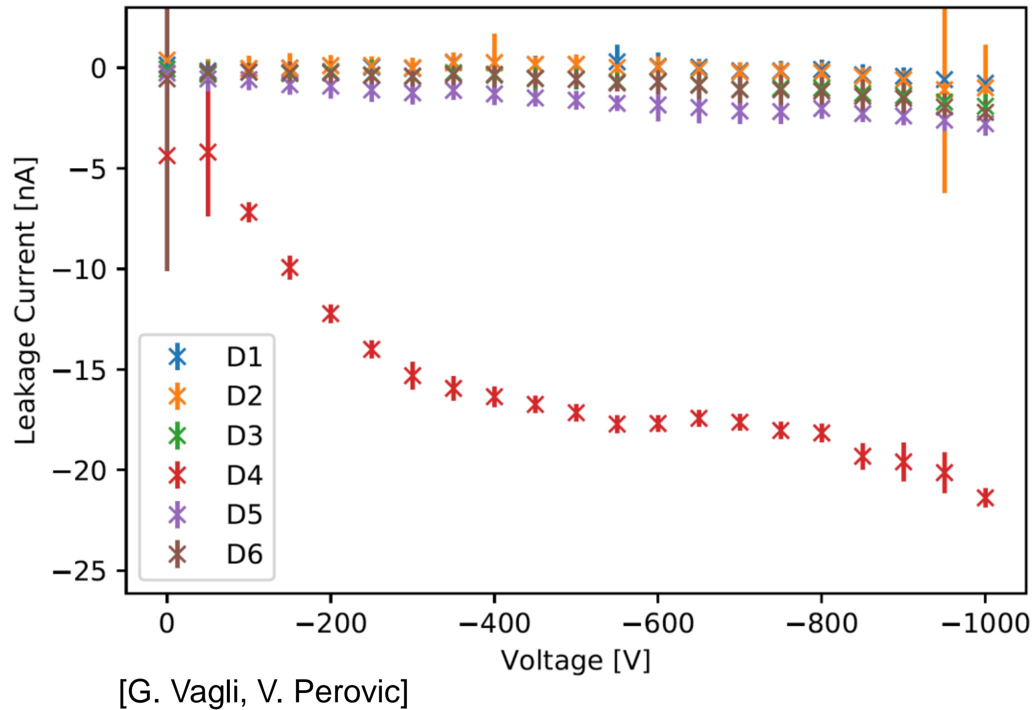
Wire bond test PCB



HDI with adapter PCB



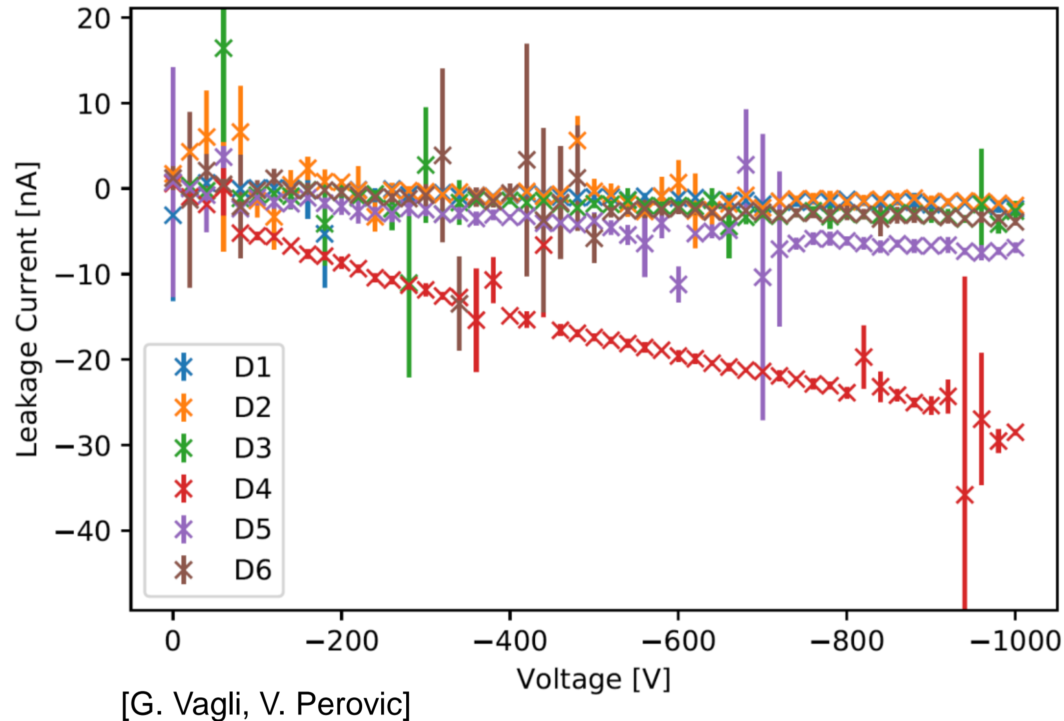
High voltage test: IV curves on bare HDI



[G. Vagli, V. Perovic]

- No problem observed up tp 1kV

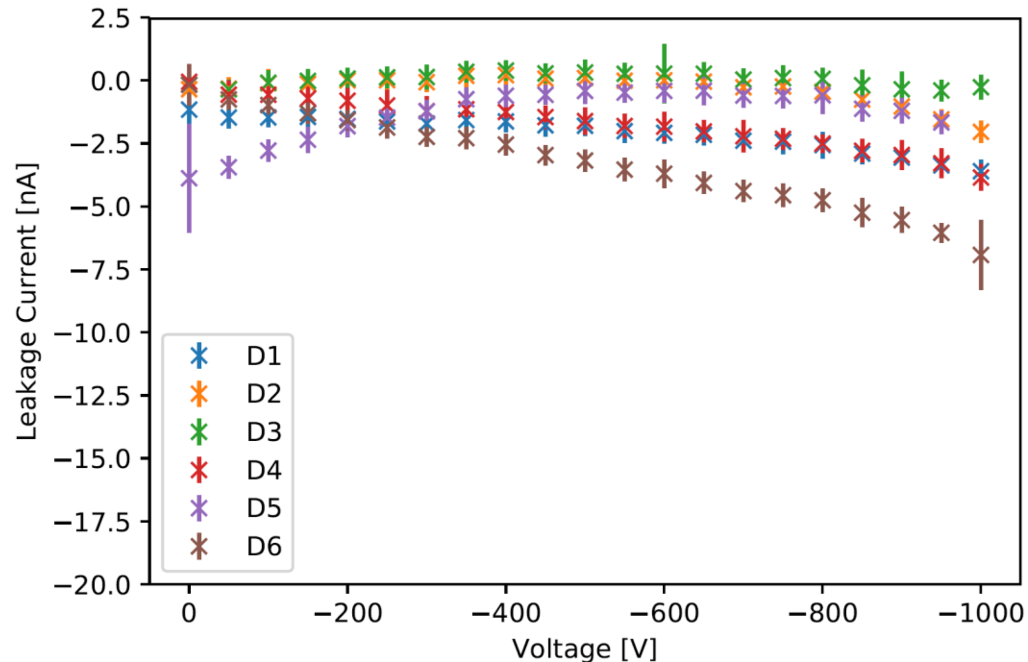
High voltage test: switch on/off on bare HDIs



[G. Vagli, V. Perovic]

- No problem observed up tp 1kV

High voltage test after thermal stress

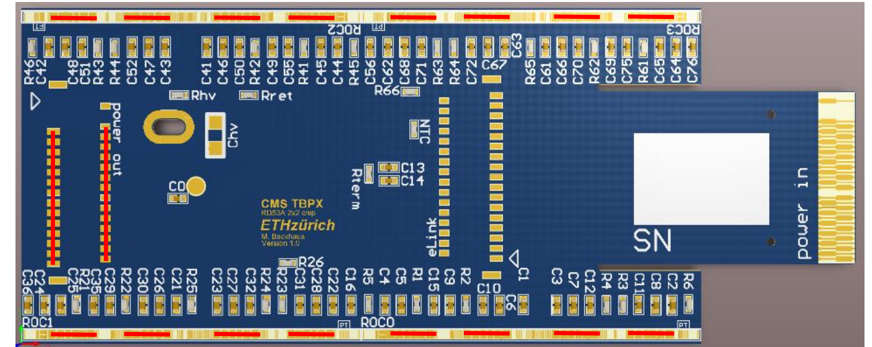


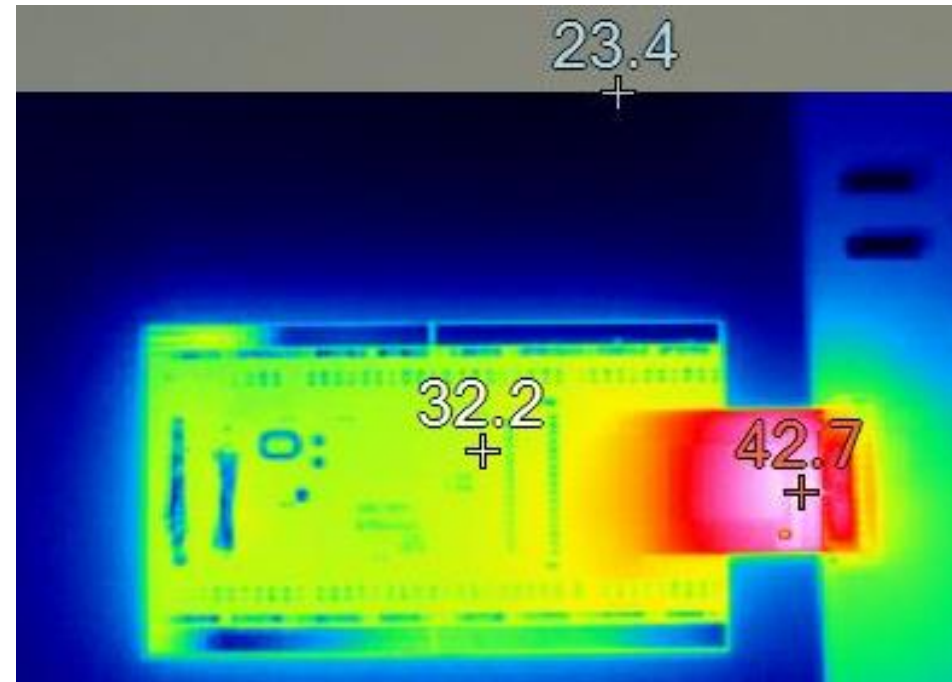
[G. Vagli, V. Perovic]

- No problem observed up tp 1kV
- Outlier sample revovered after thermal stress
  → probably due to humidity baked-out of circuitry

Current distribution and power consumption

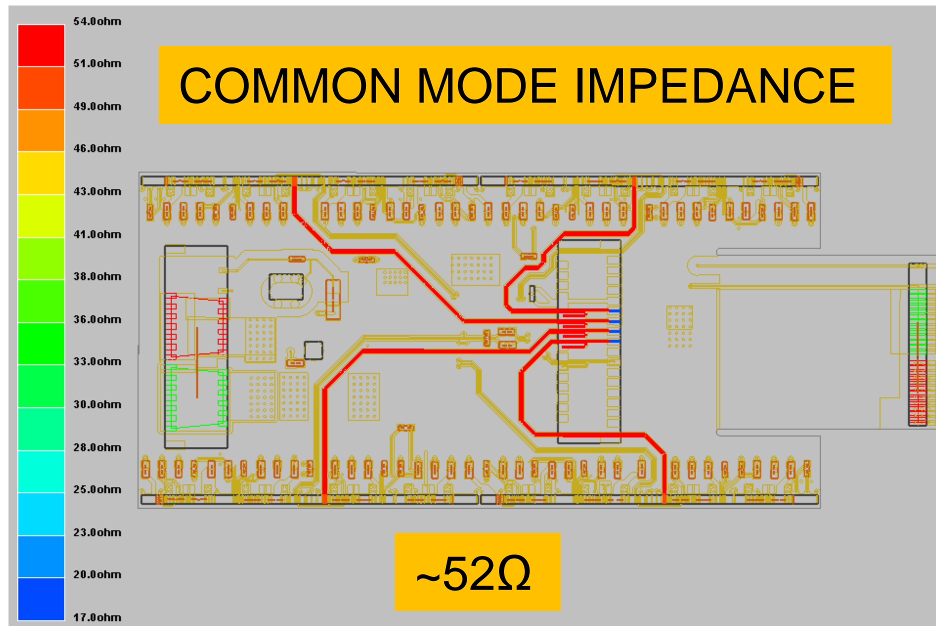
- Shorted “chip in” and chip”out” pads on one HDI sample
- Shorted also power-out connector
- Measure temperature with increasing current pushed through HDI
- $\Delta V_{in\text{-}out}$ = 100 mV
  → power consumption on HDI smaller than ~600 mW
  → see simulations on next slides

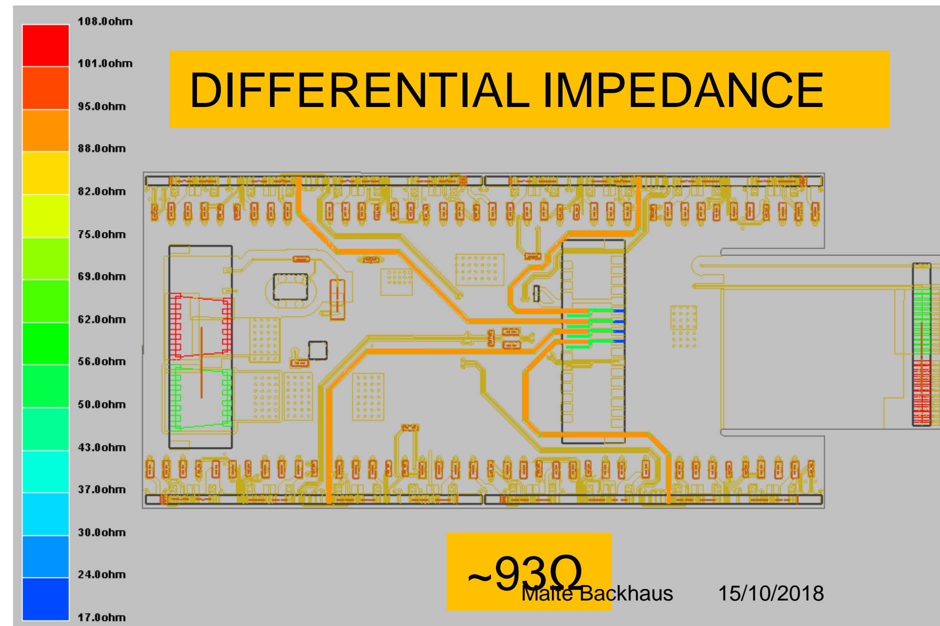




ITAINNOVA HDI simulations

- Software used: Ansys HFSS & SiWave
- Simulation model configuration and results still ongoing
  - High frequency lines impedances (common and differential)
  - Transient response, eye diagram, etc.
  - Traces and planes parasitic elements calculation (R, L, C)
  - Preliminary impedance results seems very similar to theoretical values:



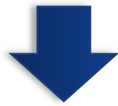


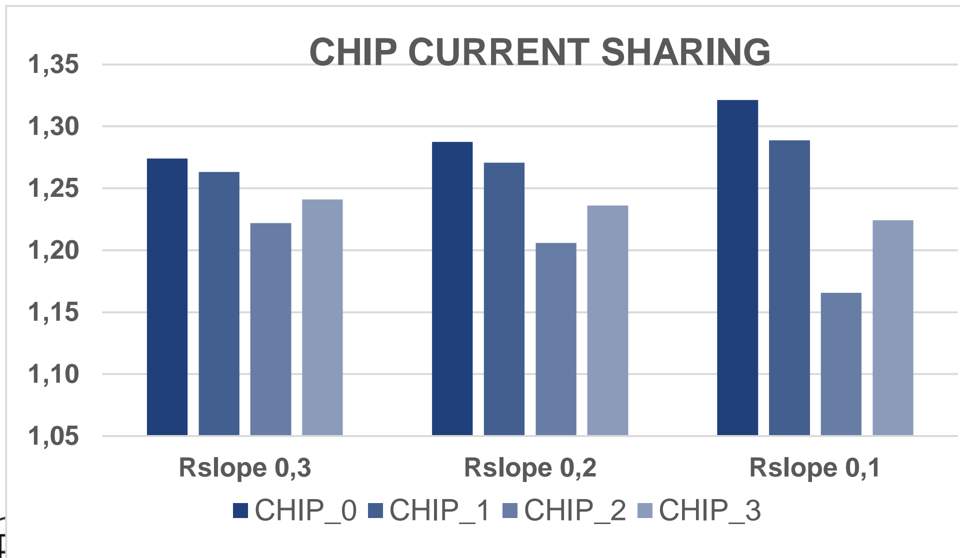
ITAINNOVA HDI simulations

- HDI Current distribution analysis:
  - Hot spots, unbalancings, etc.
- HDI layers power dissipation

- **PRELIMINARY RESULTS FOR I_{in} = 5A**

- **CHIP current sharing depending on SLDO slope configuration I_{in} = 5A**





133 A/mm²

TOP LAYER

P = 200mW

INTERNAL LAYER

P = 150mW

BOTTOM LAYER

P = 250mW

CMS Phase 2
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Introduction to TBPX thermal simulation

- Thermal simulations are performed on TBPX with thermal runaway effect of pixel sensor.
- Special focus on influence of serial powering

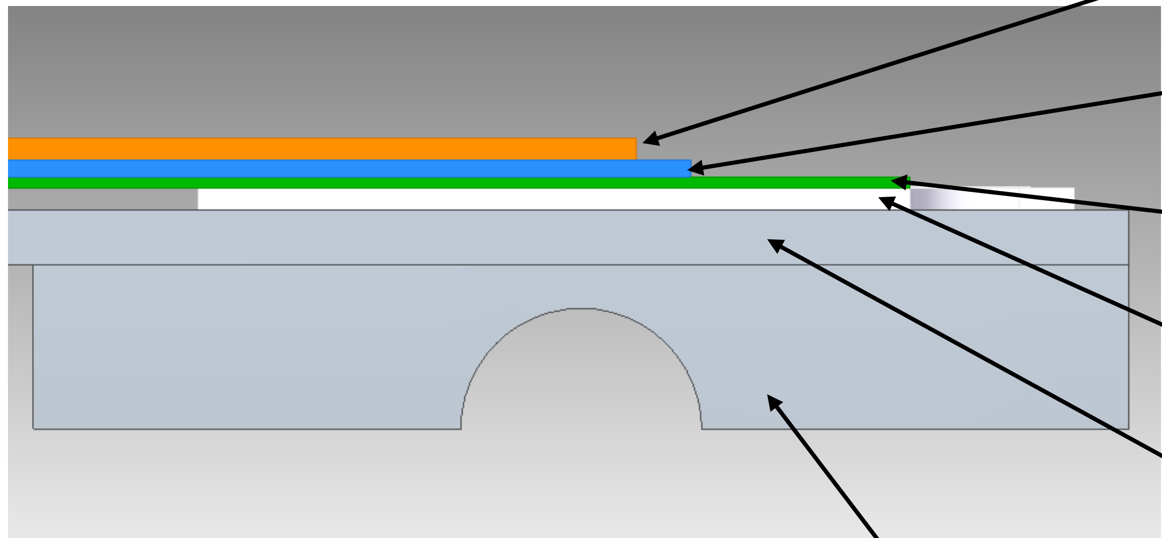
- TBPX Layer 1 is most critical and has been deeply studied to check the requirements.
  The thermal analysis of layer 1 module has been performed with the last geometry and it is complete of:
  - **Power generation of HDI (uniformly distributed)**
  - **Power generation of ROCs with nominal case**
  - **Power generation of ROCs with chip failure cases**
  - **Thermal Runaway of pixel sensor**

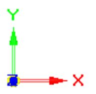
- Further sensitivity analysis on the interfaces have been performed on Layer 1 to explore possible solutions to improve the margin from the thermal runaway of the module.

- Layer 2, 3, and 4 do not show particular issues. Concentrate on TBPX Layer one here

15/10/2018

Thermal conductivities





HDI – 200 µm - Kapton
λ = 0.3 W/mK

Pixel Sensor – 150 µm – Silicon
λ = 148 W/mK

PROC – 100 µm - Silicon
λ = 148 W/mK

Module rails – 200 µm - Alumina nitride
λ = 200 W/mK

High conductivity carbon fiber – 0.5 mm λ_{xz} = 250 W/mK - λ_y = 1.5 W/mK

Housing pipe

- TPG – λ_{xz} = 1000 W/mK - λ_y = 6 W/mK
- Aluminum carbon fiber - λ_{xz} = 230 W/mK - λ_y = 120 W/mK

Interfaces

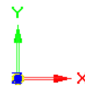
- **Epoxy glue** – 50 µm
  λ = 0.5 W/mK
- **Thermal grease** - 50 µm
  λ = 6 W/mK

Thermal grease – 100 µm
λ = 6 W/mK

High conductivity glue – 50 µm
λ = 3 W/mK

High conductivity glue – 150 µm
λ = 3 W/mK

Pipe – Stainless steel
O.D. 1.8 mm - I.D. 1.6 mm
λ = 15 W/mK



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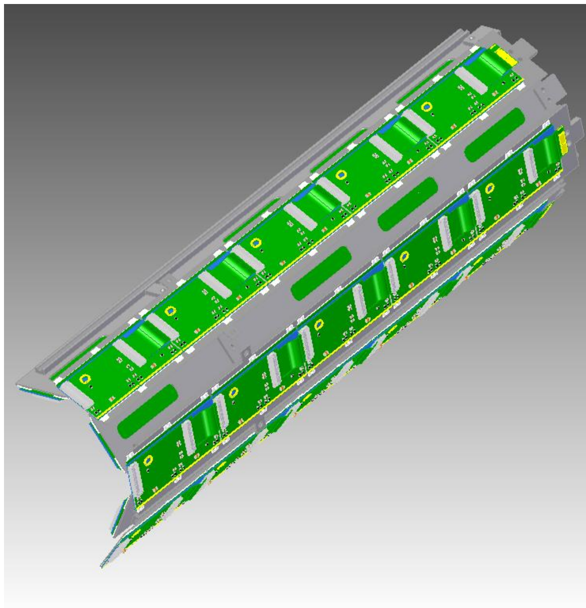
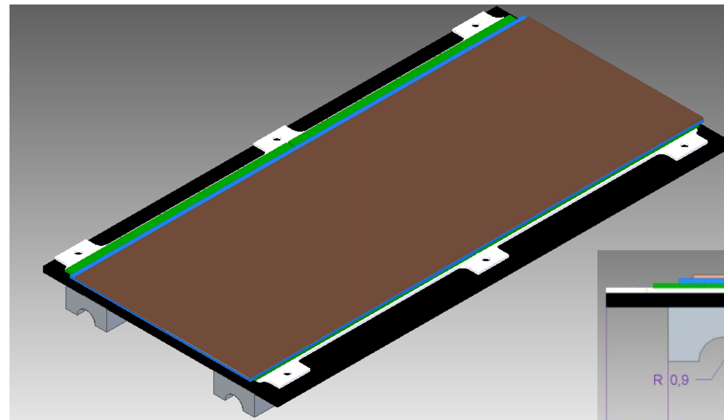
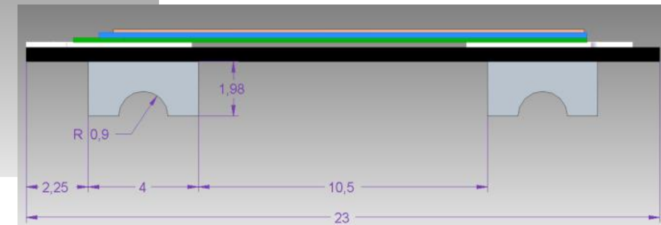
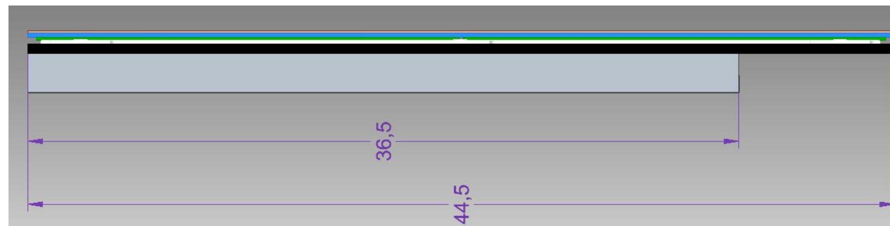
Geometric models - Layer 1









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Layer 1 results – Nominal case
Total luminosity

Conditions inside cooling pipe (CO_2):

Heat transfer coefficient – 7,000 W/m²K

T_{co2} – variable to explore the thermal runaway

HDI
0.570 Watt uniformly distributed

Pixel sensor – Thermal runaway

$$P(T)_{sensor} \propto P_0 \frac{T^2}{T_0^2} exp\left[-\frac{\Delta E}{2k_b}\left(\frac{1}{T}-\frac{1}{T_0}\right)\right]$$

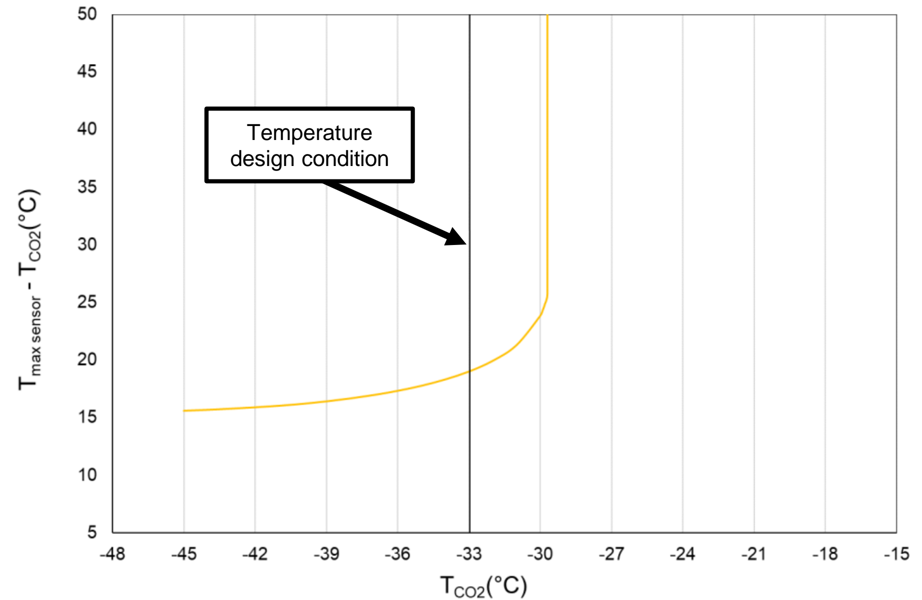
$P_0 = 1.101$ W
$T_0 = -20$ °C

ROCs
Nominal case, both chips

Array – 1.44 W

Edge – 1.36 W

Total – 2.80 W



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Layer 1 results – Chip failure cases
Total luminosity

Conditions inside cooling pipe (CO_2):

Heat transfer coefficient – 7,000 W/m^{2}K

T_{co2} – variable to explore the thermal runaway

HDI

0.570 Watt uniformly distributed

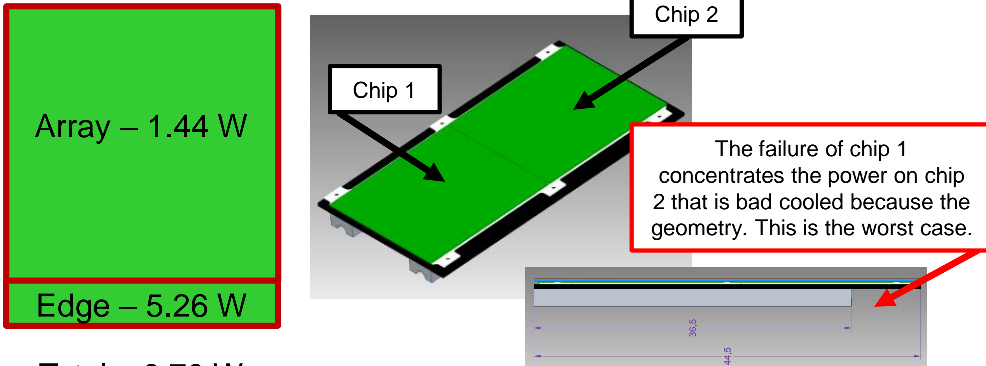
Pixel sensor – Thermal runaway

$$P(T)_{sensor} \propto P_0 \frac{T^2}{T_0^2} exp\left[-\frac{\Delta E}{2k_b}\left(\frac{1}{T}-\frac{1}{T_0}\right)\right]$$

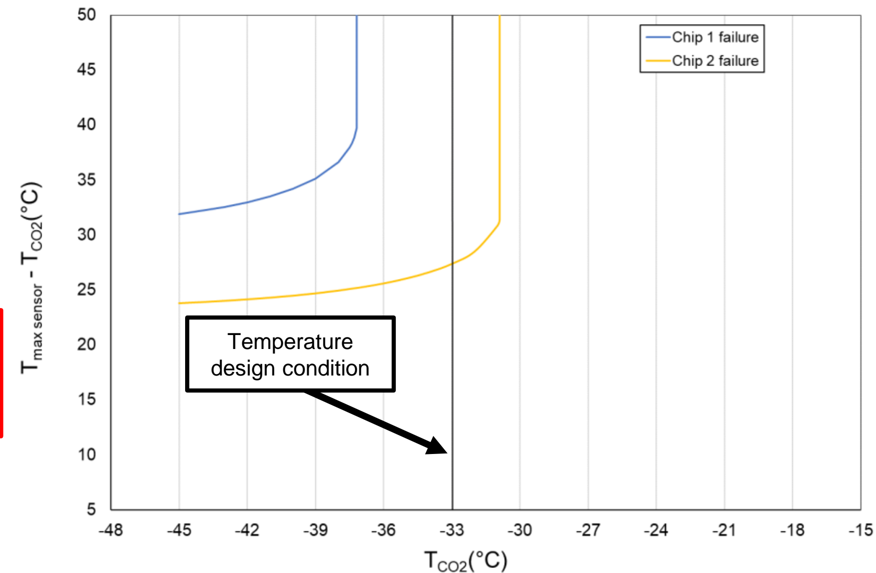
P_0 = 1.101 W
T_0 = -20 °C

ROCs

The failing Chip is without power and working chip has the power distributed as shown in the scheme.

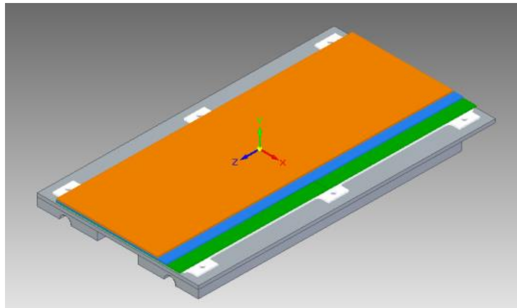


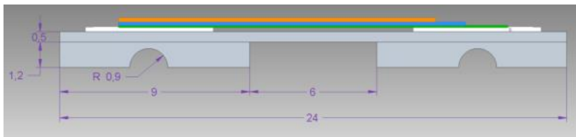
Total – 6.70 W

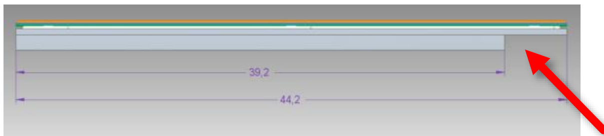


Layer 2, 3/4 results – Geometrical model

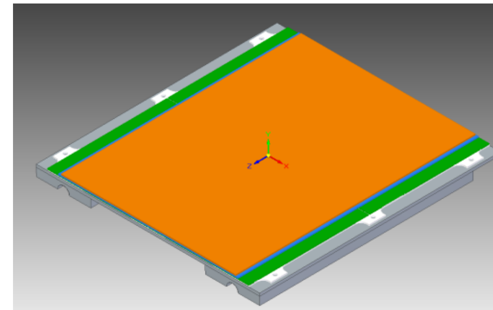
Layer 2

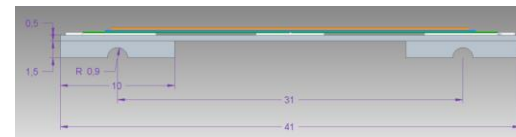


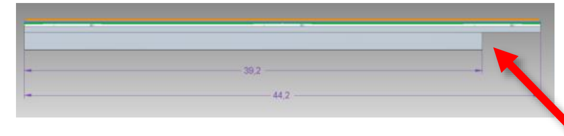




Layer 3/4







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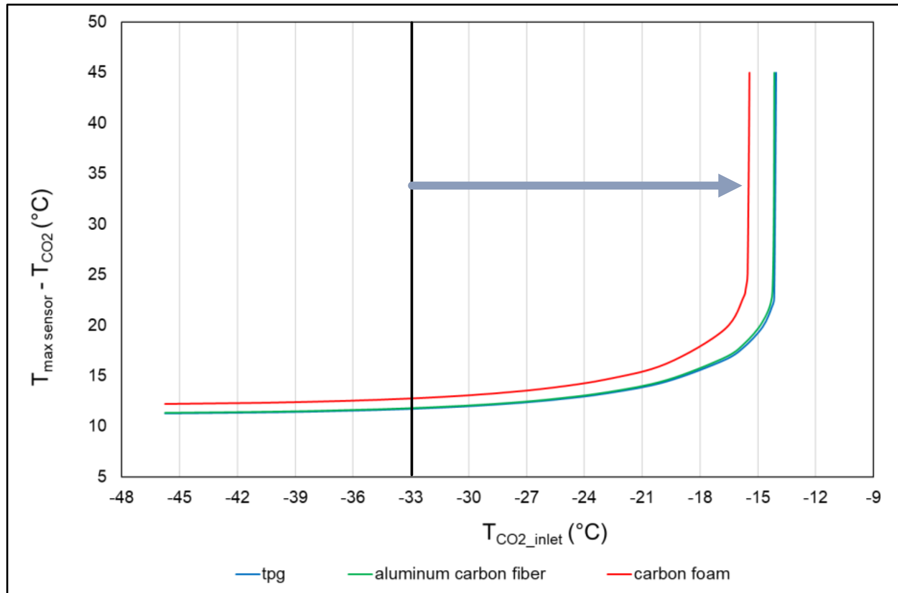
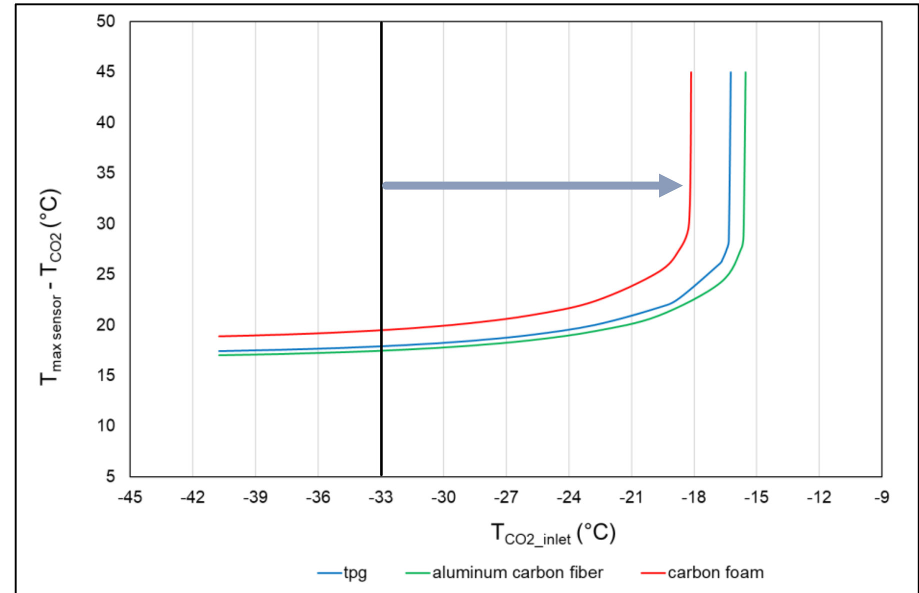
Layer 2, 3/4 results – Nominal case
Total luminosity

First simulations performed on old geometry. No power generation of HDI.
Anyway the margin between design temperature and thermal runaway is very wide.



Layer 2



Layer 3/4

15/10/2018 30

Summary

- Different geometrical constraints in disc and ladder structures
  → dedicated module connectivity for TBPX, TEPX, and TFPX
- Started HDI and module prototyping with focus on TBPX
  - Prototype for 2x2 RD53A modules in hand and under test
    → First results very promising, operation with chips planned for this week
  - HDI layout simulated, comparison with measurements started
- Performing thermal simulations including SP related issues, esp.
  - HDI power consumption
  - Variety of chip failure modes (increase of module power consumption)

  → TBPX L2-4 with good margin to thermal runaway, also in failure modes.
  Simulations with more details planned
  → Hot spots on HDI etc.

  → TBPX Layer 1 (most demanding) ok in normal operation and in most failure modes

  → In worst case failure scenario on TBPX Layer 1 further improvements are needed
  → Sensitivity analyzis for optimization of interfaces started, improvements are possible.