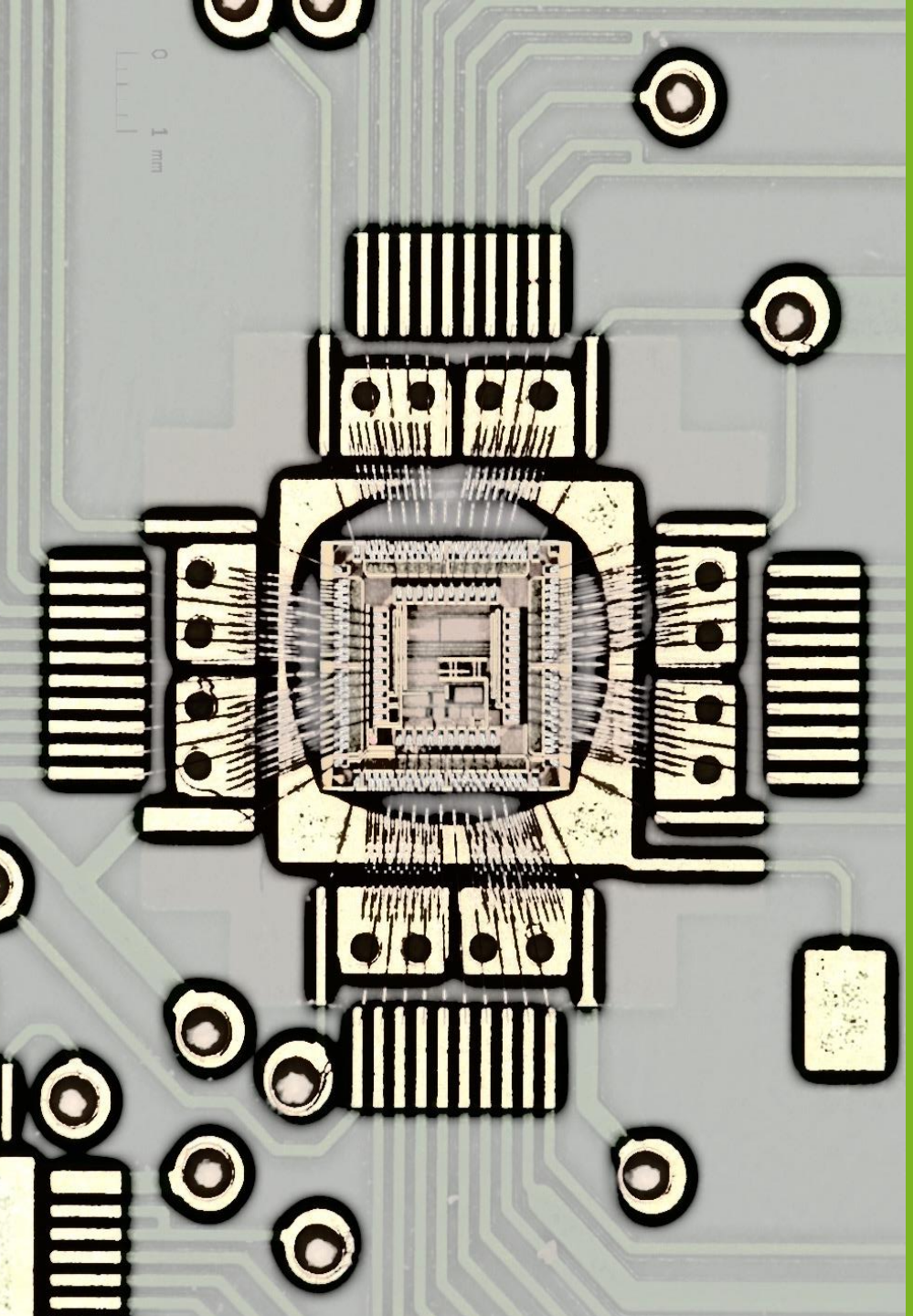


Status of PSPP

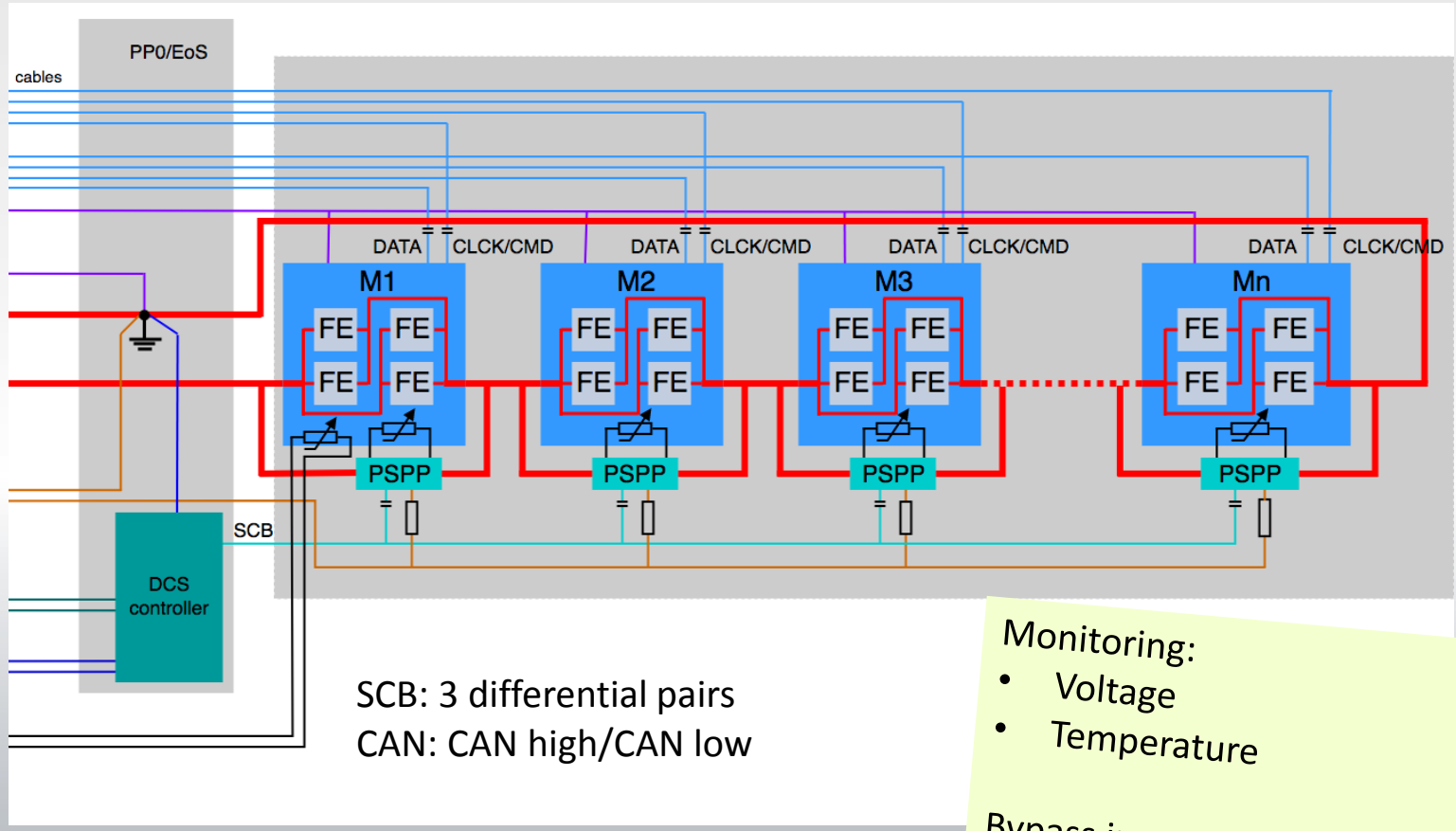
Susanne Kersten

on behalf of the DCS group

October 15, 2018

BERGISCHE
UNIVERSITÄT
WUPPERTAL

DCS concept for ATLAS Pixel: independent monitoring and control by PSPP



SCB: 3 differential pairs
CAN: CAN high/CAN low

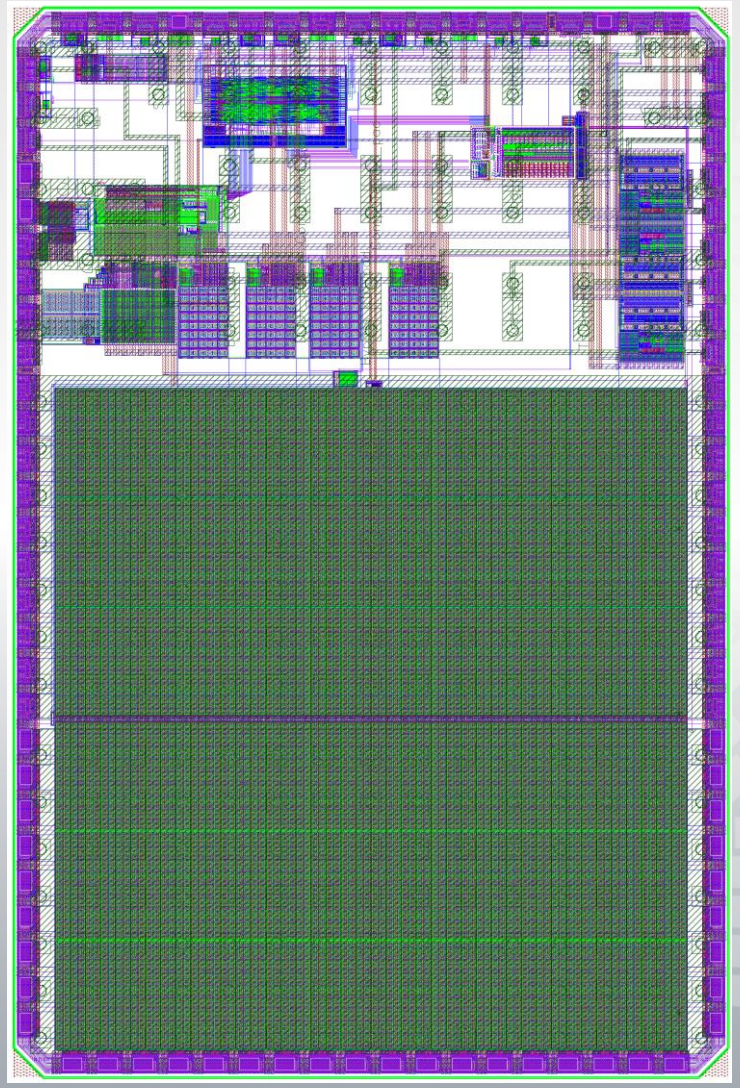
Monitoring:
- Voltage
- Temperature

Bypass in case of
- malfunctioning module
- Broken connection to module

PSPP (**P**ixel **S**erial **P**owering and **P**rotection chip)

contact: N. Lehmann

- Shunt Regulator
- Regulated voltages:
  - Vin, Vbg, Vref, VDDA, VDDD
- Logic protected by TMR
- SCB (Serial Control Bus) interface
- Power-on reset
- 2 Comparators for module interlock
  - can be deactivated
- Bypass transistor (2x 105 bumps)
  - 8A
  - automatically or
  - by command
- 10 bit ADC
  - Supports 2 NTC

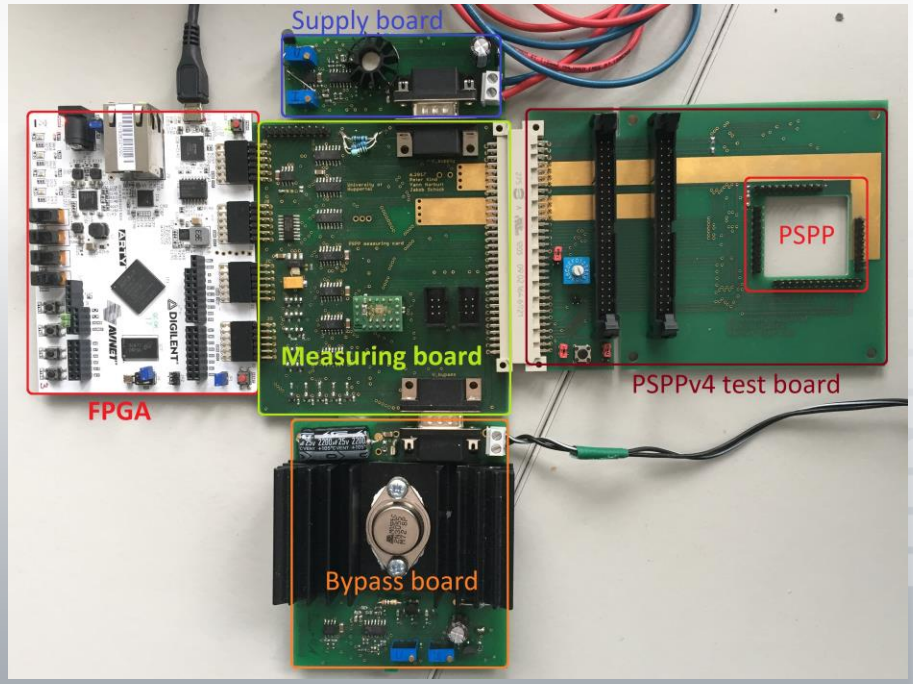


Status PSPPV4

- 130 nm GF
- Size: (3 x 4.5) mm^2
- Submitted November 2017, last MPW
- Delivered on September 17, 2018
  - ‘normal’ delivery July
  - Bump bonds caused additional delay
- We got only 40 pieces
- Sent to IZM for flip chipping
  - A few PSPP will be placed on PCB
  - ca 25 PSPP to be mounted on flex

- Test setups prepared
  - Initial test
  - **Stress test** @ IZM, mounted on flex
  - X-ray at Cern

- **Irradiation at PSI: 100 MeV protons**
- PSPPV4
- PARC chip SEU tests
  - 500 bit + 500 bit TMR shiftregisters

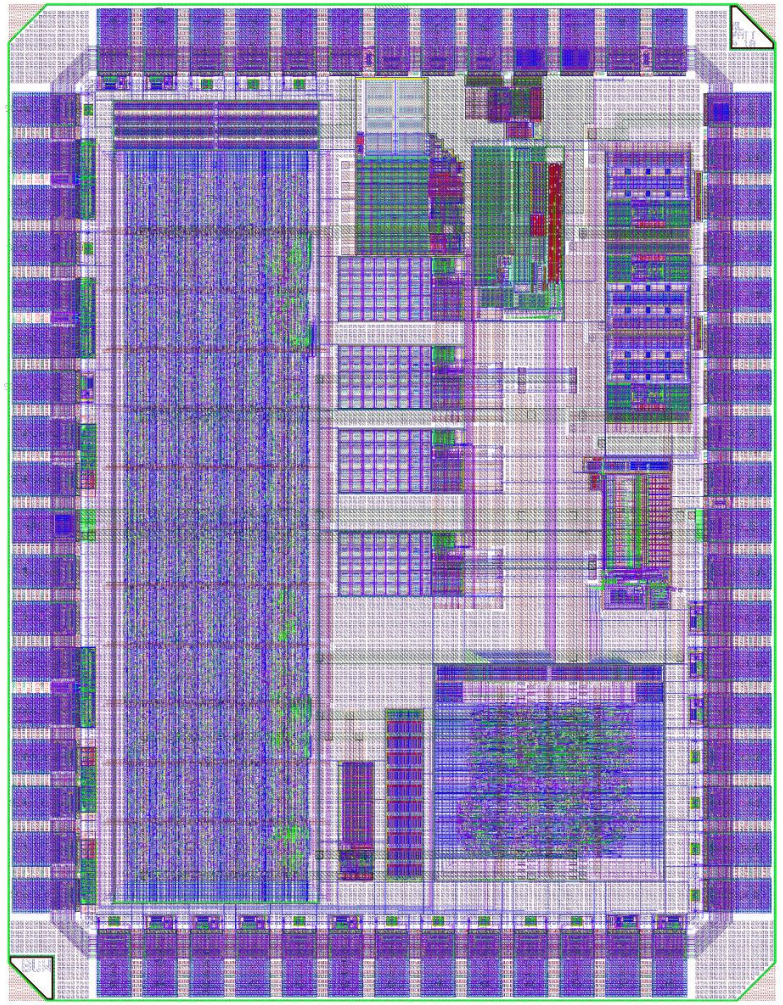


PSPP Asynchronous TMR Test (PATT)

- Offer to join ITKSTAR submission
  - thanks to strip community
- 130 nm GF

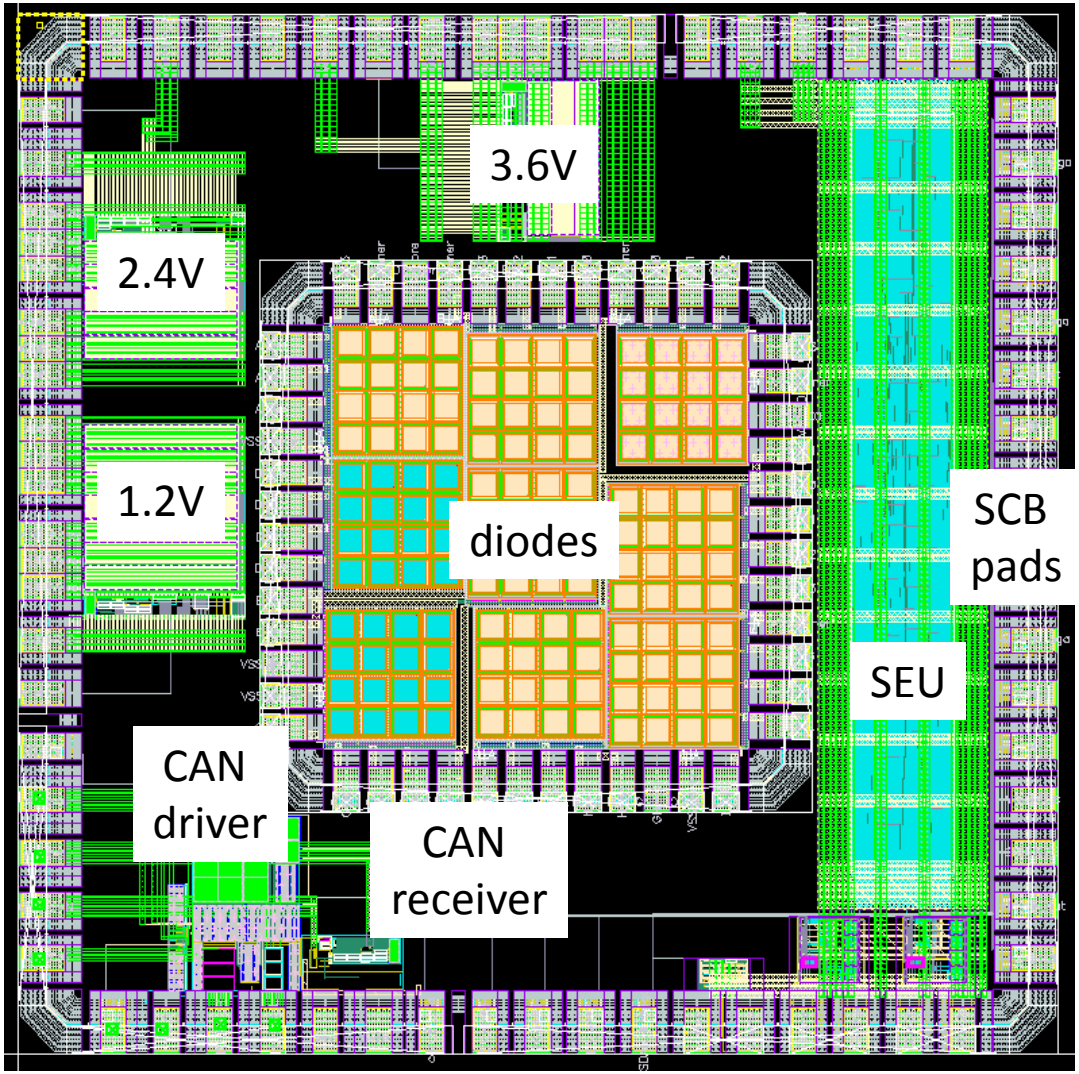
- Same components as PSPP besides
  - No bypass
  - **Asynchronous TMR**
    - TMR if clock is lost
  - Differential pads
  - SEU test logic

- Released to manufacturing in August
- Expect first diced parts end of November



Fachhochschule Dortmund
University of Applied Sciences and Arts

Test Chip with components for DCS Controller



- **Michael Karagounis, FH Dortmund**
  Alexander Walsemann
  Tobias Fröse, Semih Yilmaz
- Rizwan Ahmad, Wuppertal
  Niklaus Lehmann

- Voltage regulators (1.2V, 2.4V, 3.6V)
- CAN driver
- CAN receiver
- SCB driver/receiver
  - Single ended
  - Differential pads
- Digital SEU test structures
- Diode test structures

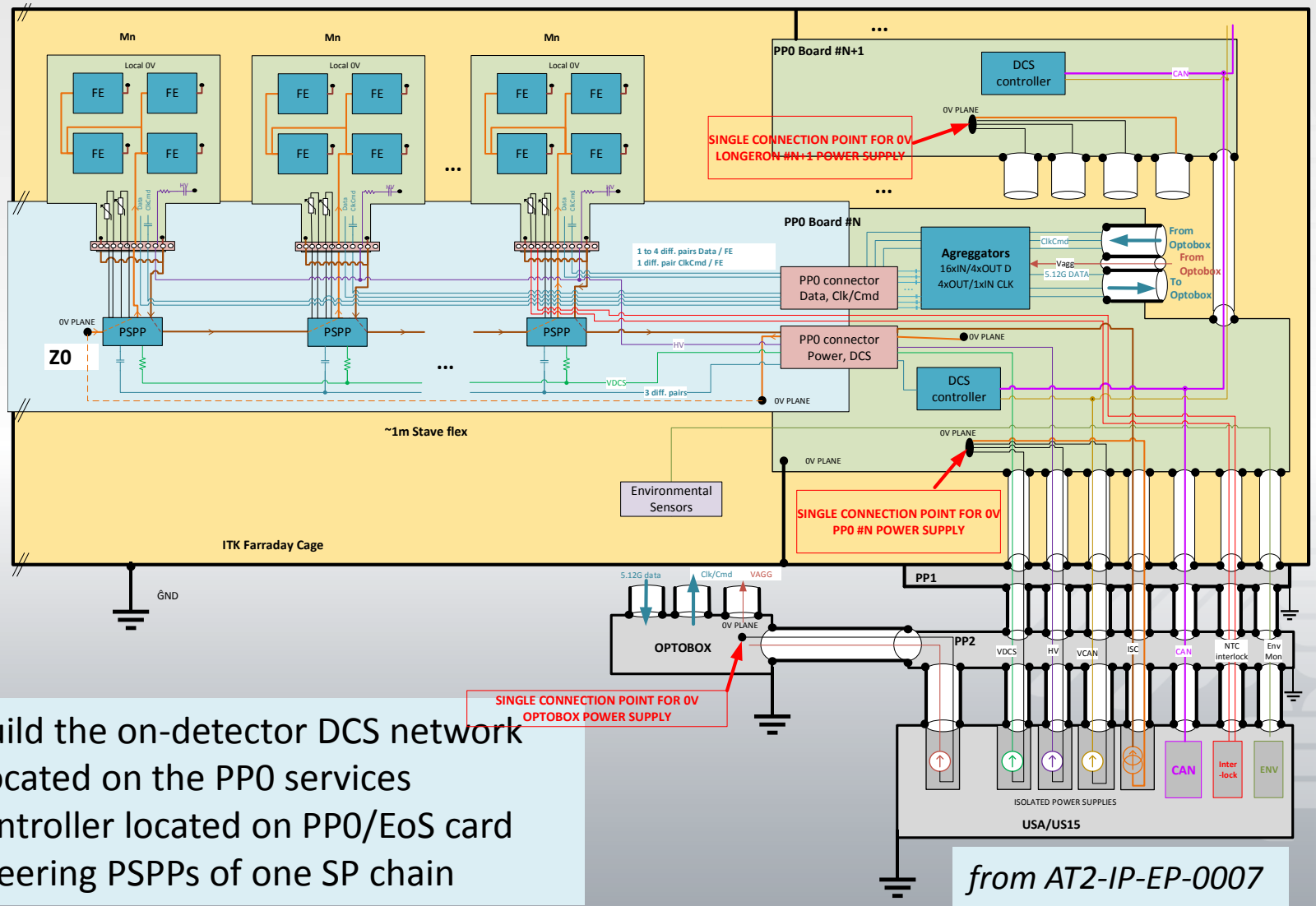
- submitted at 22th of Aug 2018
- 2mm x 2mm in TSMC 65 nm
- Expected in November

Documentation

- Manual of PSPPv3 and PARC:
  - https://twiki.cern.ch/twiki/pub/Atlas/DcsChip/PSPPv3_Manual.pdf
- Manual of PSPPv4 and PATT:
  - https://twiki.cern.ch/twiki/pub/Atlas/DcsChip/PSPPv4_Manual.pdf
- Specification documents in EDMS:
  - ATU-SYS_ES_0031 PSPP
  - AT2-IP-ES-0001 DCS controller

Backup slides

Introduction

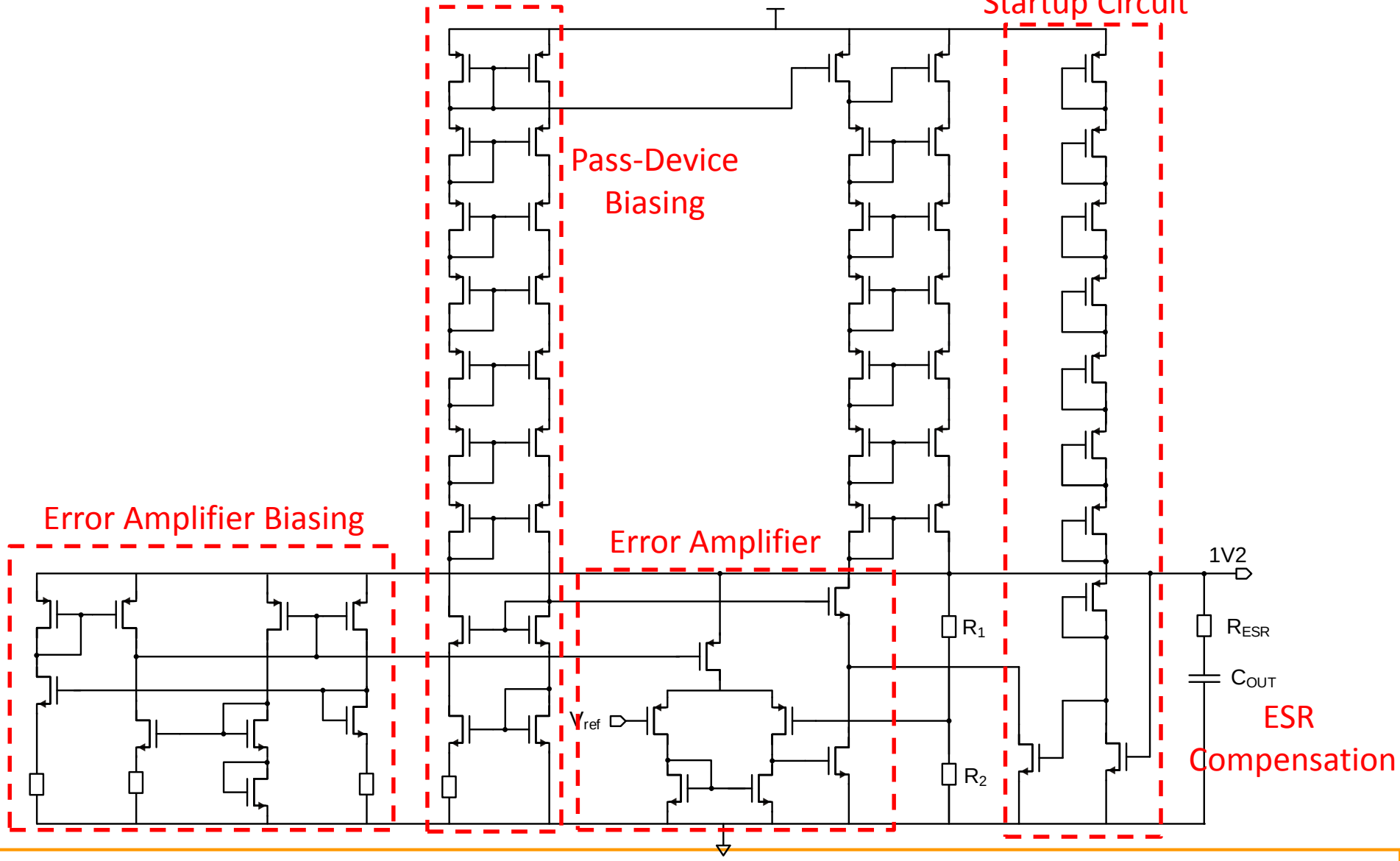


2 ASICS build the on-detector DCS network

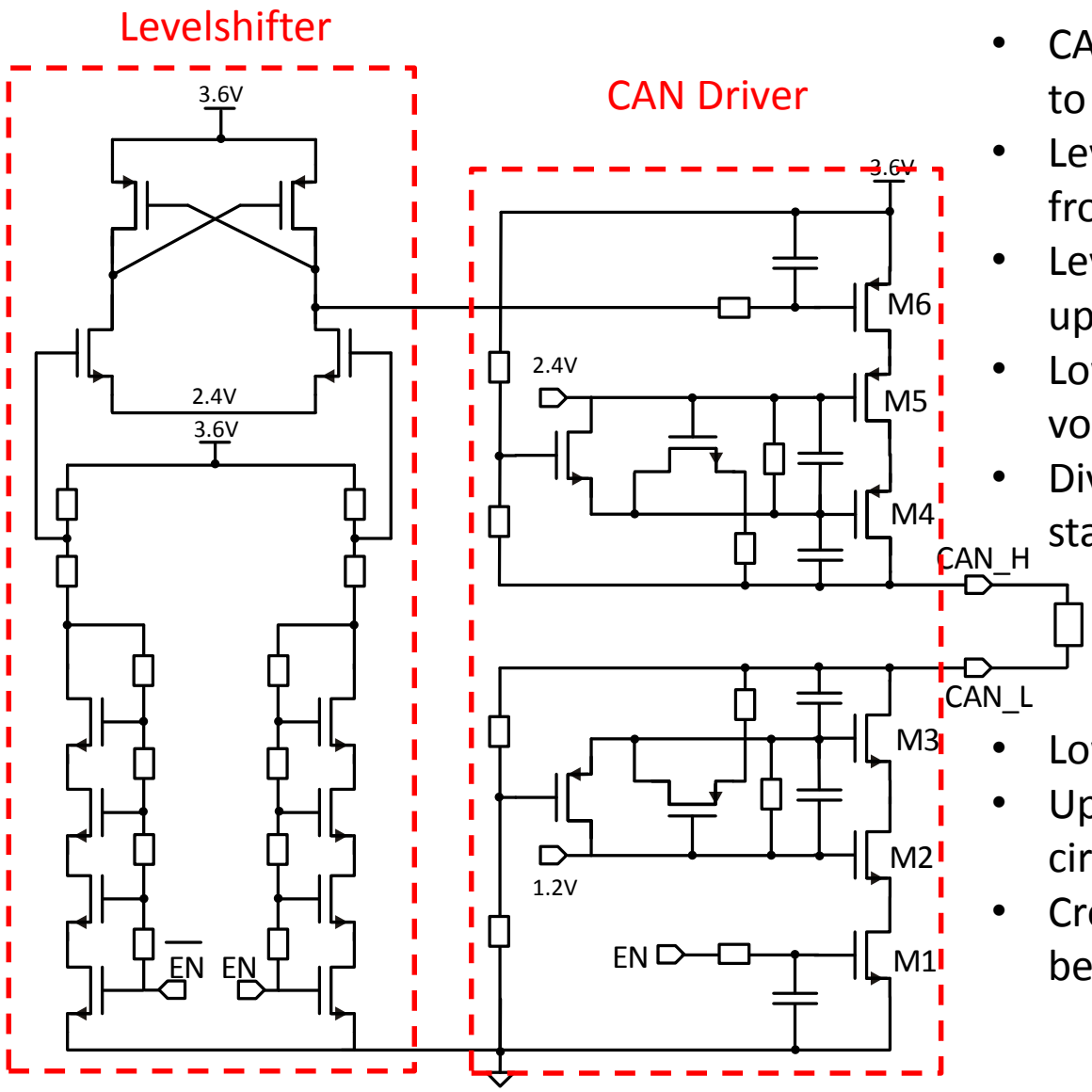
- PSPP located on the PP0 services
- DCS controller located on PP0/EoS card
  - Steering PSPPs of one SP chain

from AT2-IP-EP-0007

Complete 1V2 Regulator Circuit



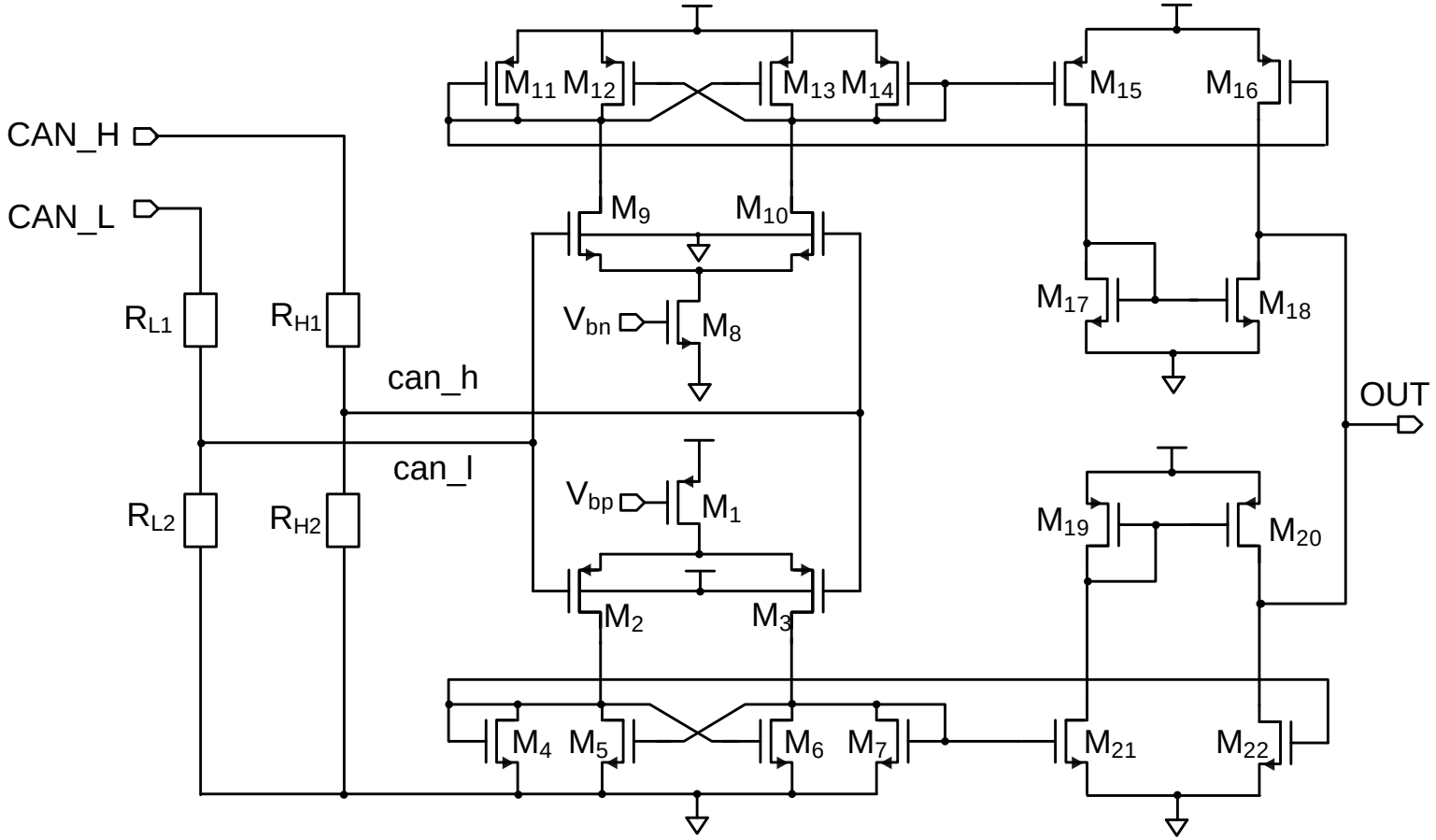
3.3V CAN Driver with levelshifter



- CAN Driver needs 3.6V CMOS signal to switch transistor M6
- Levelshifter translates EN signal from 1.2V to 3.6 V voltage level
- Levelshifter consists of lower and upper part
- Lower part is a switchable resistive voltage divider
- Divison ratio depends on switching state

- Lower part shifts signals above 2.4 V
- Upper part is classical levelshifter circuit
- Creates CMOS signal switching between 2.4V and 3.6V

CAN Receiver



- Resitive voltage division by 1/3 for CAN level to 1.2V CMOS level adaption
  - non-symmetric voltage divider for recessive state detection $R_{L1}/R_{L2} \neq R_{H1}/R_{H2}$
- Rail-to-Rail comparator stage (concept reuse from FE-I4)

CAN driver/receiver layouts