Serial Powering for the ITk Pixel Detector

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Serial Powering Meeting
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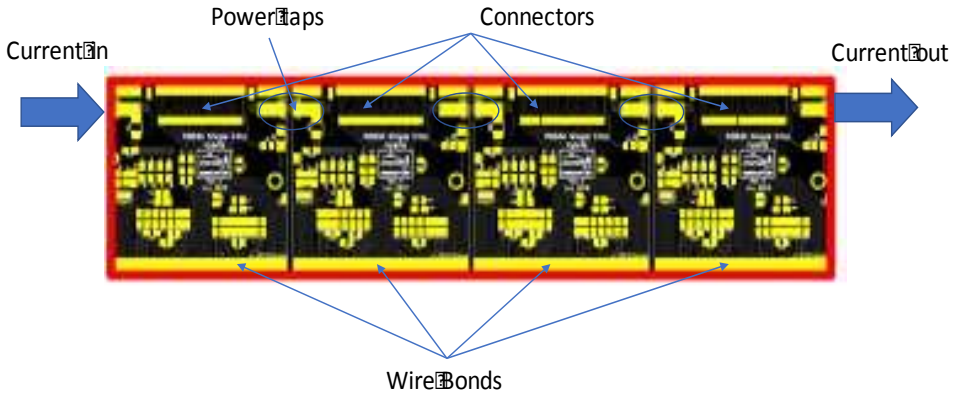
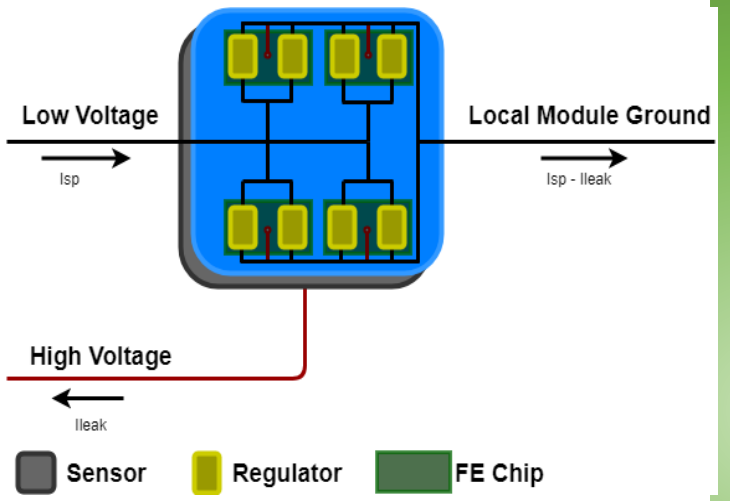
ITk Pixel Detector Basics

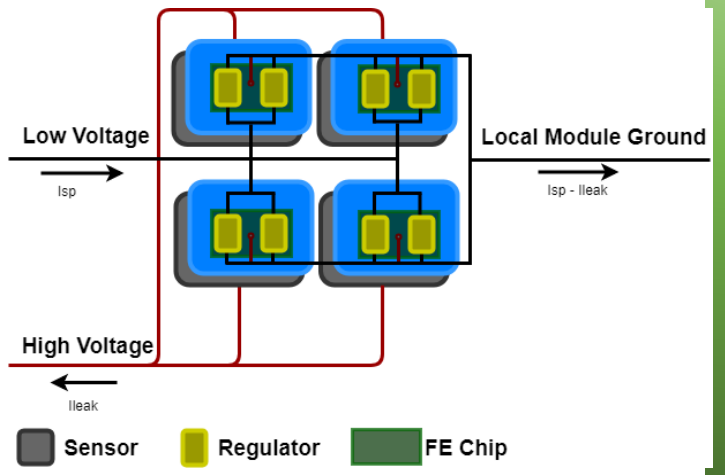
- Serial powering strategy is a new powering scheme for the ATLAS pixel detector.
  - Need to safe material (cables)
  - ITk Pixels will re-use Type3/4 powering cables → contraints on how many lines are available
- There will be a powering unit made from always 4 FE-chips.
  - Background: in case of a regulator failure we want to have the remaining ShuLDOs take the current in a safe way to keep the rest of the module working.
- Two kinds of modules:
  - Single chips modules in L0
  - Quad chip modules everywhere else
  - Single chip modules are assembled with 3D sensors, all others with planar sensors.

Powering Unit

- **Always four FE-chips are grouped in a powering unit (either 1 quad chip module, or 4 single chips modules).**
- The powering units are powered in series, while the FE-chips are in parallel within each unit.
- 5A (6A for L0) nominal /6A (7A for L0) max current
- 1.5V nominal / 1.9 V max.
- 0.5 W/cm^2 nominal / 0.7 W/cm^2 max. (plus 0.1 W/cm^2 sensor power)
- HV connections are in parallel to each sensor tile.

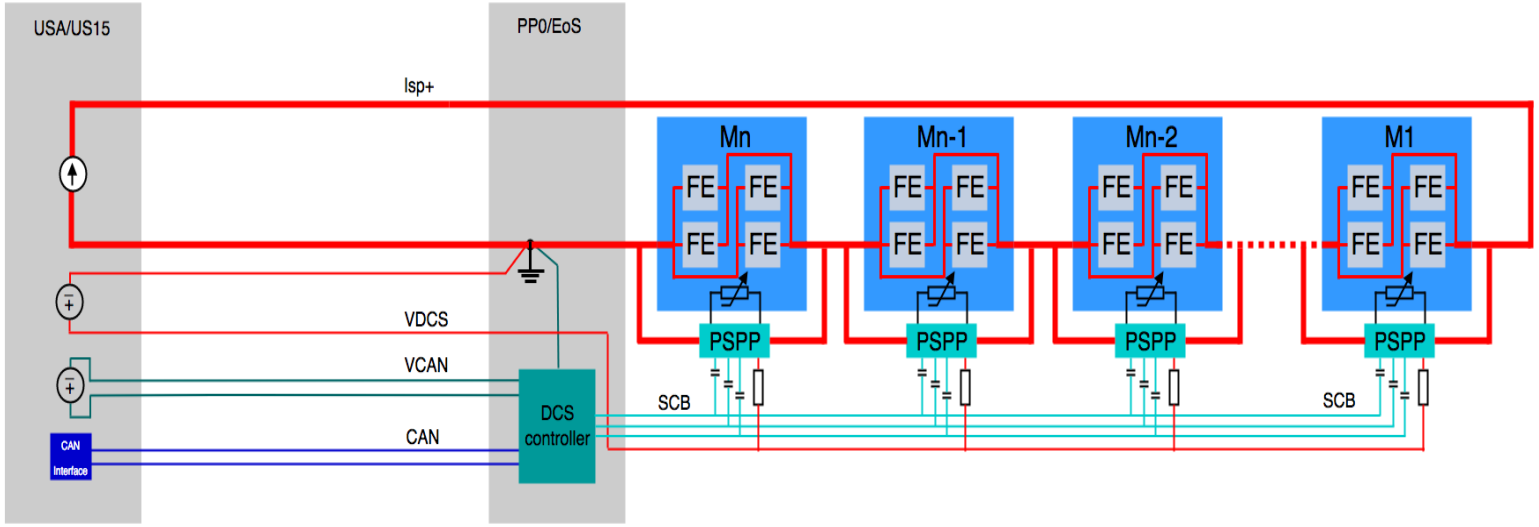






Serial Powering Chains

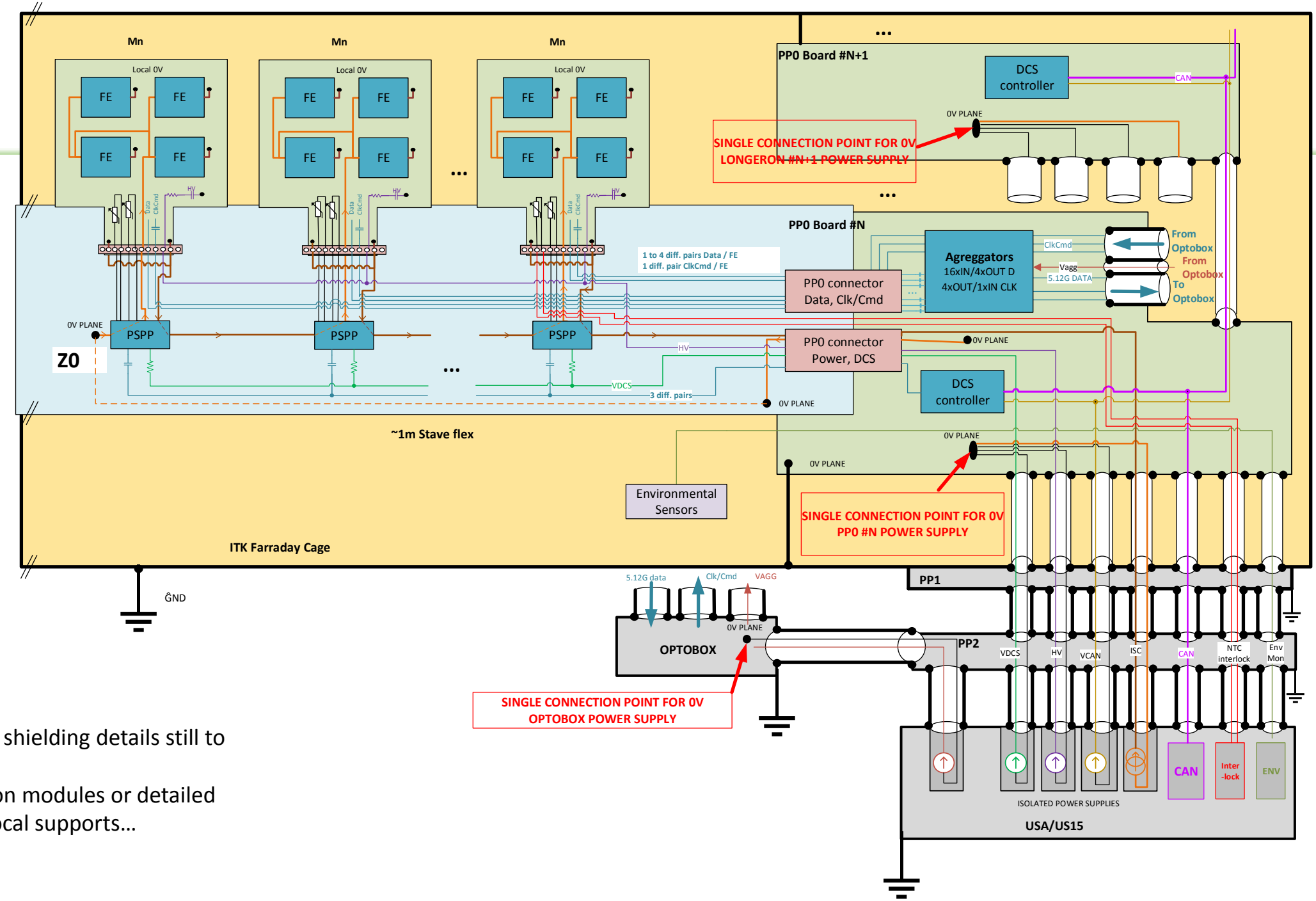
- Modules powered in series → Serial powering chain.
- Current driven
- FE chips in the module generate the needed voltage via shunt regulators → Voltage steps in between modules.
- Serial powering: less powering lines, but higher risk to loose modules due to failure in the powering system → **Protection chip (PSPP) for each module on Type-0 services.**
- Additional power lines and communication lines needed for these chips.
- Interlock system via PSPP-chip information and one hard-wired NTC per chain.



Serial Powering Chains

- Average number of modules per serial powering chain is ~10.
  - In L0 shorter chains are needed, because of the HV levels vs. local module ground. (around 4 modules per chain)
  - In the other layers chain lengths of up to 14 modules are to be realized.
- Per chain Type-0:
  - 1 LV + 1LVret
  - 1-4 HV (shared return with LV up to PP0)
  - 1 Vdcs (shared return with LV up to PP0)
  - 3 DCS chip communication bus lines (differential)
  - 1 Data in per module (differential)
  - 16 Data out per quad chip module (differential) (can be less for the outer layers)
  - 1 NTC+ and 1 NTC- for the outermost module per chain.
- PP0 is the grounding point for each SP chain. At PP0 the DCS controller ASIC is located realizing the communication between the PSPP chips and the DCS computer farm.

Serial Power Chain Sketch



Some grounding and shielding details still to be checked:
i.e. Global 0V plane on modules or detailed connections to the local supports…
Testing needed!

Summary

- Powering unit made from 4 chips always. (there might be an execption if inner rings are too difficult to connect this way → go for 3 chips instead).
- Chains between 4 modules for L0 and 14 modules in the outer system will be implemented
- Current understanding (from RD53B document) is to have nominal 5A (6A) as operation current and a max. of 6A (7A) per serial powering chain.
- HV will be supplied in parallel to the modules in the SP chains.
  - There might be several HV channels per serial powering chain (up to 4 in the inner system, up to 2 in the outer system).
- DCS chips for monitoring and as bypass instance (as a safety measure) in case of failure (still under discussion if this doesnt introduce a too high risk in the end).
  - PSPP will be located on Type-0 services
  - LV inside module will be distributed in parallel.

Backup

Pseudo-schematic of SP chain